Sustainable Green Multicore Codesigned with Compiler

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Senior Executive Vice President (2018-2022), Waseda Univ.

IEEE Computer Society President 2018

ACM/IEEE ISCA'25 General Co-Chair

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1980 BS, 82 MS, 85 Ph.D. , Dept. EE, Waseda Univ.
1985 Visiting Scholar: U. of California, Berkeley,
1986 Assistant Prof., 1988 Associate Prof., 1989-90 Research Scholar: U. of Illinois, Urbana-Champaign, Center for Supercomputing R&D, 1997 Prof.,
2004 Director, Advanced Multicore Research Institute,
2017member: the Engineering Academy of Japan
(2020- Board Mem) and the Science Council of Japan
2018 IEEE Computer Society President
Senior Exectutive Vice President, Waseda U. (2018-22)

AWARD: 1987 IFAC World Congress Young Author Prize
1997 IPSJ Sakai Special Research Award,
2005 STARC Academia-Industry Research Award,
2008 LSI of the Year Second Prize,
2008 Intel Asia Academic Forum Best Research Award,
2010 IEEE CS Golden Core Member Award
2014 Minister of Edu., Sci. & Tech. Research Prize
2015 IPSJ Fellow, 2017 IEEE Fellow, Eta Kappa Nu
2019 Spirit of IEEE Computer Society Award,
2020 IPSJ Contribution Award, , 2023 IEEE Life Fellow

Reviewed Papers: 243, Invited Talks: 246,
Granted Patents: 72 (Japan, US, GB, DE, China),
Articles in News Papers, Web News, TV etc.: 713

Committees in Societies and Government 300
IEEE Computer Society: President 2018, Executive Committee(2017-2019), BoG(2009-14), Strategic Planning Committee Chair 2018, Multicore STC Chair (2012-), Japan Chair(2005-07),
IPSJ Chair: HG for Magazine. & J. Edit, Sig. on ARC.
【METI/NEDO】 Project Leaders: Multicore for Consumer Electronics, Advanced Parallelizing Compiler,
Chair: Computer Strategy Committee【Cabinet Office】
CSTP Supercomputer Strategic ICT PT, Japan Prize Selection Committees, etc.
【MEXT】Info. Sci. & Tech. Committee, Supercomputers Development Member (Top 1:NWT, Earth Simulator, K)
JST SPRING Ph.D Promotion Chair, Boost AI Ph.D. Boosting Chair, SBIR Phase 1 Chair, Moonshot Project G3 Robot & AI Advisor & Int'l Symp Vice Chair,
【COCN】Council of Competitiveness Nippon Ex-Board

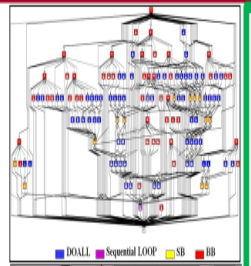
Research on OSCAR Parallelizing Compiler & Co-designed Hardware Since 1984

72 international patents in USA, UK, China, Japan to improve effective performance, cost-performance, software productivity and power efficiency

High Performance & Low Power

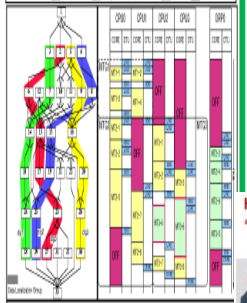
1) Multigrain Parallelization for Embedded to HPC Homogeneous and Heterogeneous Multicores

Coarse-grain task parallelism among loops, subroutines & basic blocks in addition to the loop parallelism



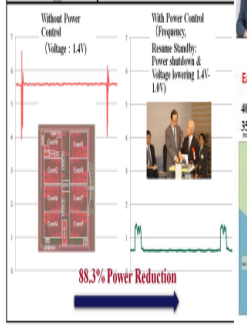
2) Data Localization:
Optimization of Cache & Local Memory Usage

- Automatic data decomposition and data reuse control for Distributed shared memory, Cache and Local memory
- Data Transfer Control
  - Overlapping Data Transfer using Data Transfer Unit, or DMAC



3) Automatic Power Reduction

- OSCAR Compiler can reduce power consumption by using DVFS and Clock- & Power- gating with hardware supports.



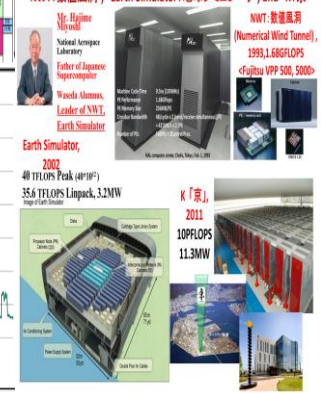
4) Codesigned Accelerator: See right figure

Green Accelerator

can be attached to any processor cores, RISCV, arm, Infineon Renesas, AMD, Intel, etc, without instruction extensions.

- It works with automatic local memory management and power reduction control by OSCAR Automatic vectorizing & parallelizing compiler

H. Kasahara was a member of 3 World No.1 Supercomputers "NWT:数値風洞", "Earth Simulator:地球シミュレータ", and "K:京"



Demo of NEDO Green Multicore Processor for Real Time Consumer Electronics at Council of Science and Engineering Policy on April 10, 2008

http://www8.cao.go.jp/cstp/gaiyo/honkaigi/74index.html

第74回総合科学技術会議【平成20年4月10日】


第74回総合科学技術会議の様子(1)

第74回総合科学技術会議の様子(2)

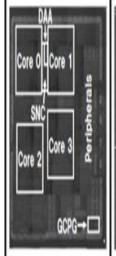
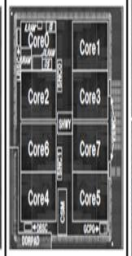
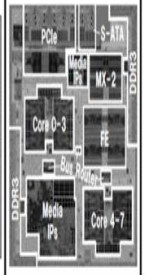

第74回総合科学技術会議の様子(3)


第74回総合科学技術会議の様子(4)

Prime Minister FUKUDA is touching our multicore chip during execution.

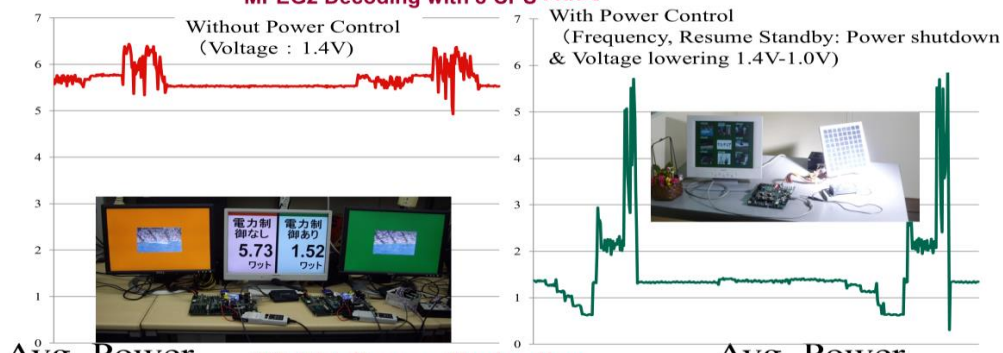
Codesign of Compiler and Multiprocessor Architecture since 1985

4 core multicore RP1 (2007), 8 core multicore RP2 (2008) and 15 core Heterogeneous multicore RPX (2010) developed in NEDO Projects with Hitachi and Renesas

RP-1 (ISSCC2007 #5.3)	*RP-2* (ISSCC2008 #4.5)	*RP-X* (ISSCC2010 #5.3)
		
90nm, 8-layer, triple-Vth, CMOS	90nm, 8-layer, triple-Vth, CMOS	45nm, 8-layer, triple-Vth, CMOS
97.6 mm² (9.88 x 9.88 mm)	104.8 mm² (10.61 x 9.88 mm)	153.8 mm² (12.4 x 12.4 mm)
1.0V (internal), 1.8/3.3V (I/O)	1.0-1.4V (internal), 1.8/3.3V (I/O)	1.0-1.2V (internal), 1.2-3.3V (I/O)
600MHz, 4.32 GIPS, 16.8 GFLOPS	600MHz, 8.64 GIPS, 33.6 GFLOPS	648MHz, 13.7GIPS, 115GOPS, 36.2GFLOPS
11.4 GOPS/W (32b換算)	16.3 GOPS/W (32b換算)	37.3 GOPS/W (32b換算)

Power Reduction of MPEG2 Decoding to 1/4 on 8 Core Homogeneous Multicore RP-2 by OSCAR Parallelizing Compiler

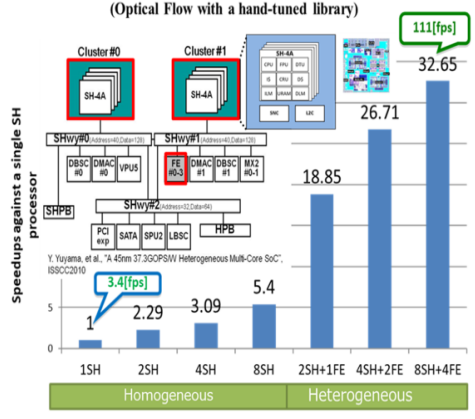
MPEG2 Decoding with 8 CPU cores



Speedups & Power Reduction on RP-X Heterogeneous Multicore with 8 CPUs and 4 DRPs

33 Times Speedup Using OSCAR Compiler and API on Renesas RP-X with 8 CPUs & 4 DRP Accelerators

(Optical Flow with a hand-tuned library)

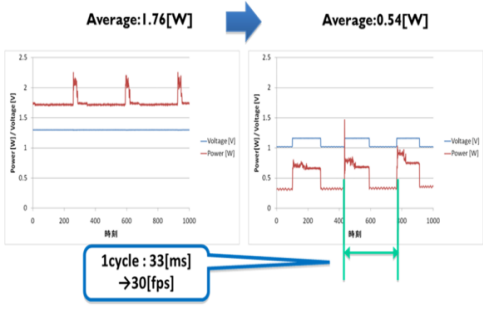


Power Reduction in a real-time execution controlled by OSCAR Compiler and OSCAR API on RP-X (Optical Flow with a hand-tuned library)

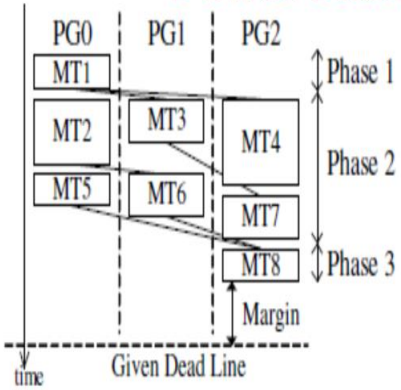
Without Power Reduction

With Power Reduction by OSCAR Compiler

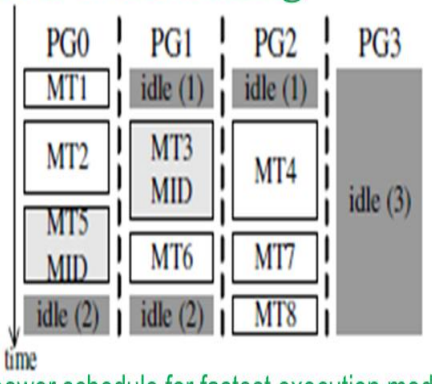
70% of power reduction



Power Reduction Scheduling



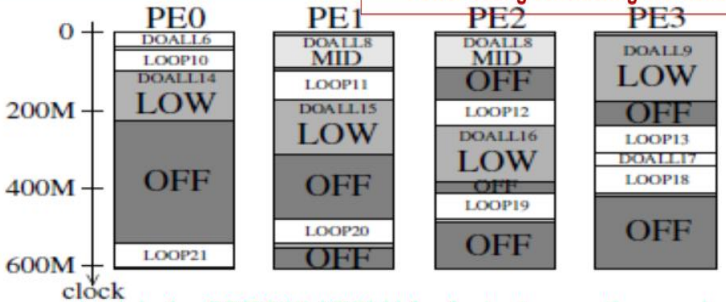
A macrotask graph assigned to 3 cores



A power schedule for fastest execution mode

Realtime scheduling mode
MTs 1,4,7,8 are on Critical Path (CP)

1) Reduce frequencies (Fs) of MTs on CP considering dead line.
2) Reduce Fs of MTs not on CP. Idle: Clock or Power Gating considering overheads.



A power schedule for SPEC95 APPLU for fastest execution mode

Doall6, Loop 10,11,12,13, Doall 17, Loop 18,19,20, 21 are on CP

An Image of Static Schedule for Heterogeneous Multi-core with Data Transfer Overlapping and Power Control