

Automatic Speedup and Secure Multicore



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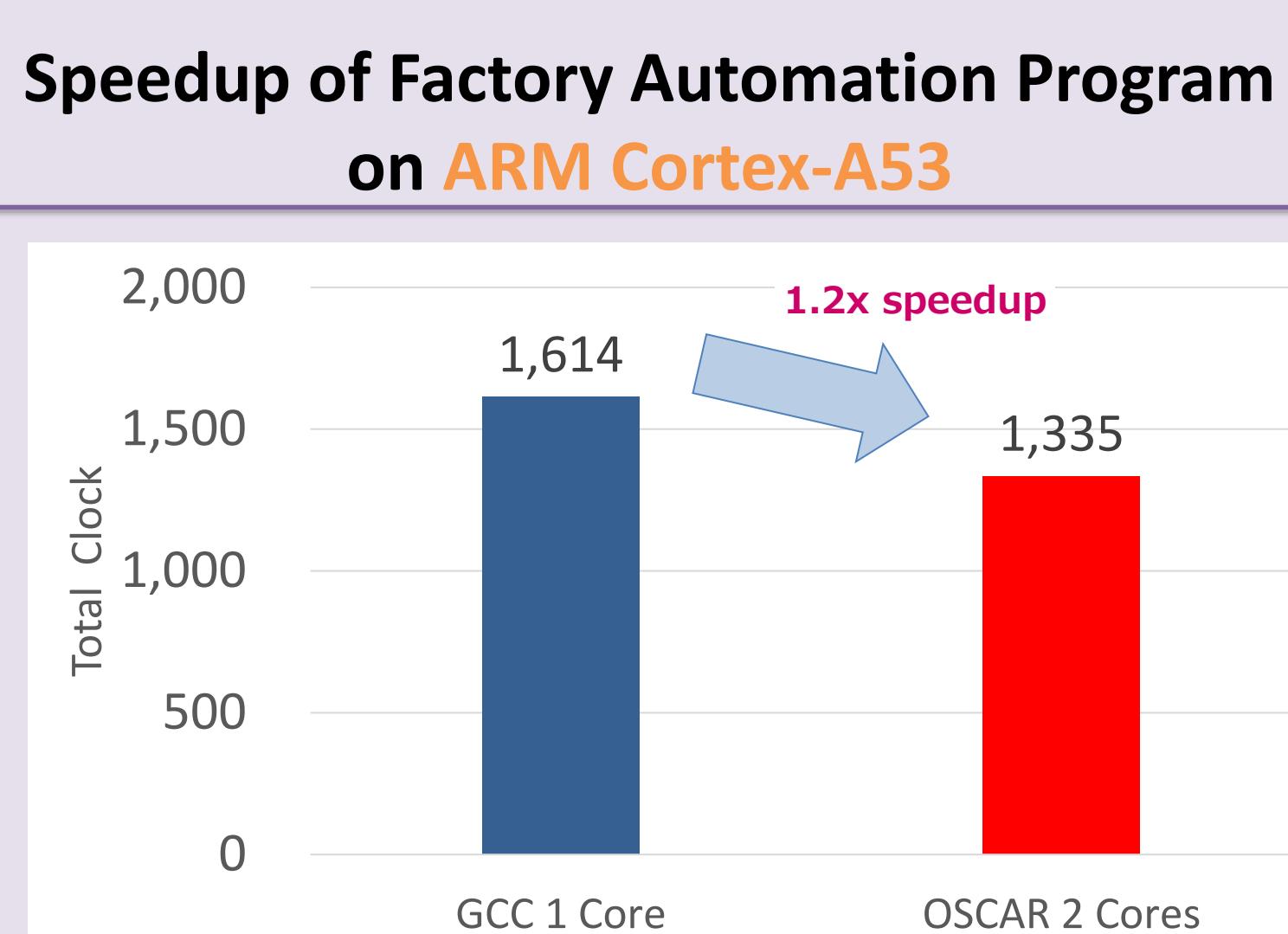
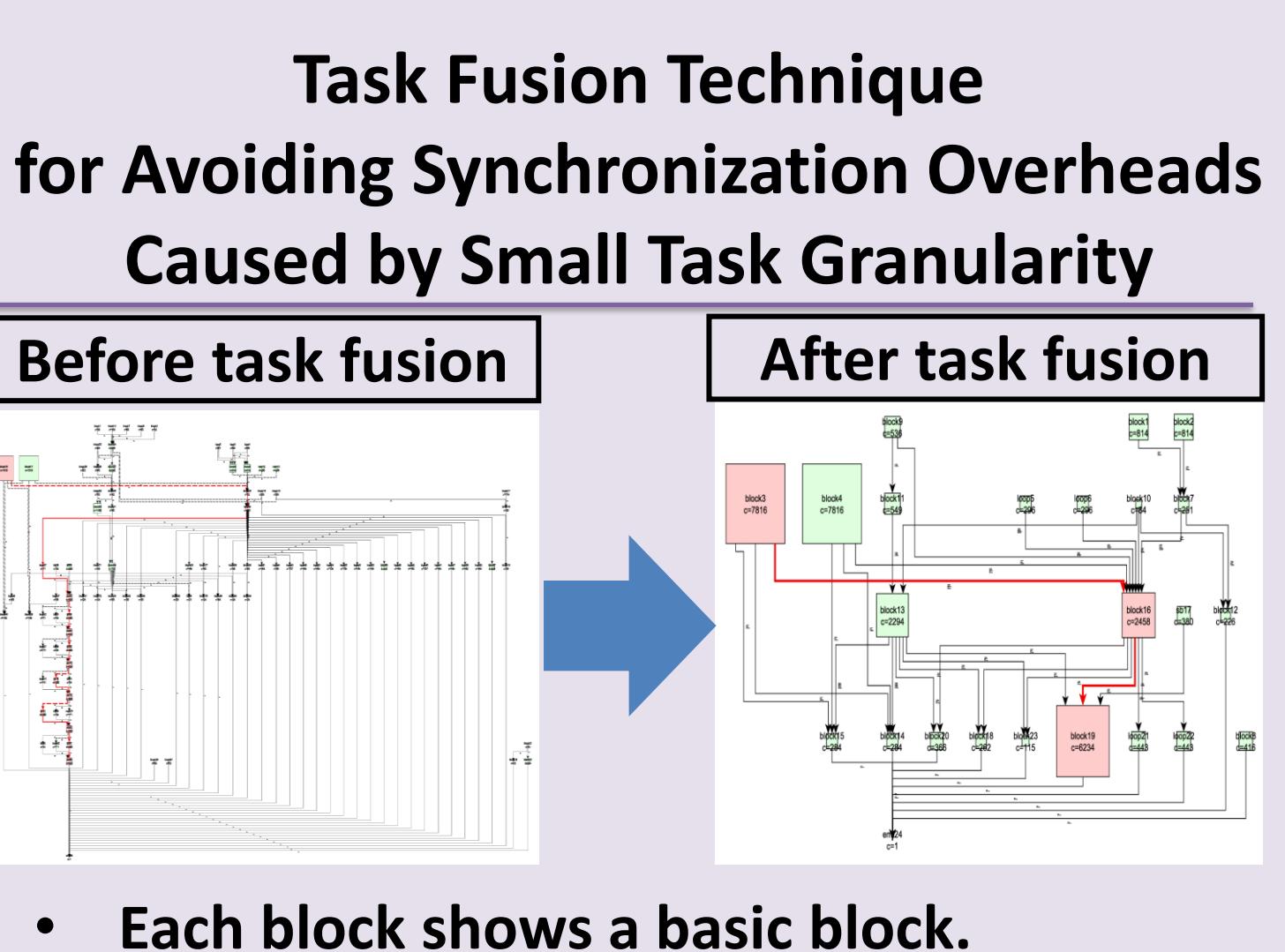
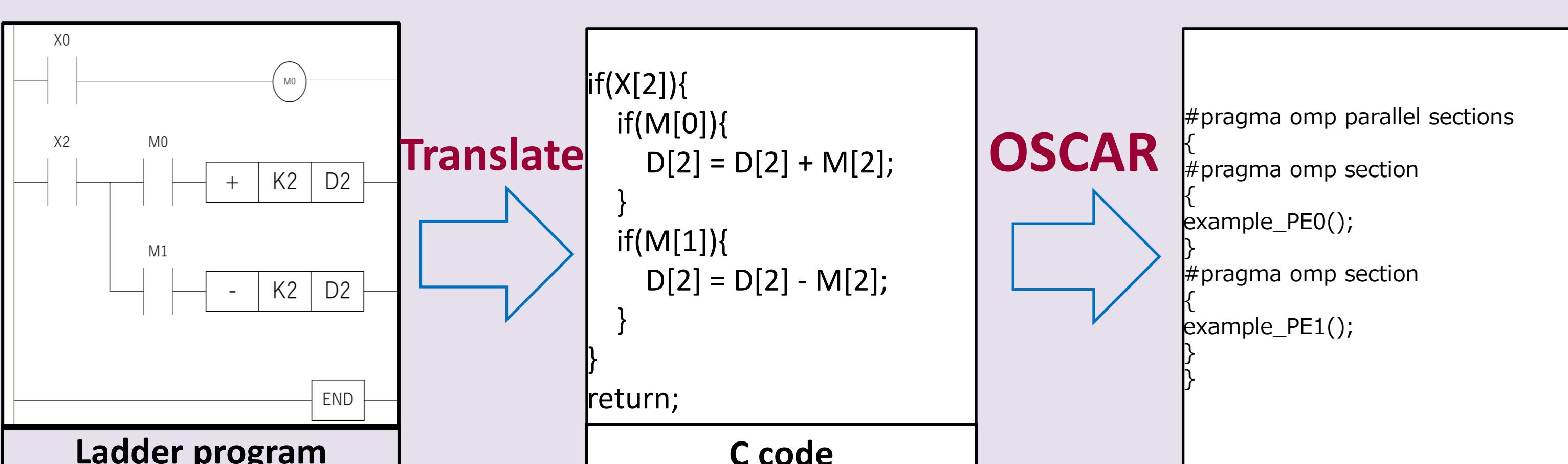
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Parallel Processing of Ladder Programs for Factory Automation by the OSCAR Compiler

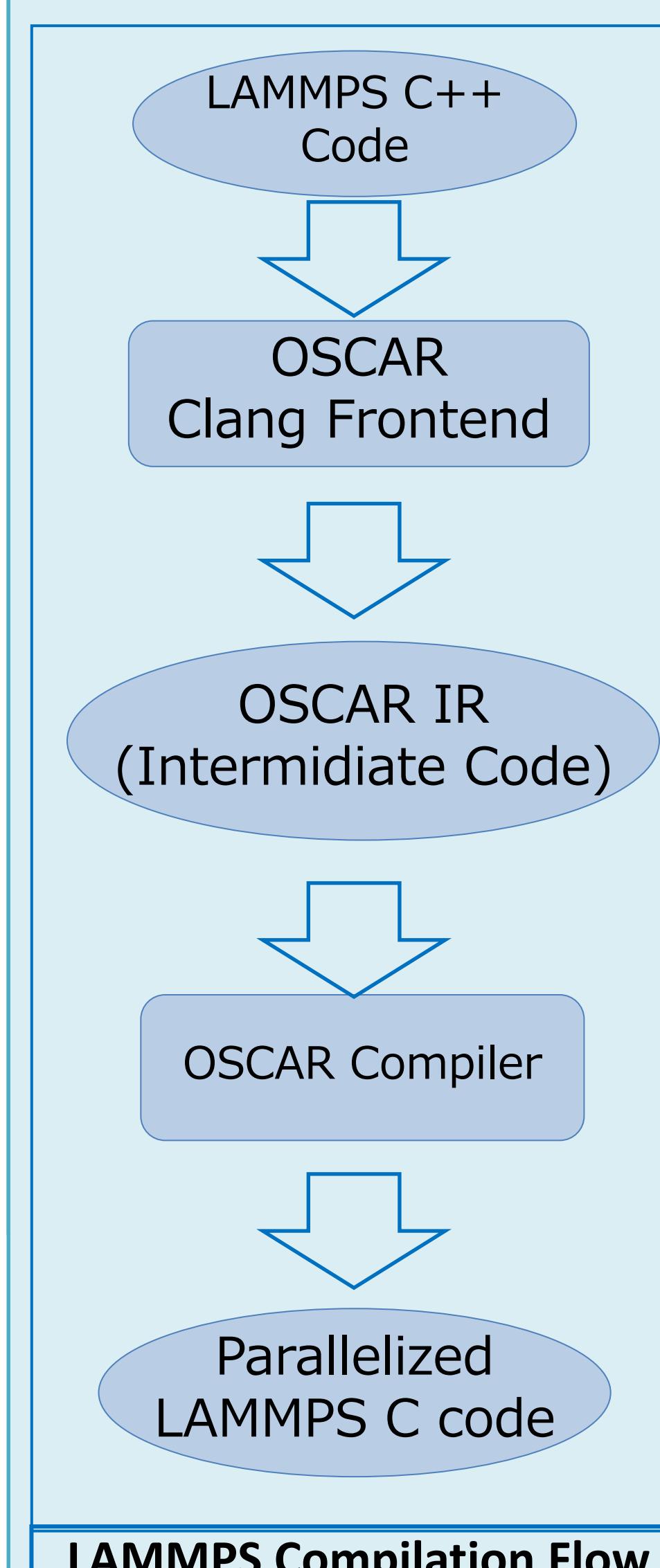
Our Proposal:

Automatic Parallelizing Compilation Flow for Ladder Programs

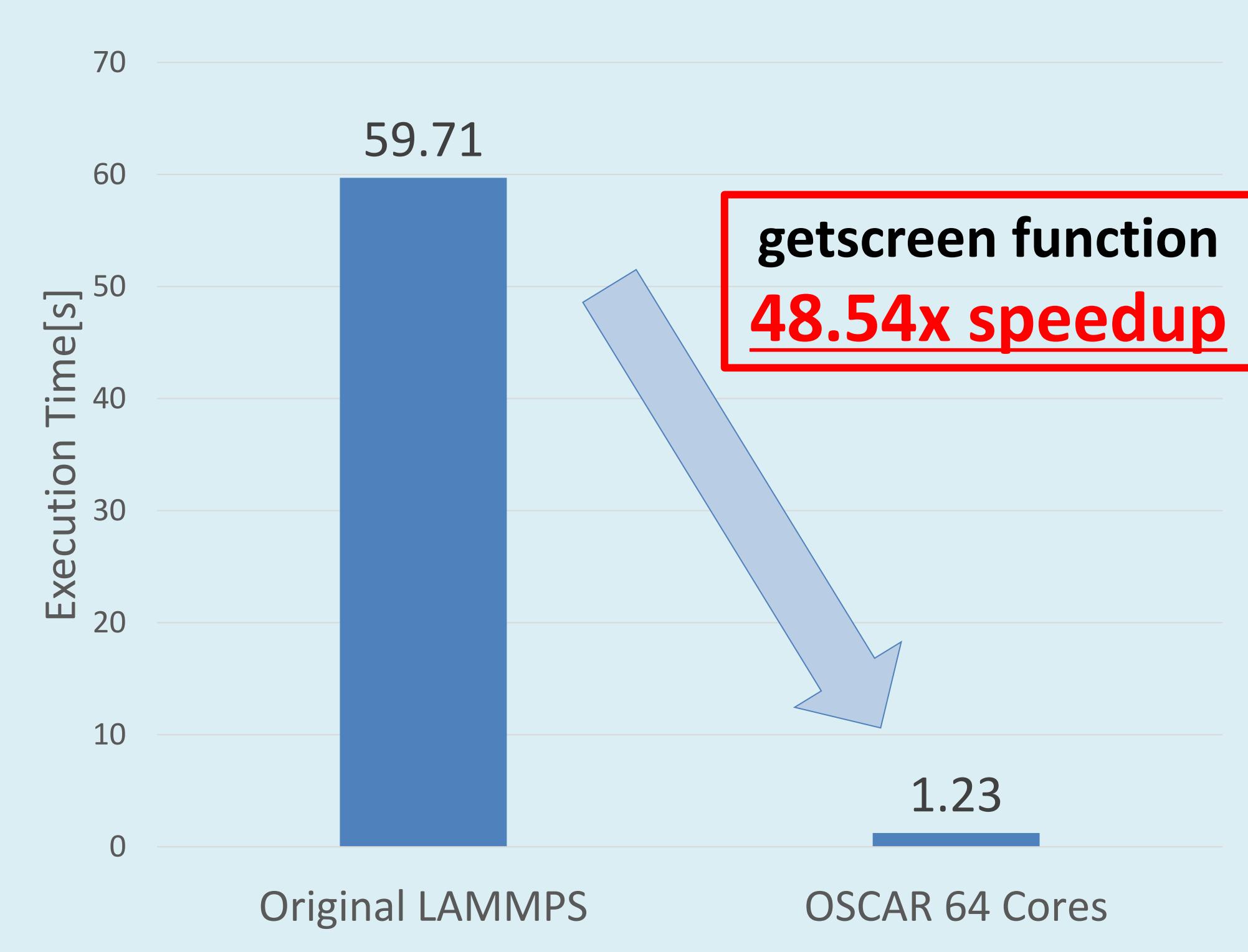


LAMMPS Speedup on Intel 64 cores by the OSCAR Compiler

Parallelization of LAMMPS C++ code by OSCAR Compiler



Execution Time of "LAMMPS MEAM Potential Getscreen" Function on Intel Xeon Gold 6448Y



Original LAMMPS on 64 threads consumed 59.7[s]
OSCAR Compiler Reduced It to 1.2[s]

NAS Parallel Benchmark CG Class C Speedup on AMD EPYC 64-core processor by the OSCAR Compiler

Computational Environment

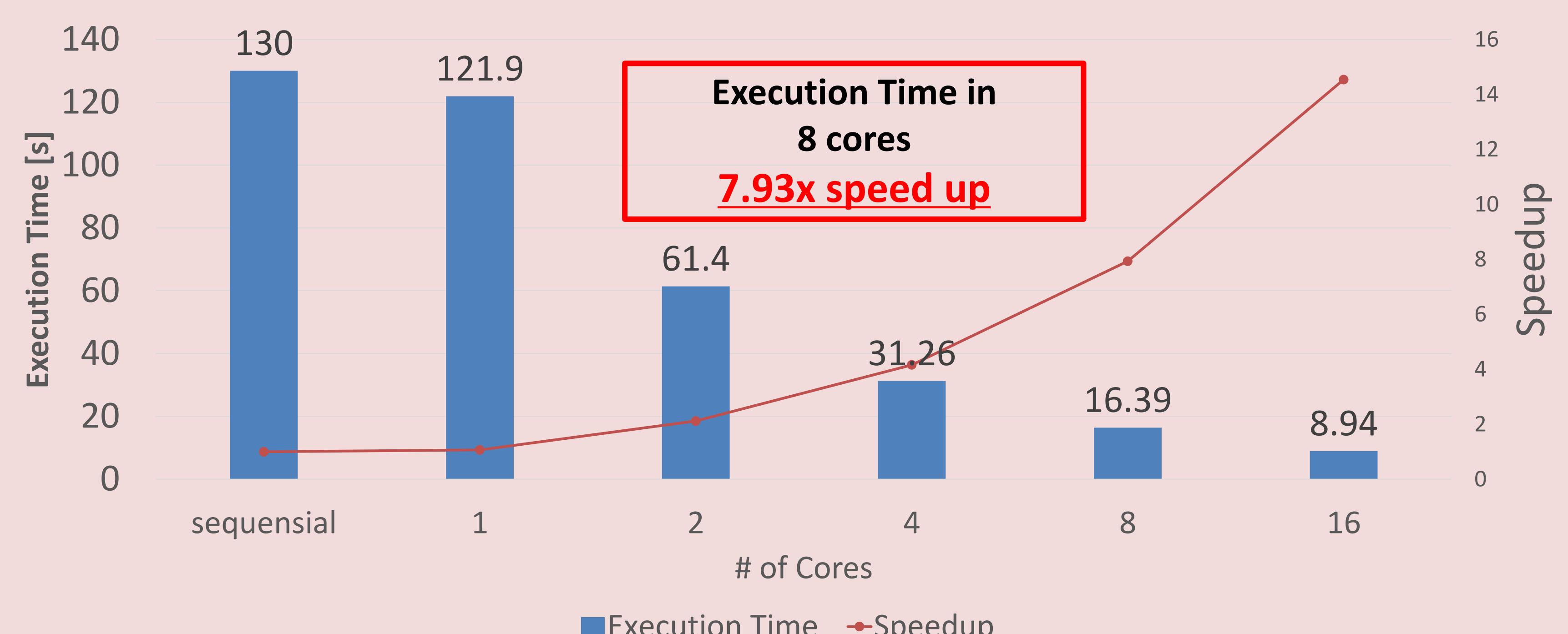
CPU: AMD EPYC 7702P × 1
Zen 2 "Rome" architecture
64 cores, 64 threads
2.0 [GHz] base frequency
3.35 [GHz] boost frequency
32 [KiB] L1d cache
512 [KiB] L2 cache
256 [MiB] L3 cache
Grouped into 4-core clusters

Memory: DDR4-3200 ECC Registered
64GB × 8 modules (total 512 [GB])

NUMA topology: Configured as 1 NUMA node

Problem Class: NPB CG C

Speedup of NAS Parallel Benchmark CG Class C on AMD EPYC 7702P



Future Security Extension – Performance Improvements on RISC-V TEEs

Trusted Execution Environments (TEEs)

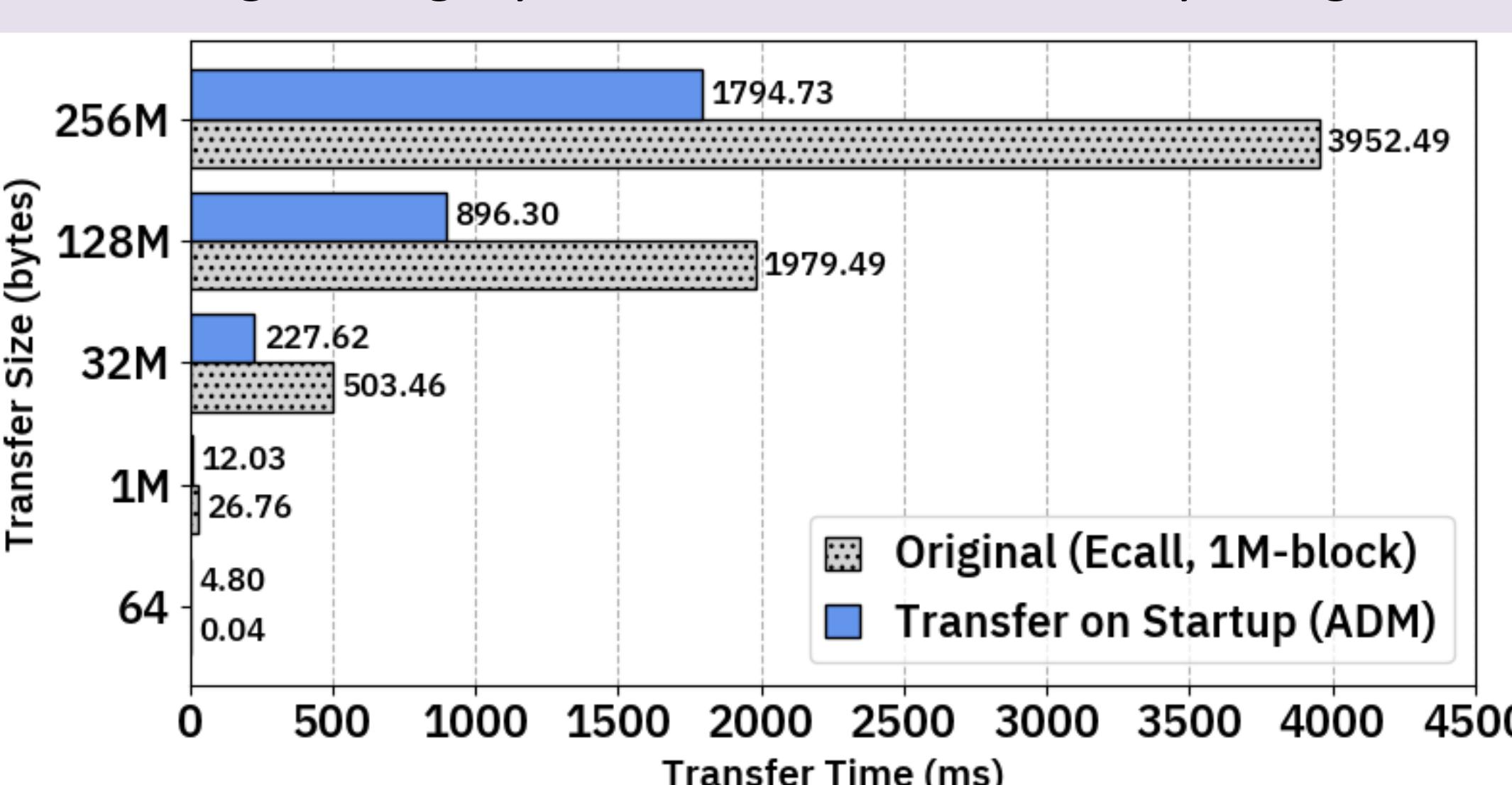
- Secure environments isolated from the host systems
- Do not trust even the operating systems
- e.g., Intel SGX, ARM TrustZone, RISC-V Keystone Enclave

Issues on Keystone Enclave

- TEEs need a data transfer method with the host system to send/receive data processed in the enclave to delegate system-related operation (e.g., I/O)
- Keystone has **insecure, inflexible** data transfer method
 - Not suitable for large data (too much overhead)
 - Overlook integrity of the data

Keyston Enclave with ADM

- We introduce the memory region dedicated to secure and flexible data transfer, Additional Data Memory (ADM).
- Dynamic access permission controls and data verifications realize stronger integrity and more flexible memory sizing.



For large data (>1M)
2.2x speed up

Evaluated on
HiFive Unmatched
(RISC-V Physical System)