OSCAR Power Reduction Multicore Compiler

Kasahara & Kimura Lab, Waseda University, TOKYO
K. Takamatsu, J. Pickar, B. Magnussen, H. Mikami, K. Kimura, H. Kasahara
http://www.kasahara.cs.waseda.ac.jp

OSCAR Automatic Parallelizing Compiler

To improve effective performance, cost-performance and software productivity and reduce power

Multigrain Parallelization

coarse-grain parallelism among loops and subroutines, near fine grain parallelism among statements in addition to loop parallelism

Data Localization

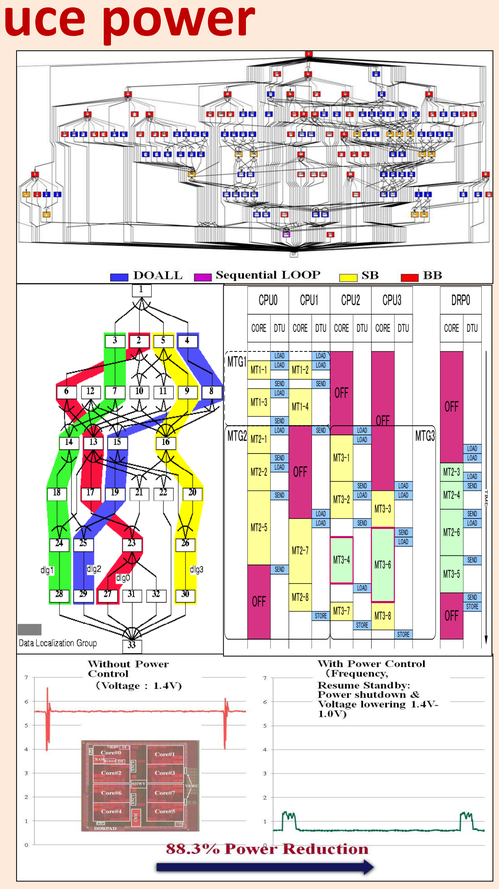
Automatic data management for distributed shared memory, cache and local memory

Data Transfer Overlapping

Data transfer overlapping using Data Transfer Controllers (DMAs)

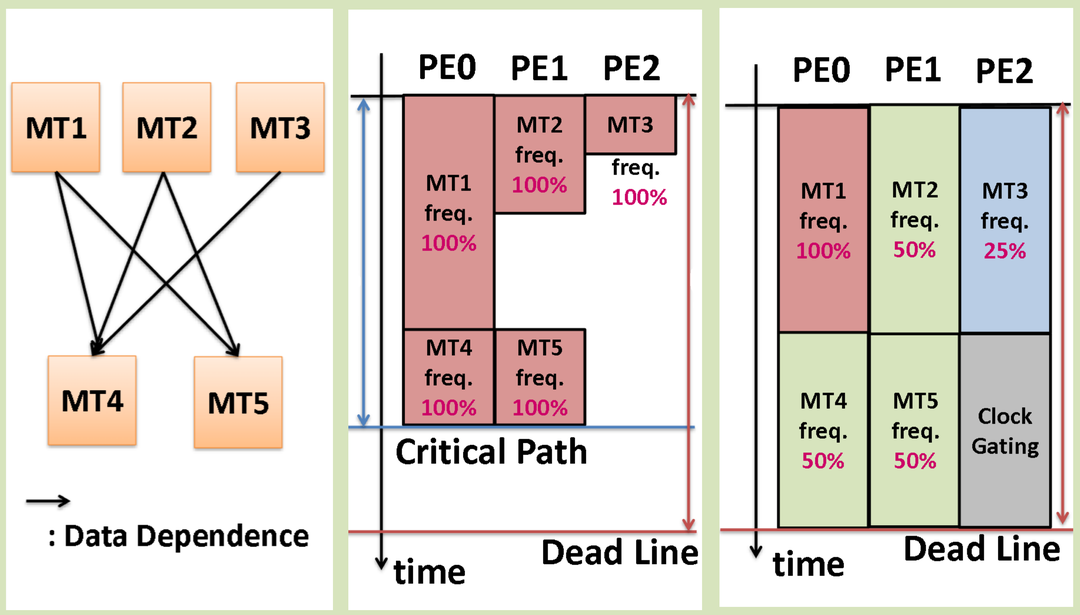
Power Reduction

Reduction of consumed power by compiler control DVFS and Power gating with hardware supports.



Saving Energy by Compiler

Parallelization → Power Reduction



Task graph | **Tasks assigned to 3 cores** | **Schedule Minimizing Power**

Software Coherent Cache

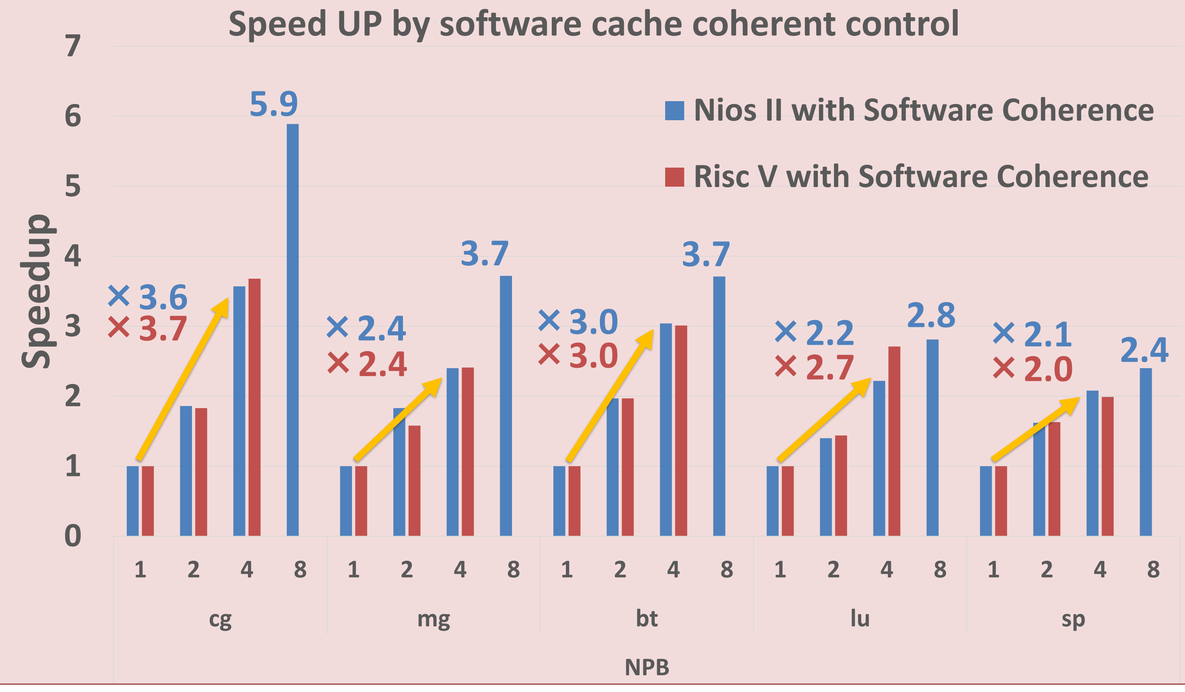
Parallelizing compiler directed software coherence technique for shared memory multicore systems without hardware cache coherence control

Advantages

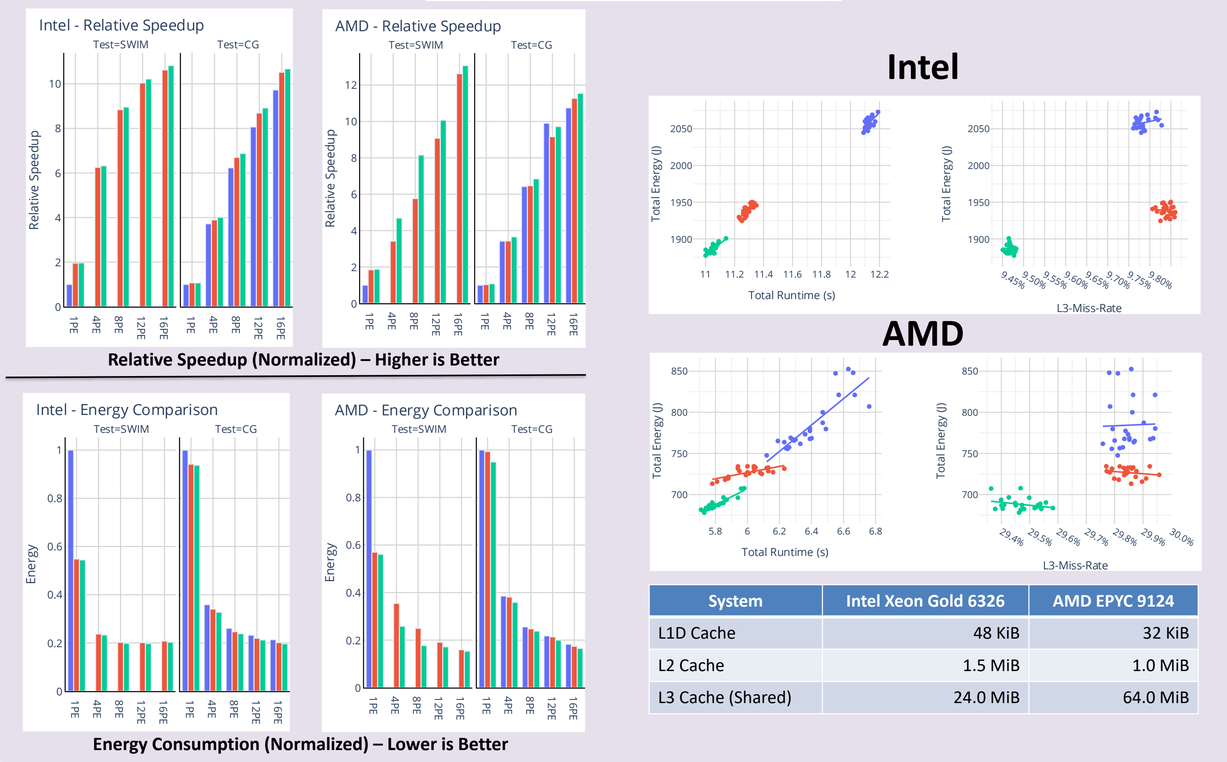
- Smaller hardware and lower power consumption brought by removing expensive hardware cache coherence mechanism
- Higher performance by compiler's careful cache operation scheduling as well as memory optimization

Evaluation

- NIOS II / Risc V multicore system implemented in Arria10 SoC FPGA
  - I$: 32KB / D$:32KB (Each PE)
  - # of PE: 1PE, 2PE, 4PE, 8PE (only NIOS II)
- Application
  - NAS Parallel Benchmarks



RAPL Energy Consumption of "SWIM" & "NPB CG" OpenMP and Automatically Generated Code by OSCAR on Intel & AMD 16 Cores



System	Intel Xeon Gold 6326	AMD EPYC 9124
L1D Cache	48 KiB	32 KiB
L2 Cache	1.5 MiB	1.0 MiB
L3 Cache (Shared)	24.0 MiB	64.0 MiB

Automatic Power Reduction of OpenCV Face Detection on big.LITTLE ARM Processor