世界最速のコンピュータってどんなの？

早稲田大学　理工学術院　情報理工学科　教授　笠原博徳

IEEE Computer Society President 2018, 早稲田大学副総長(2018-2022)

JST博士学生支援事業SPRING/BOOST委員長/ ACM・IEEE ISCA(コンピュータアーキテクチャ会議)2025実行委員長

1980 早大電気工学科卒、1982 同修士課程了
1985 早大大学院博士課程了 工学博士,学振第一回PD
　　カリフォルニア大学バークレー客員研究員
1986 早大理工専任講師、1988年 助教授
1989-1990 イリノイ大学Center for
　　Super computing R&D客員研究員
1997 教授、現在 理工学術院情報理工学科
2004 アドバンストマルチコア研究所所長
2017 日本工学アカデミー会員、 日本学術会議連携会員
2018 IEEE Computer Society会長、
　　早大副総長（-2022年9月）
2019-2023　産業競争力懇談会(COCN) 理事
2020-2024 日本工学アカデミー理事
2023- ACM/IEEE ISCA2025@Tokyo 実行委員長

【受賞】
1987 IFAC World Congress Young Author Prize
1997 情報処理学会坂井記念特別賞
2005 半導体理工学研究センタ共同研究賞
2008 LSI・オブ・ザ・イヤー 2008 準グランプリ、
　Intel Asia Academic Forum Best Research Award
2010 IEEE CS Golden Core　Member Award
2014 文部科学大臣表彰科学技術賞研究部門
2015 情報処理学会フェロー
2017 IEEE Fellow,　IEEE Eta-Kappa-Nu
2019 IEEE CS Spirit of Computer Society Award
2020 情報処理学会功績賞、SCAT表彰 会長大賞
2023 IEEE Life Fellow

査読付き論文234件、招待講演244、国際特許取得70件(米・英・中・日等)、
新聞・Web記事・TV等メディア掲載 709件

【政府・学会委員等】 歴任数 300件
IEEE Computer Society President 2018、Executive Committee委員長、理事(2009-14)、戦略的計画委員会委員長、Nomination Committee委員長、Multicore STC 委員長、IEEE CS Japan委員長、IEEE技術委員、IEEE Medal選定委員、ACM/IEEE SC'21基調講演選定委員等
【経済産業省・NEDO】情報家電用マルチコア・アドバンスト並列化コンパイラ・グリーンコンピューティング・プロジェクトリーダ、NEDOコンピュータ戦略委員長等
【内閣府】スーパーコンピュータ戦略委員、政府調達苦情検討委員、総合科学技術会議情報通信PT 研究開発基盤領域&セキュリティ・ソフト検討委員、日本国際賞選定委員
【文部科学省】地球シミュレータ（ES）中間評価委員、情報科学技術委員、HPCI計画推進委員、次世代スパコン（京）中間評価委員・概念設計評価委員、地球シミュレータES2導入技術アドバイザイリー委員長等、
JST: ムーンショットG3ロボット&AIアドバイザ, 博士学生支援事業SPRING/ BOOST委員長,SBIRフェーズ1委員長,大学発新産業創出基金事業ガバニングボード

早稲田大学理工展，2024年11月3日（日）午前11:00-11:45, 61号館 2F 202室

USA President:
Bill Clinton

USA Ambassador:
Caroline Kennedy

Chinese President:
Hu Jintao

WASEDA University

Tokyo, Japan

Microsoft:
Dr. Bill Gates

British Prime Minister:
Boris Johnson

1882 》
Okuma Shigenobu
founded Tokyo
Senmon Gakko
(College)

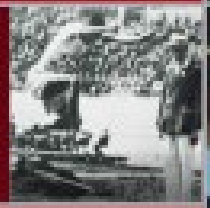
The "Group of Four" who contributed to
the development of Waseda University

1903 》
Start of the Waseda-Keio baseball match (Jubilee)

早稲田大学

《 1922
Visit by physicist Albert Einstein to
Waseda University

Archaeological excavation of
the Amarna site



1928 》
Japan's first gold medalist

1993 》
Visit to Waseda University
by then U.S. President
Bill Clinton

《 1940
"Vows for life"
from diplomat Chiune Sugihara

1956 》
The beginnings of the Ishibashi Cabinet, first
alumnus of Waseda to become Prime Minister

2007 》
150th founding anniversary...
toward the "second establishment"
of the university

《 1962
Robert Kennedy attends
student awards

《 2012
Formulation of Waseda Vision 150

Alibaba
Mr. Jack Ma

WASEDA UNIVERSITY

Waseda University
早稲田大学

Number of International Students
7,942 from 125 countries and territories

Alumni CEOs in Japan
10,606

9 Prime Ministers

Founder Shigenobu OKUMA

Graduate Employability
#1 in private university of Japan
(#2 in Japan, #27 in the world)
QS Graduate Employability Rankings 2019

0% Schools

ALUMNI [卒業生]	PARTNER INSTITUTIONS [協定大学・機関]
630,000	848 (93 countries)

Hiroshi YAMAUCHI

Masaru IBUKA

Tadashi YANAI

https://www.kantei.go.jp/jp/rekidaina/kaku/index.html

mercari HEROZ JAPAN

FACULTY [教員]	ENROLLMENT [学生数]	UNDERGRADUATE STUDENTS [学部生]	GRADUATE STUDENTS [大学院生]
5,468	49,436	41,051	8,385

* Entire Year 2018

NUMBER OF BOOKS [図書館蔵書]
5,800,000

Prime Ministers	Business Leaders	Business Leaders
	Founders of global companies	CEOs of global companies
8th Shigenobu Okuma		ANA (All Nippon Airways)
17th Shigenobu Okuma		HONDA
55th Tanzan Ishibashi		Nintendo
74th Noboru Takeshita	Sony	UNIQLO
76th Toshiki Kaifu	Samsung	Shiseido
84th Keizo Obuchi	Casio	Nomura Securities Co., Ltd.
85th Yoshiro Mori	LOTTE	Tokio Marine & Nichido Fire Insurance Co., Ltd.
91st Yasuo Fukuda		Olympus Corporation
95th Yoshihiko Noda		
100th Fumio Kishida		

Aiji TANAKA
President International Political Science Association (IPSA) President 2016

Hironori KASAHARA
Senior Executive Vice President IEEE Computer Society President 2018. The first president from outside USA and Canada in 72 years CS history. CS has 84,000 members from 168 countries.

芸術功労者表彰
Sayuri Yoshinaga

Toshio FUKUDA
The University Professor Waseda, Waseda Alumnus, Prof. Emeritus Nagoya Univ., Prof. Meiji Univ. IEEE President 2020. The first from Asia in 135 years history. IEEE has 420,000 members.

Haruki MURAKAMI

Hirokazu KOREEDA

Yuzuru HANYU

S. ARAKAWA

Yui Suzaki

Oxford Univ.で笠原グリーンコンピューティング招待講演(2019年11/13)

_日本で唯一、早稲田はオックスフォードと大学間協定締結

Oxford大は、2017年よりTHE大学ランキング8年連続No.1

前Vice Chancellor Prof. Louise Richardson
(WoI 2020での基調講演(予定))
Head of Astrophysics：Prof. Rob Fender
Dept. of Physics: Prof. Ian Shipsey
Astrophysics: Prof. H.Falche, et. al.

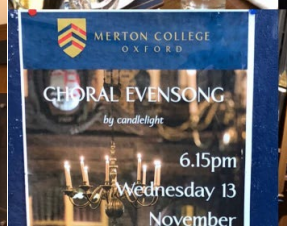
現Vice Chancellor Prof. Irene Tracy
前Merton College Warden
Fellow: Dr. Peter Braam
Sub Warden: Prof. Judy Armitage
CS: Prof. Jeremy Gibbons

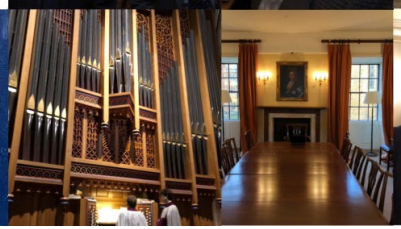













Choral Evensong, 750th Anniversary Room

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https://www.top500.org/

June 2023

TOP 500 The List.

FIND OUT MORE AT top500.org

2021 ACM A.M. Turing Award: Prof. Jack Dongarra, Univ. of Tennessee
https://amturing.acm.org/award_winners/dongarra_3406337.cfm

For his pioneering contributions to numerical algorithms and libraries that enabled high performance computational software to keep pace with exponential hardware improvements for over four decades

JUNE 2023

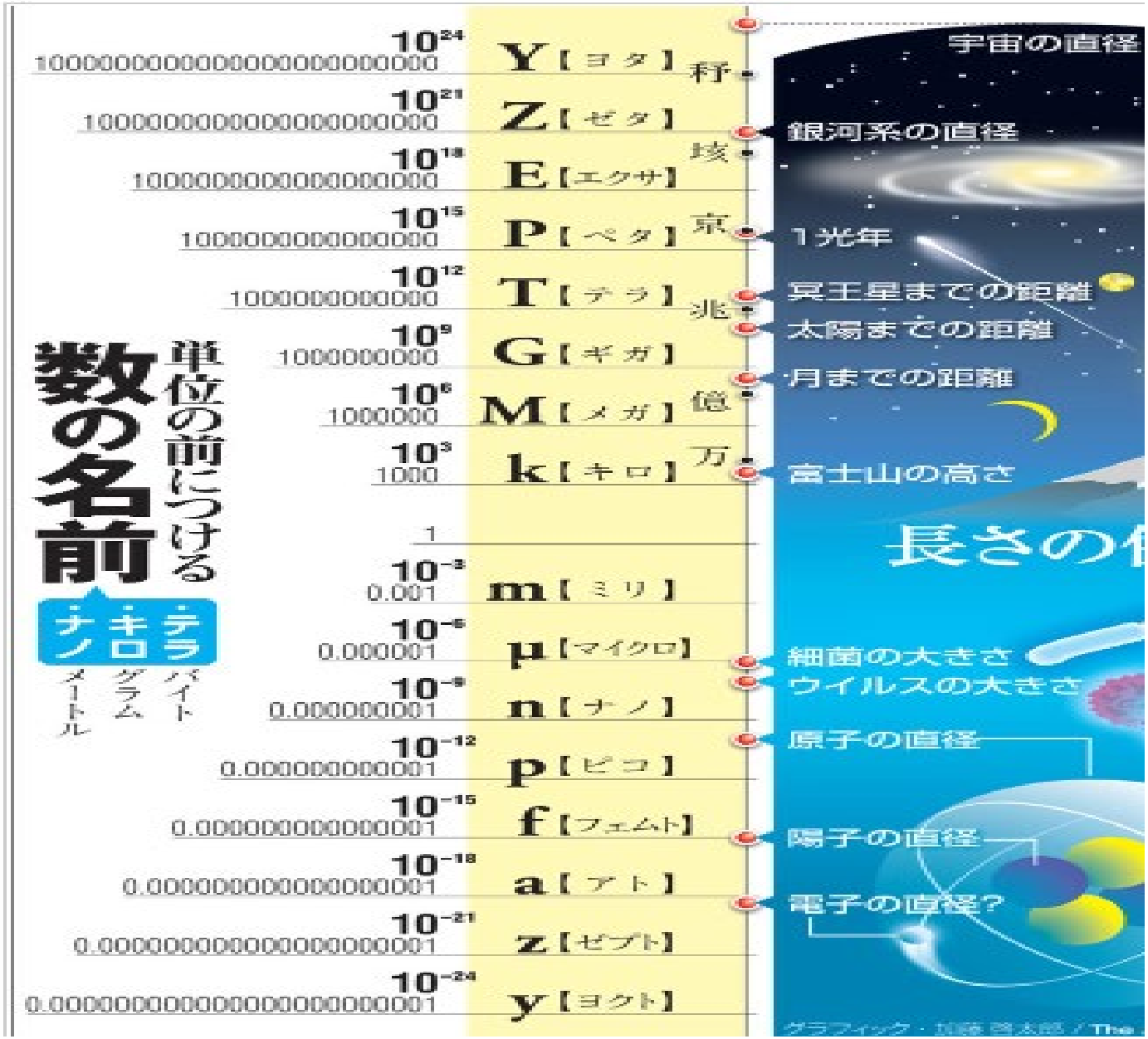
			SITE	COUNTRY	CORES	RMAX PFLOP/S	POWER MW
1	Frontier	HPE Cray EX235a, AMD Opt 3rd Gen EPYC (64C 2GHz), AMD Instinct MI250X, Slingshot-11	DOE/SC/ORNL	USA	8,699,904	1,194.0	22.7
2	Fugaku	Fujitsu A64FX (48C, 2.2GHz), Tofu Interconnect D	RIKEN R-CCS	Japan	7,630,848	442.0	29.9
3	LUMI	HPE Cray EX235a, AMD Opt 3rd Gen EPYC (64C 2GHz), AMD Instinct MI250X, Slingshot-11	EuroHPC/CSC	Finland	2,220,288	309.0	6.01
4	Leonardo	Atos Bullsequana intelXeon (32C, 2.6 GHz), NVIDIA A100 quad-rail NVIDIA HDR100 Infiniband	EuroHPC/CINEC	Italy	1,824,768	238.7	7.40
5	Summit	IBM POWER9 (22C, 3.07GHz), NVIDIA Volta GV100 (80C), Dual-Rail Mellanox EDR Infiniband	DOE/SC/ORNL	USA	2,414,592	148.6	10.1

No. 1 June 2022-23 870万プロセッサ, 22.7MW
Frontier - HPE Cray EX235a, 8,699,904 total cores, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X accelerators,
HPE Slingshot-11 interconnect 168京回演算/秒
Oak Ridge National Laboratory (ORNL) , USA
Rmax: 1.19 (ExaFlop/s), Rpeak 1.68(ExaFlop/s)
HPCG:14,054[TFlop/s]

朝日新聞 DIGITAL

http://www.asahi.com/science/intro/TKY201203070434.html

サイエンス 写真-図版



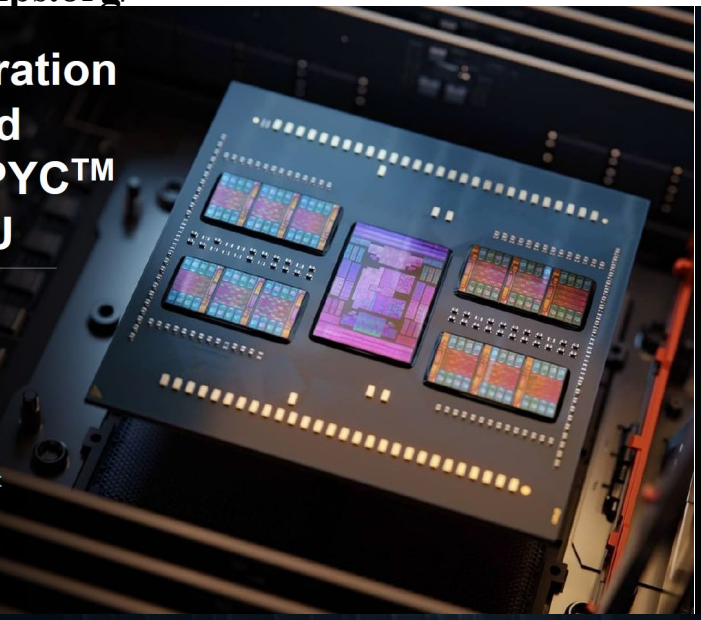
https://en.wikipedia.org/wiki/5_nm_process

MOSFET scaling (process nodes)

- 10 µm – 1971
- 6 µm – 1974
- 3 µm – 1977
- 1.5 µm – 1981
- 1 µm – 1984
- 800 nm – 1987
- 600 nm – 1990
- 350 nm – 1993
- 250 nm – 1996
- 180 nm – 1999
- 130 nm – 2001
- 90 nm – 2003
- 65 nm – 2005
- 45 nm – 2007
- 32 nm – 2009
- 22 nm – 2012
- 14 nm – 2014
- 10 nm – 2016
- 7 nm – 2018
- 5 nm – 2020
- Future 3 nm ~ 2022
- 2 nm ~ 2023

https://hc2023.hotchips.org/

AMD Next Generation "Zen 4" Core and 4th Gen AMD EPYC™ 9004 Server CPU

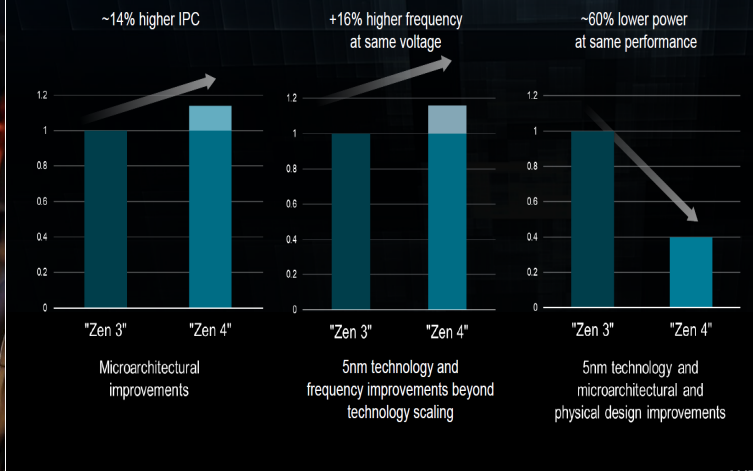


Kai Troester
AMD Fellow Silicon Design Engineer
"Zen 4" Lead Architect

Ravi Bhargava
AMD Senior Fellow
"Zen 4" EPYC™ Performance Architect

Hot Chips 2023

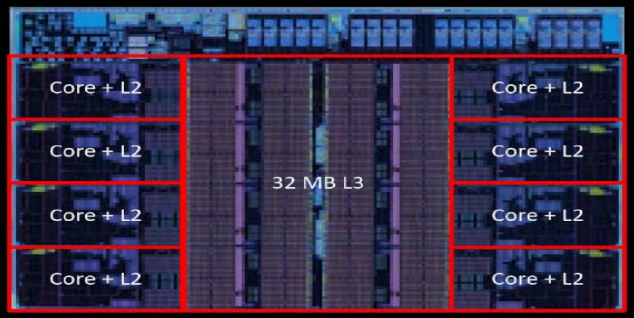
"Zen 4" Improves on Successful "Zen 3" Microarchitecture



"Zen 4c" Doubles Cores Per Compute Die

5nm

"Zen 4" CCD



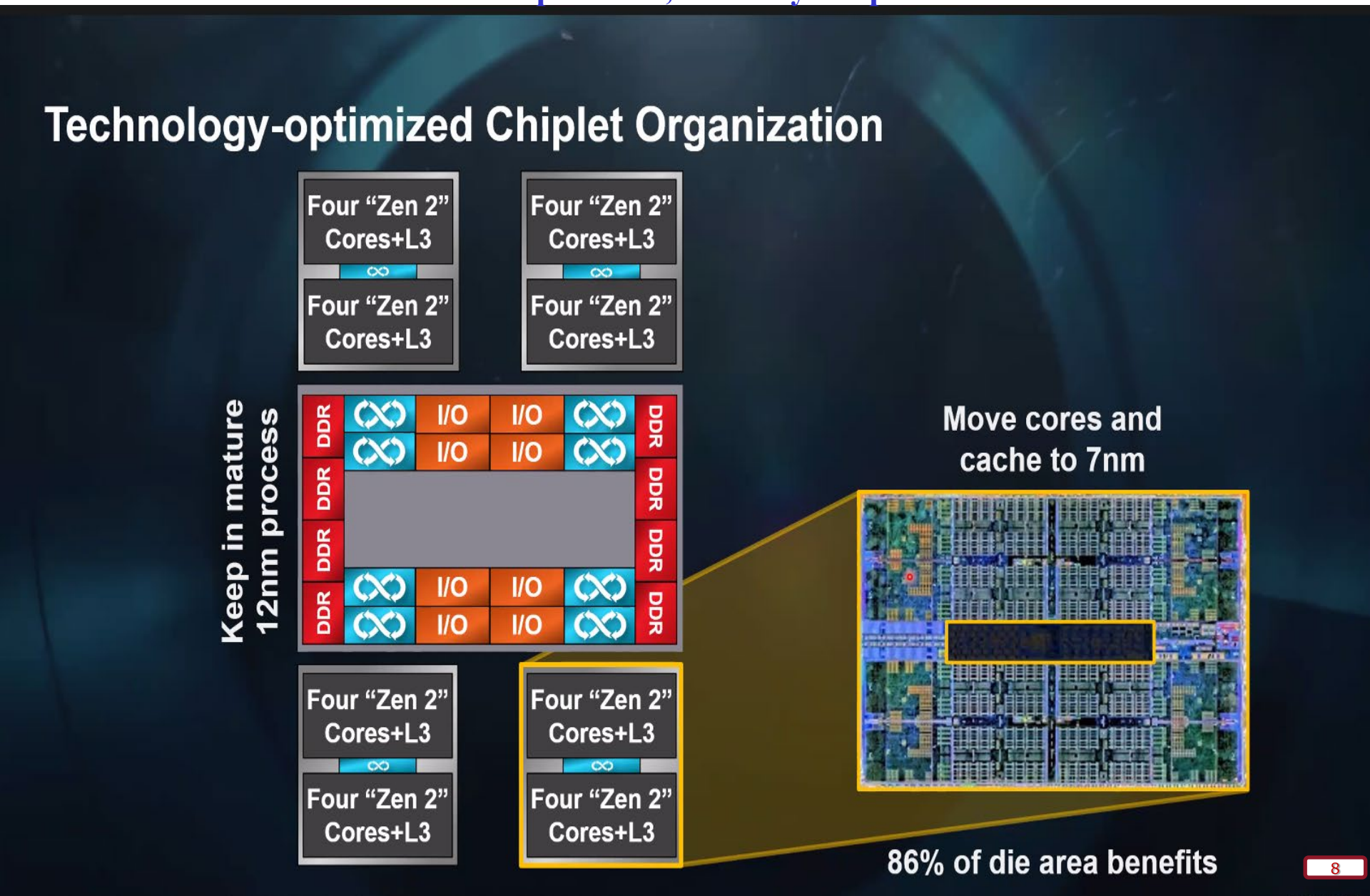
"Zen 4c" CCD

Cores	8	16
L2 cache/core	1 MB	1 MB
L3 cache/core	4 MB	2 MB

AMD

AMD Chiplet for 64 cores: Zen2

Processor Chiplet 7nm, Memory Chiplet: 12nm



AMD

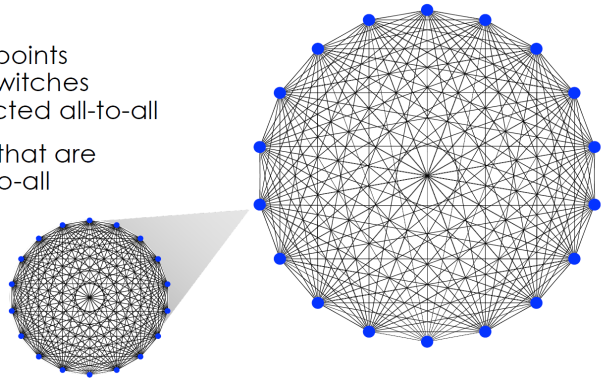
https://olcf.ornl.gov/wp-content/uploads/Frontiers-Architecture-Frontier-Training-Series-final.pdf

What is a Dragonfly topology?

- A set of groups that are connected all-to-all
  - Every group has one or more links to every other group

Another view of a Dragonfly Topology

- A group of endpoints connected to switches that are connected all-to-all
- A set of groups that are connected all-to-all



OAK RIDGE National Laboratory | LEADERSHIP COMPUTING FACILITY

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Technology-Driven, Highly-Scalable Dragonfly Topology*

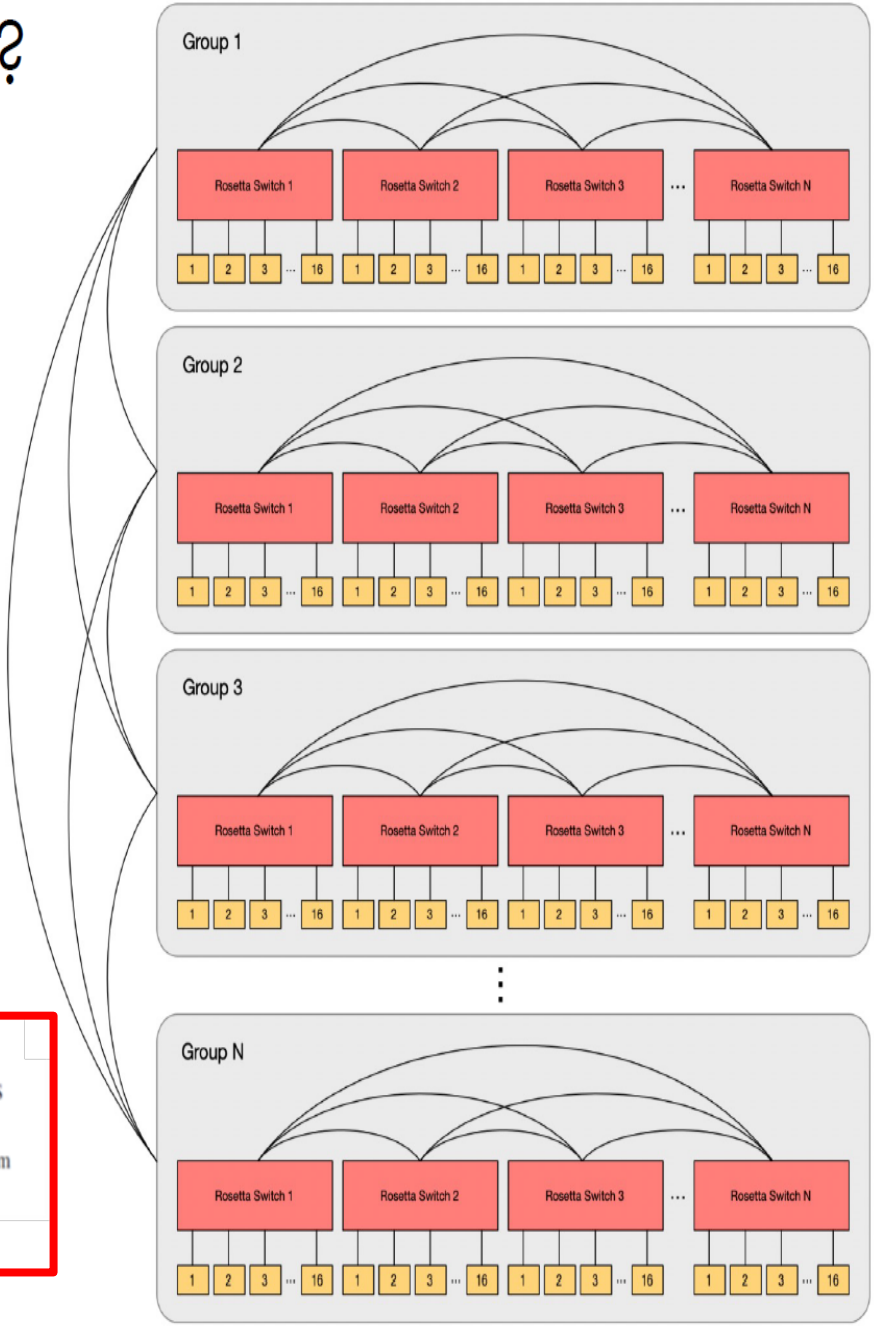
John Kim
Northwestern University
Evanston, IL 60208
jjk12@northwestern.edu

William J. Dally
Stanford University
Stanford, CA 94305
dally@stanford.edu

Steve Scott
Cray Inc.
Chippewa Falls, WI 54729
sscott@cray.com

Dennis Abts
Google Inc.
dabts@google.com

IEEE computer society
1063-6897/08 $25.00 © 2008 IEEE
DOI 10.1109/ISCA.2008.19



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The List.

MAY 2024

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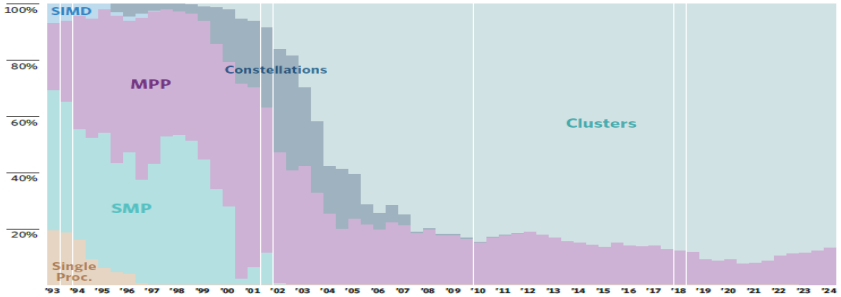
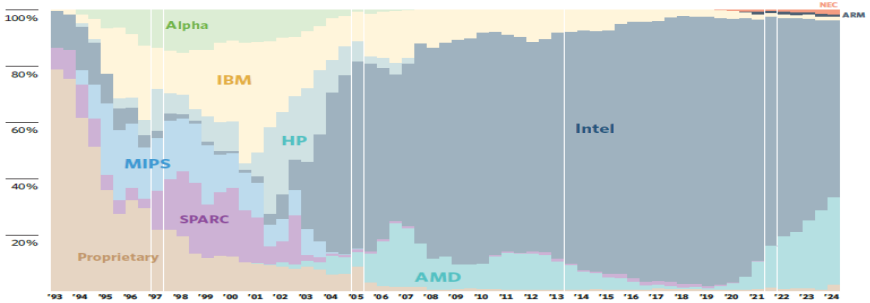
			SITE	COUNTRY	CORES	RMAX PFLOP/S	POWER MW
1	**Frontier**	HPE Cray EX235a, AMD Opt 3rd Gen EPYC (64C 2GHz), AMD Instinct MI250X, Slingshot-11	DOE/SC/ORNL	USA	8,699,904	1,206.0	22.7
2	**Aurora**	HPE Cray EX - Intel Exascale Compute Blade, Xeon CPU Max 9470 (52C 2.4GHz), Intel Data Center GPU Max, Slingshot-11	DOE/SC/ANL	USA	9,264,128	1,012.0	38.7
3	**Eagle**	Microsoft NDv5, Xeon Platinum 8480C (48C 2GHz), NVIDIA H100, NVIDIA Infiniband NDR	Microsoft Azure	USA	1,123,200	561.2	
4	**Fugaku**	Fujitsu A64FX (48C, 2.2GHz), Tofu Interconnect D	RIKEN R-CCS	Japan	7,630,848	442.0	29.9
5	**LUMI**	HPE Cray EX235a, AMD Opt 3rd Gen EPYC (64C 2GHz), AMD Instinct MI250X, Slingshot-11	EuroHPC/CSC	Finland	2,220,288	379.7	6.01

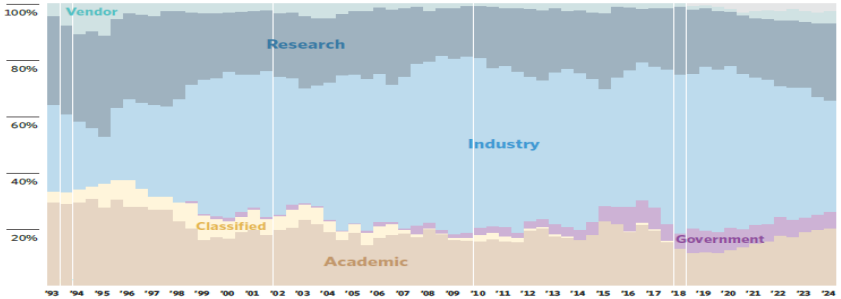
ARCHITECTURES



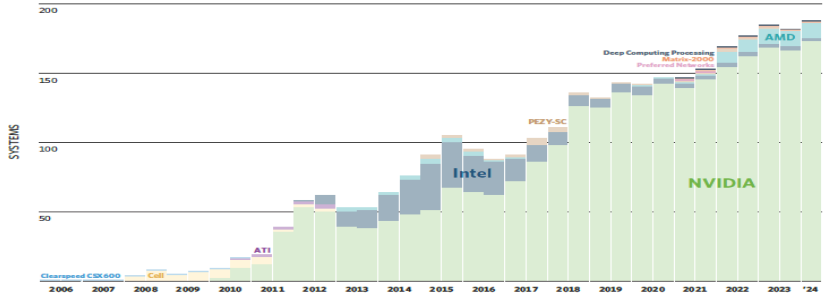
CHIP TECHNOLOGY



INSTALLATION TYPE



ACCELERATORS/CO-PROCESSORS



年200億個以上のプロセッサが生産

マルチコアプロセッサ：スマホ,タブレット,IoTデバイス,自動車制御,サーバ,スパコン等

例：ARM,IBM Power,Renesas RH850, Infineon,SPARC,RISC V

https://www.apple.com/jp/shop/buy-iphone

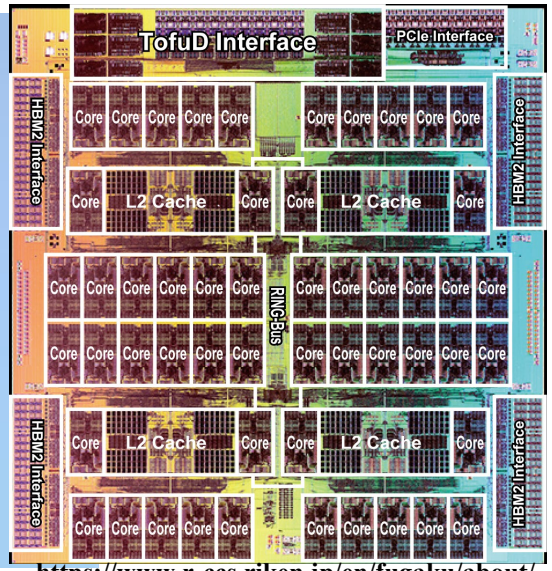
64-bit
iPhone 13
2021

Launched September 14, 2021
Designed by Apple Inc.
Common manufacturer(s)： TSMC
Max. CPU clock rate to 3.23 GHz in iPhone 13 Pro
Technology node: 5 nm
6 Cores: 2 “Avalanche“高性能コア & 4 ”Blizzard”省エネコア
Instruction set: A64, Transistors: 15 billion (15億個)
5 core GPU(s): Apple-designed GPU in iPhone 13

https://en.wikipedia.org/wiki/Apple_A15

理研富岳スーパーコンピュータ 2020年6月から2021年11月まで世界No.1

https://fugaku100kei.jp/fugaku/



https://www.r-ccs.riken.jp/en/fugaku/about/

RIKEN Center for Computational Science,
Fujitsu（arm based processor）
Cores:7,299,072； Memory:4,866,048GB；
Processor:A64FX 48Cores, 2.2GHz
Interconnect: Tofu interconnect D
Linpack (Rmax)415,530 TFlop/s;
Theoretical Peak (Rpeak): 513PFLOPS
HPCG [TFlop/s]13,366.4; Power: 28.3MW

48コア/チップ, 2.2GHz, 7 nm FinFET,
約7百30万コア, 28MW
理論最高性能:51京回浮動小数点演算/秒,
2020年6月時点

https://japanese.engadget.com/arm-super-computer-fugaku-top-500-034015910.html

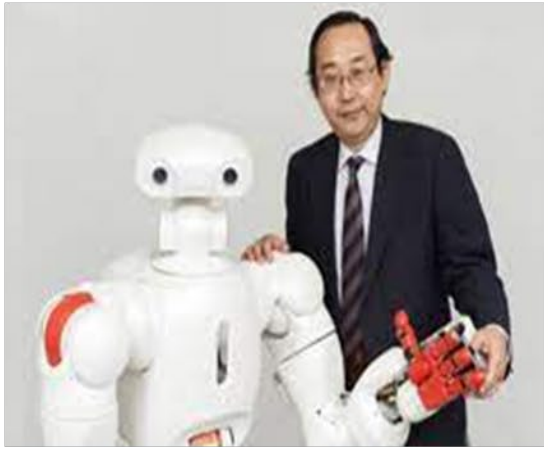
https://www8.cao.go.jp/cstp/english/moonshot/sub3_en.html

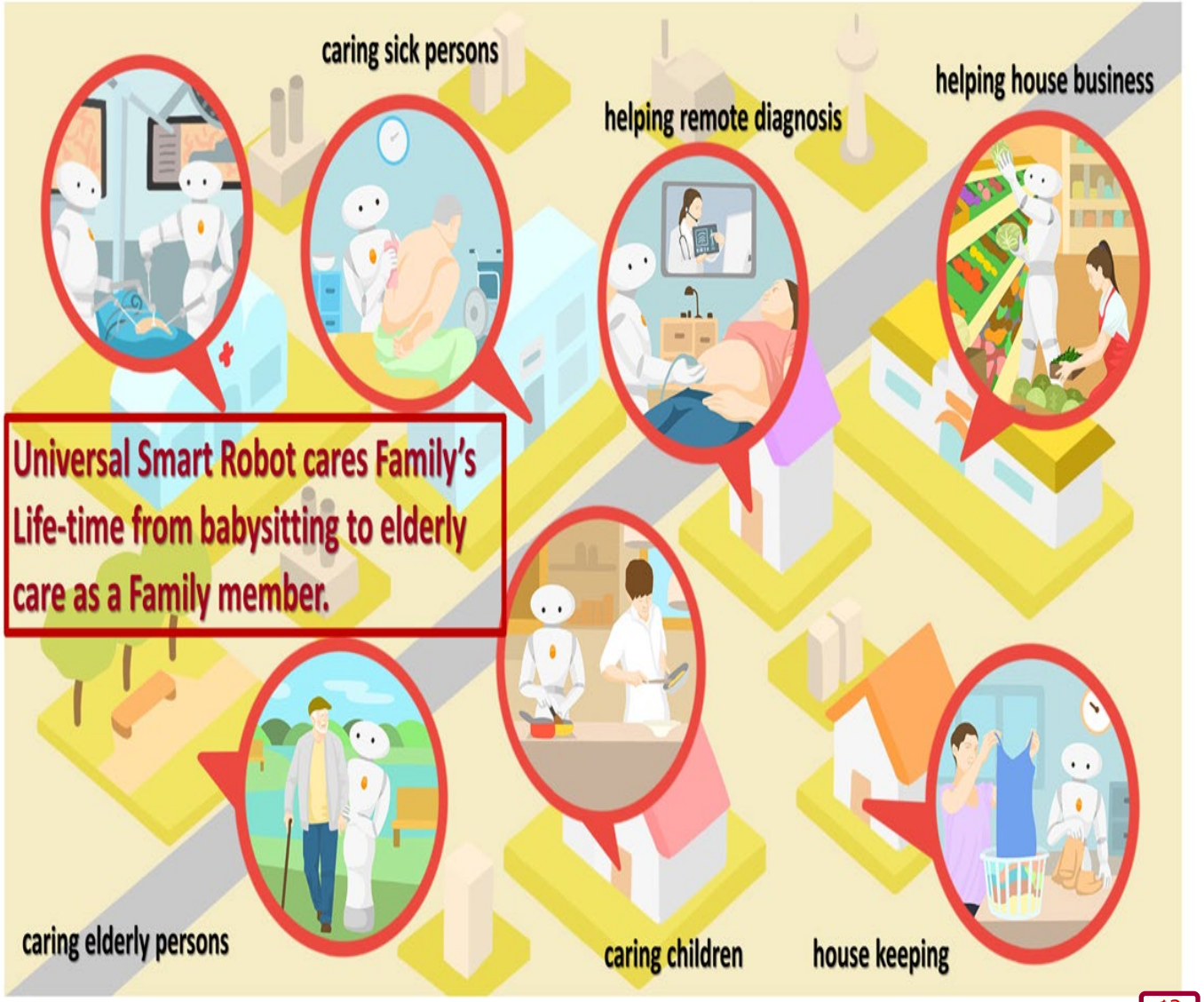
Cabinet Office

MOONSHOT
RESEARCH & DEVELOPMENT PROGRAM

AIREC (AI-driven Robot for Embrace and Care) Led by Prof. Sugano

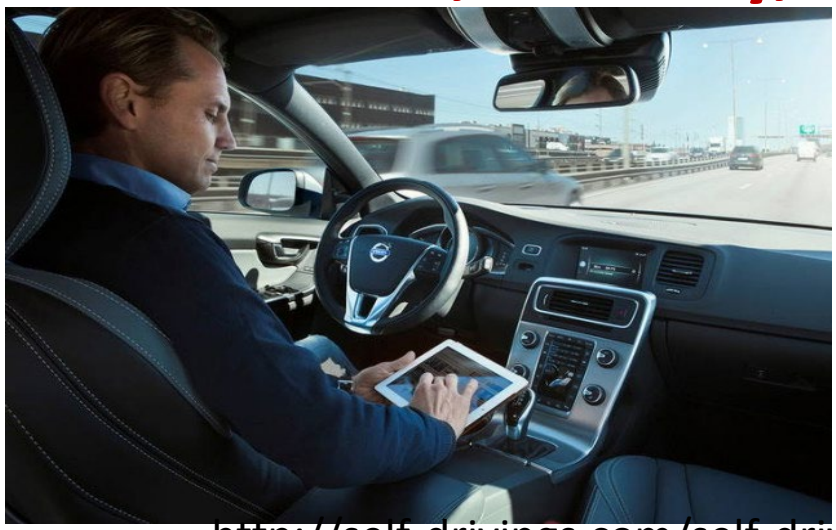
Supported by Japanese Government "Moonshot" Project from 2020





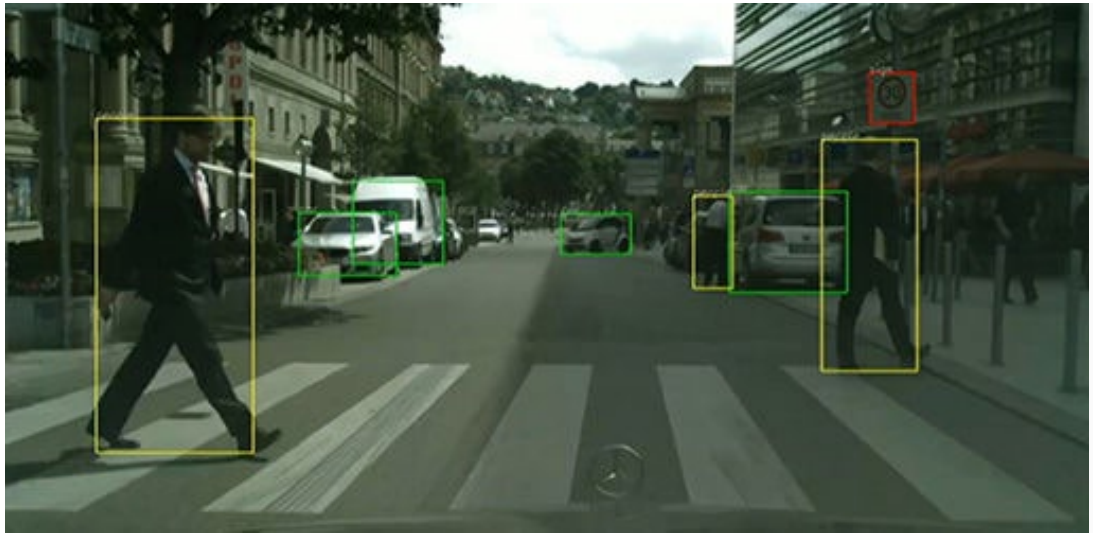
Self Driving Cars (自動運転)

Connected, Security, Big Data, Traffic Cloud



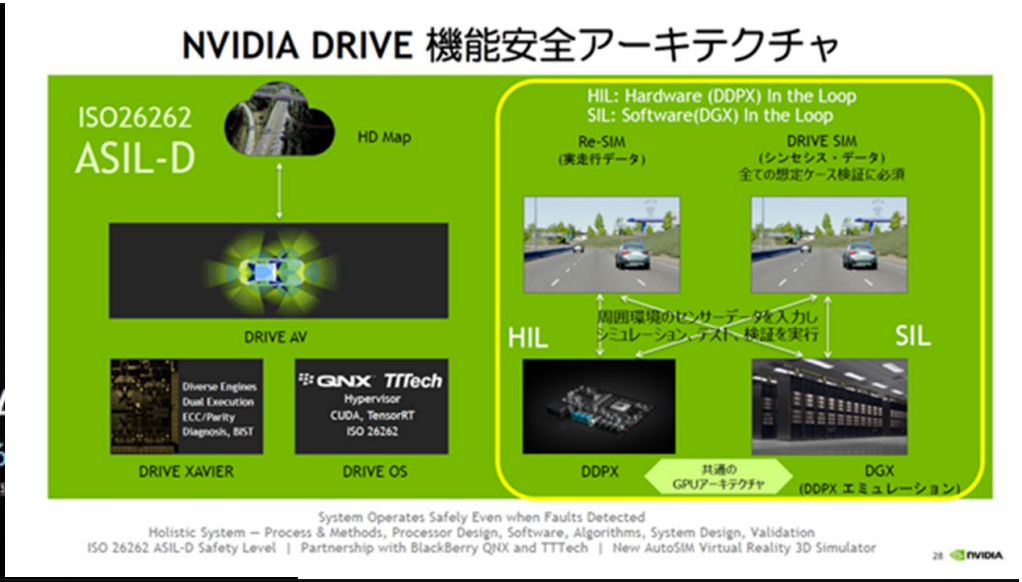
http://self-drivings.com/self-driving-cars-updated-market-analysis/

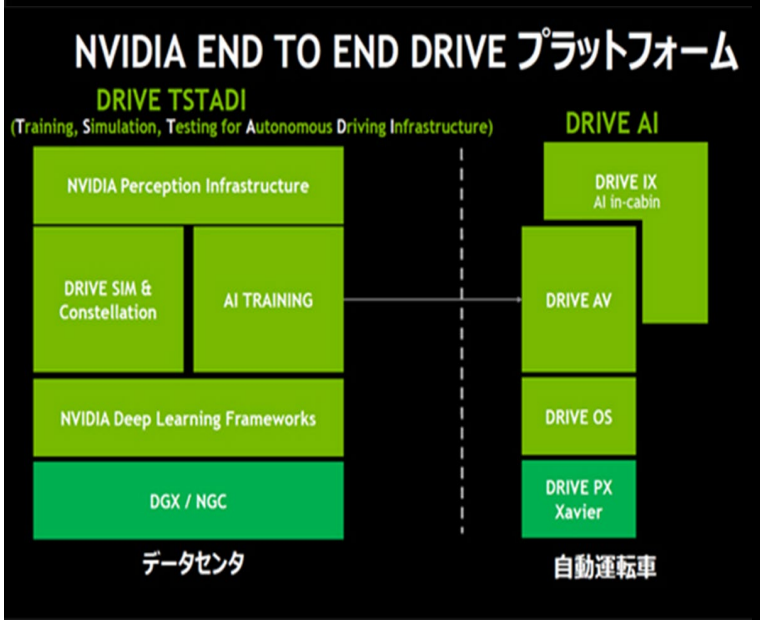
Deep Leaning （多層ニューラルネット）により画像認識

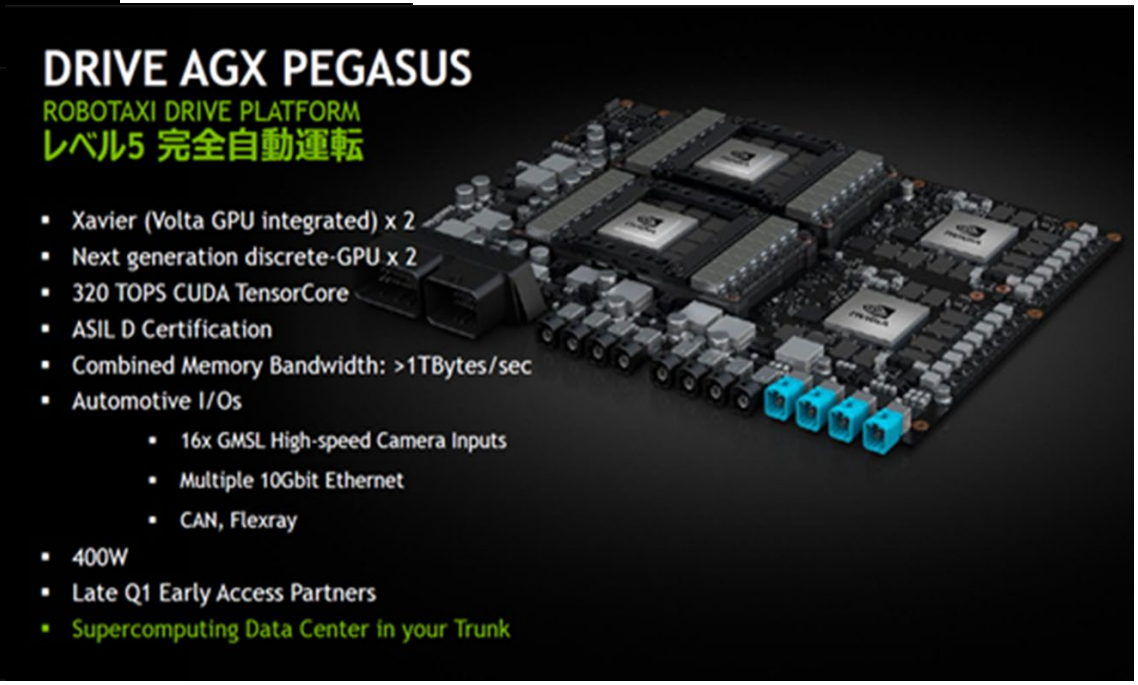


http://www.digitalartsonline.co.uk/news/creative-hardware/nvidias-water-cooled-supercomputer-helps-cars-drive-themselves/

NVIDIA自動車用アクセラレータ　DRIVE PX XAVIER







https://news.mynavi.jp/article/20181003-700546/

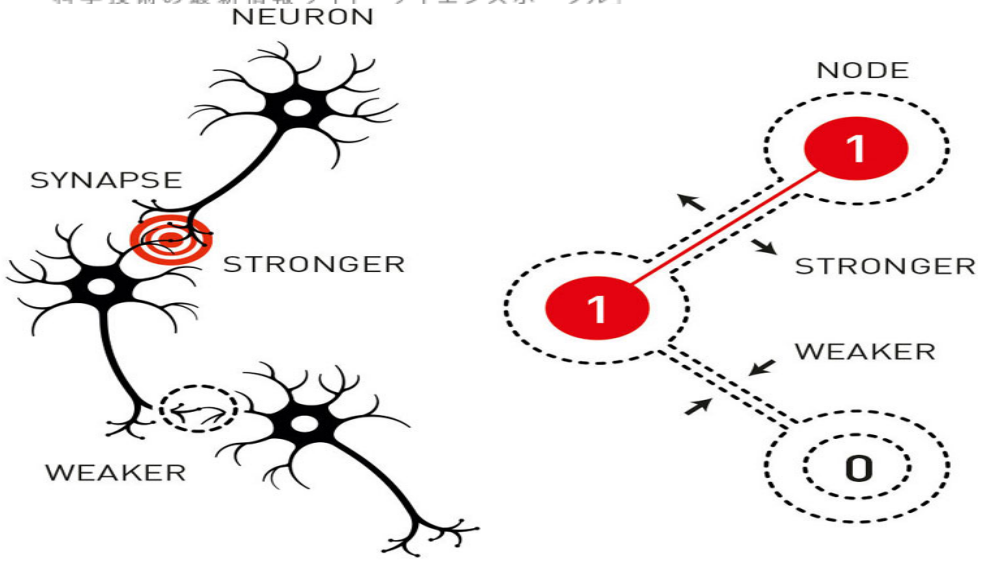
ノーベル物理学賞、機械学習の基礎を築いた米国とカナダの2氏に

2024.10.08

Science Portal
科学技術の最新情報サイト「サイエンスポータル」

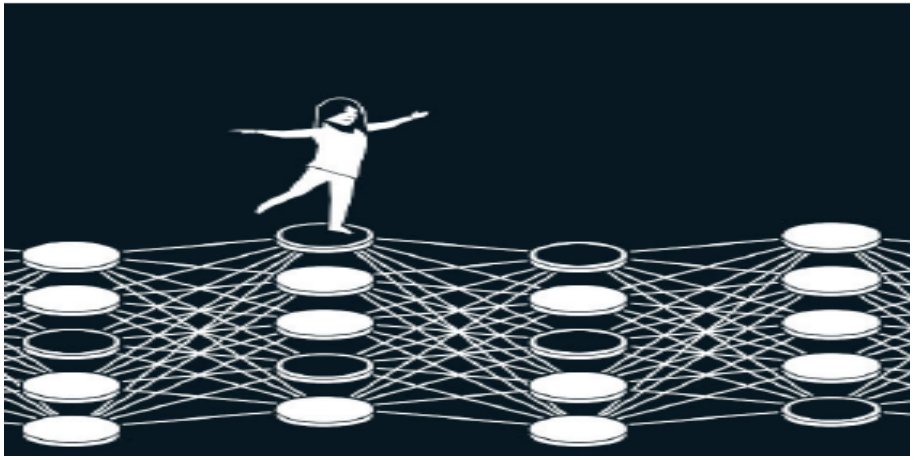
スウェーデン王立科学アカデミーは8日、2024年のノーベル物理学賞を、人工ニューラルネット（神経回路網）による機械学習の分野を切り開いた2氏に授与すると発表した。受賞が決まったのは米プリンストン大学のジョン・ホップフィールド名誉教授（91）と、カナダ・トロント大学のジェフリー・ヒントン名誉教授（76）。2021年の真鍋淑郎氏（米国籍）以来となる、日本人の物理学賞受賞はならなかった。

ノーベル物理学賞の受賞が決まったホップフィールド（左）、ヒントン両氏のイラスト（ニクラス・エルメヘド氏、ノーベル財団提供）



脳の神経細胞はシナプスを介してネットワークをつくり、学習によってその結合の強さが変わる（左）。人工のニューラルネットはその仕組みをまね、「1」「0」の信号を受けてノードの強さが変わる（ノーベル財団提供）

人工知能（AI）草創期の1960年代には、コンピューターが認識できるように知識をデータ化した。これに対し、人間などの脳の神経細胞の働きをモデルにした方法でデータを処理するのが、人工ニューラルネットの手法だ。神経細胞は「ノード」（結び目、点）で表され、シナプスのような接続を介して影響し合う。80年代以降、人工ニューラルネットに関する重要な研究が進展してきた。



人工ニューラルネットのイメージ（ノーベル財団提供）

https://scienceportal.jst.go.jp/newsflash/20241008_n01/

ACM チューリング賞

A.M. TURING CENTENARY CELEBRATION WEBCAST

コンピュータ分野のノーベル賞

Prof. Yoshua Bengio
モントリオール大学
2024年3月7日
大川賞授賞式
Okawa Prize
Alphabet(Google親会社)会長

Turing Award › Winners

Jeffrey Ullman
2020 アルゴリズムと
プログラミング言語

Geoffrey Hinton
2018 AI
ディープ・ラーニング

John L. Hennessy
2017 コンピュータ構成法
RISC:スマホ-スパコン

毎年生産される200億個以上の
プロセッサの99%がRISC

Alfred Aho
2020 アルゴリズムと
プログラミング言語

Yoshua Bengio
2018 AI
ディープ・ラーニング

Tim Berners-Lee
2016 World Wide Web

ディズニー・アニメーション・
スタジオ&ピクサーの元社長

Edwin Catmull アニメーションと
3Dグラフィックス
2019
トイ・ストーリー,モンスターズ・インク

Yann LeCun
2018 AI
ディープ・ラーニング

Whitfield Diffie
2015 公開鍵暗号

Pat Hanrahan
2019 アニメーションと
3Dグラフィックス

カリフォルニア大バークレー
名誉教授, ACM元会長

David A Patterson
2017 コンピュータ構成法
RISC:スマホ-スパコン

Martin Hellman
2015 公開鍵暗号

毎年生産される32bit,64bitプロセッサの99%はRISC

https://www.acm.org/hennessy-patterson-turing-lecture

https://dl.acm.org/cms/attachment/164b78fa-de5b-4d7e-bb28-17084e83e06a/f6.jpg

RISCはスマホ,IoT,自動車制御からサーバ,スパコン等まで広く使用されている

例 : ARM,IBM Power,Renesas RH850, Infineon,SPARC,RISC V

64-bit iPhone 13 2021

https://www.apple.com/jp/shop/buy-iphone

IBM Watson

http://watson2016.com/

Renesas 自動車制御

https://www.renesas.com/

理研富岳

https://fugaku100kei.jp/fugaku/

Amazon buys nuclear-powered data center from Talen

Thu, Mar 7, 2024, 10:01PM | Nuclear News

Susquehanna nuclear plant in Salem Township, Penn., along with the data center in foreground. (Photo: Talen Energy)

Talen Energy announced its sale of a 960-megawatt data center campus to cloud service provider Amazon Web Services (AWS), a subsidiary of Amazon, for $650 million.

The data center, Cumulus Data Assets, sits on a 1,200-acre campus in Pennsylvania and is directly powered by the adjacent Susquehanna Steam Electric Station, which generates 2.5 gigawatts of power.

早稲田大学博士在学中及び学位取得直後の代表的国際論文

IEEE TRANSACTIONS ON COMPUTERS, VOL. C-33, NO. 11, NOVEMBER 1984 1023

Practical Multiprocessor Scheduling Algorithms for Efficient Parallel Processing

HIRONORI KASAHARA, MEMBER, IEEE, AND SEINOSUKE NARITA, SENIOR MEMBER, IEEE

Courtesy of dexchao - Fotolia.com

104 IEEE JOURNAL OF ROBOTICS AND AUTOMATION, VOL. RA-1, NO. 2, JUNE 1985

Parallel Processing of Robot-Arm Control Computation on a Multimicroprocessor System

HIRONORI KASAHARA MEMBER, IEEE, AND SEINOSUKE NARITA, SENIOR MEMBER, IEEE

2nd International Conference on Superecomputing
Santa Clara, CA, USA May 3-8,1987

A PARALLEL PROCESSING SCHEME FOR THE SOLUTION OF SPARSE LINEAR EQUATIONS USING STATIC OPTIMAL-MULTIPROCESSOR-SCHEDULING ALGORITHMS

H.Kasahara*, T.Fujii*, H.Nakayama*, S.Narita*, and Leon O.Chua**

* Dept. of Electrical Eng., Waseda University, Tokyo, 160, Japan
** Dept. of Electrical Eng. and Computer Sciences, University of California, Berkeley, CA 94720, U.S.A.

PARALLEL PROCESSING OF ROBOT MOTION SIMULATION

H. Kasahara, H. Fujii and M. Iwata

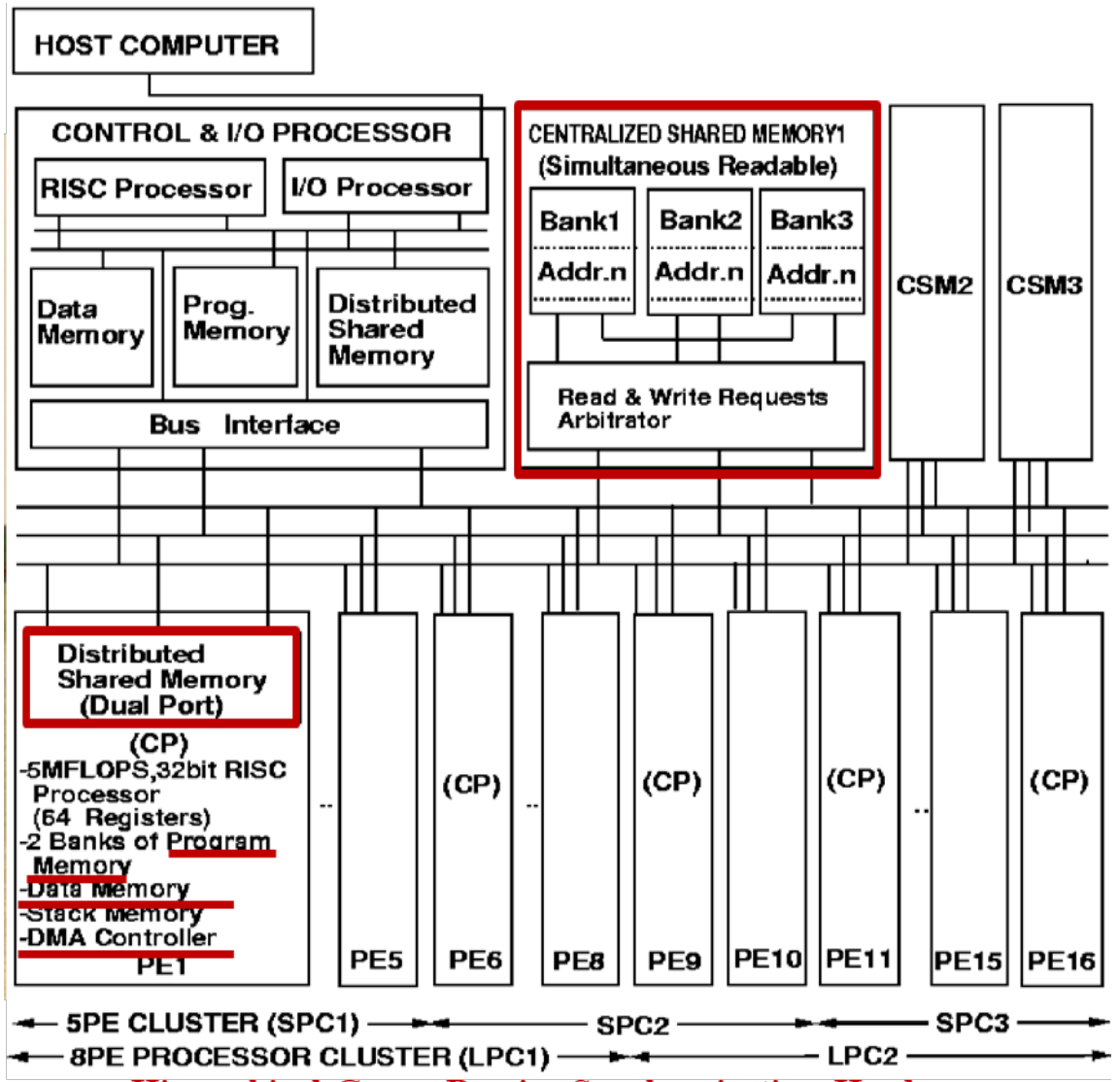
Department of Electrical Engineering, Waseda University, 3–4–1 Ohkubo Shinjuku-ku, Tokyo 160, Japan

The First Compiler Codesigned Multiprocessor

OSCAR (Optimally Scheduled Advanced Multiprocessor) in 1987

AMD29325 32-bit Floating-point unit

H. Kasahara, "OSCAR Fortran Multigrain Compiler", Stanford University, Hosted by Professor John L. Hennessy and Professor Monica Lam, May. 15. 1995.

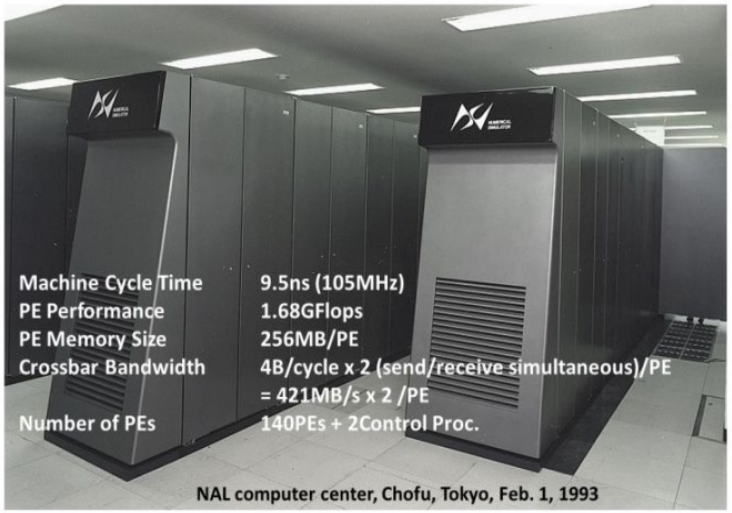


AMD29325 32-bit Floating-point unit

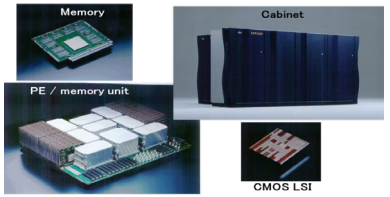
Hierarchical Group Barrier Synchronization Hardware

笠原博徳が設計・開発に参加した3つの世界No.1 スーパーコンピュータ “NWT：数値風洞”, “Earth Simulator：地球シミュレータ”, and “K：京”

日本スパコンの父
三好甫氏
航空宇宙技術研究所
早稲田大学数学卒
Father of Japanese Supercomputer
Mr. Hajime Miyoshi,
Waseda Alumnus,
Leader of NWT,
Earth Simulator

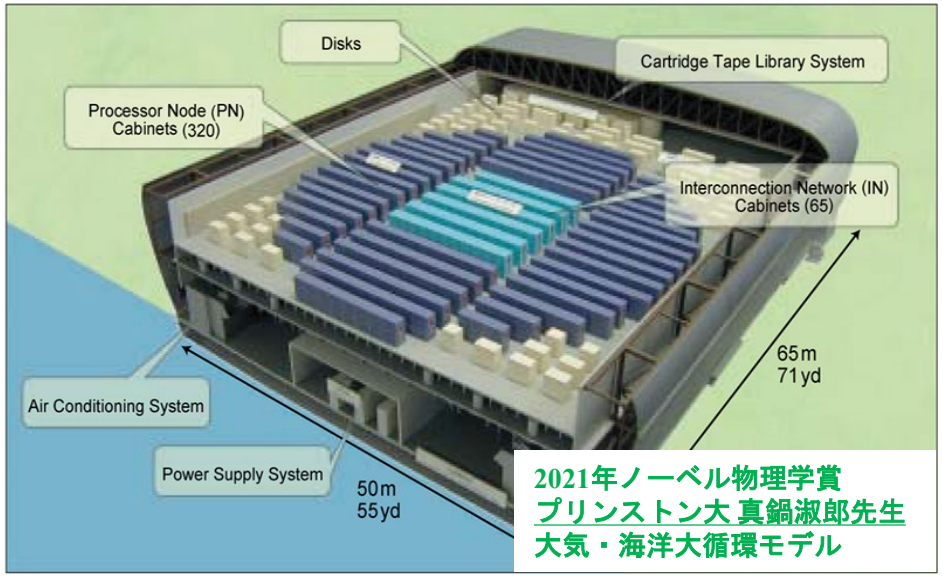


NWT：数値風洞
(Numerical Wind Tunnel) ,
1993,1.68GFLOPS
<Fujitsu VPP 500, 5000>



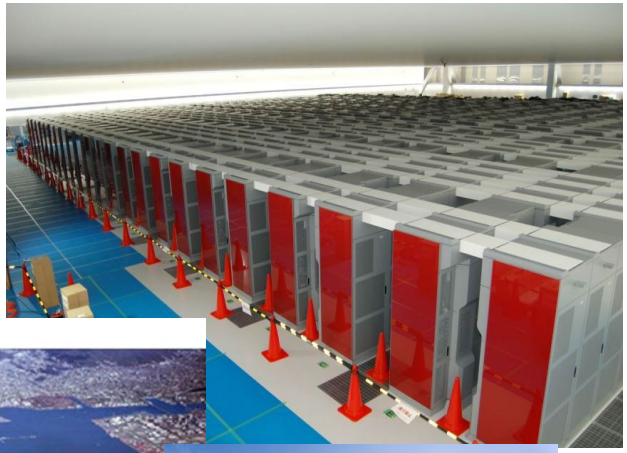
Earth Simulator,
2002

40 TFLOPS Peak ($40*10^{12}$)
35.6 TFLOPS Linpack
3.2MW



2021年ノーベル物理学賞
プリンストン大 真鍋淑郎先生
大気・海洋大循環モデル

K「京」,
2011
10PFLOPS
11.3MW

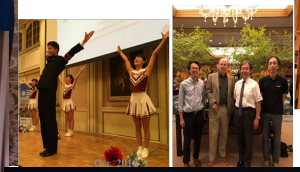


IEEE Computer Society

The first President from outside North America in 72 years history of IEEE CS

Bjarne Stroustrup: Morgan Stanley & Columbia Univ.
2018 IEEE Computer Society Computer Pioneer Award
IEEE COMPSAC2018 Keynote & Award Ceremony

July 26, 2018, Keynote, Hitotsubashi Hall



July 25, 2018 Award Ceremony Rihga Royal Hotel Tokyo

215 International Conferences

12 Magazines

35 Journals

47 Total Publications

847,000+ Articles in CSDL

6 New Standards

230 Active Standards

IEEE754, 802

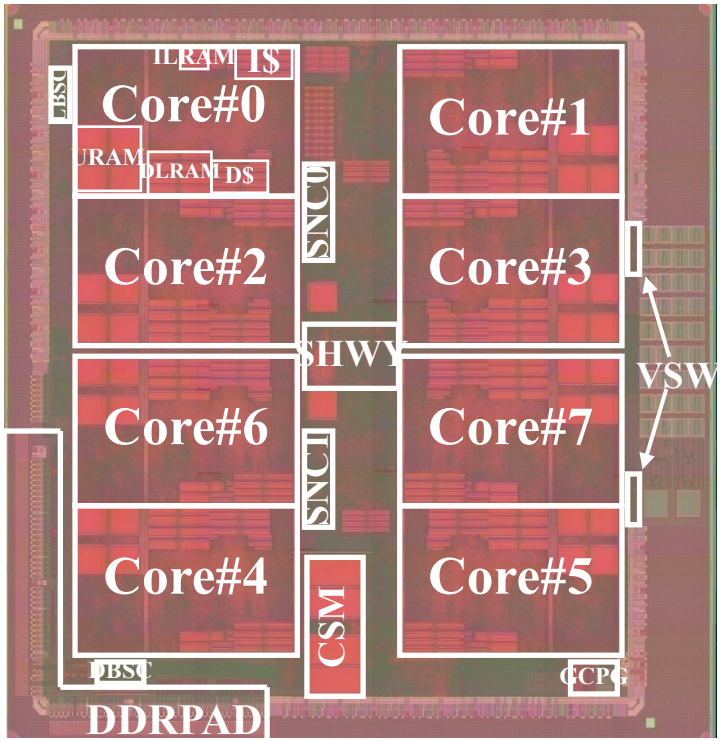
ACM/IEEE SC (SuperComputing) 19, Denver, Nov.17-22, 2019

Cornel Univ. Prof. Steven Squyres: Mars Exploration、CalTech. Dr. Katie Bouman: Visualization of Black Hole

ムーアの法則の終焉

ムーアの法則(Moore's law): インテル創業者の一人であるゴードン・ムーア(Gordon E. Moore: IEEE Computer Pioneer Award)が、1965年の論文で提唱した「半導体の集積率は18か月で2倍になる」という経験則。

コンピュータの高性能化と低消費電力化にはマルチコアが必須



IEEE ISSCC08: Paper No. 4.5, M.ITO, … and H. Kasahara, "An 8640 MIPS SoC with Independent Power-off Control of 8 CPUs and 8 RAMs by an Automatic Parallelizing Compiler"

$$\text{Power} \propto \text{Frequency} * \text{Voltage}^2$$

$$(\text{Voltage} \propto \text{Frequency})$$

$$\text{Power} \propto \text{Frequency}^3$$

周波数 Frequency を1/4にすると
(Ex. 4GHz→1GHz),
消費電力は 1/64に削減
性能は 1/4に低下 .

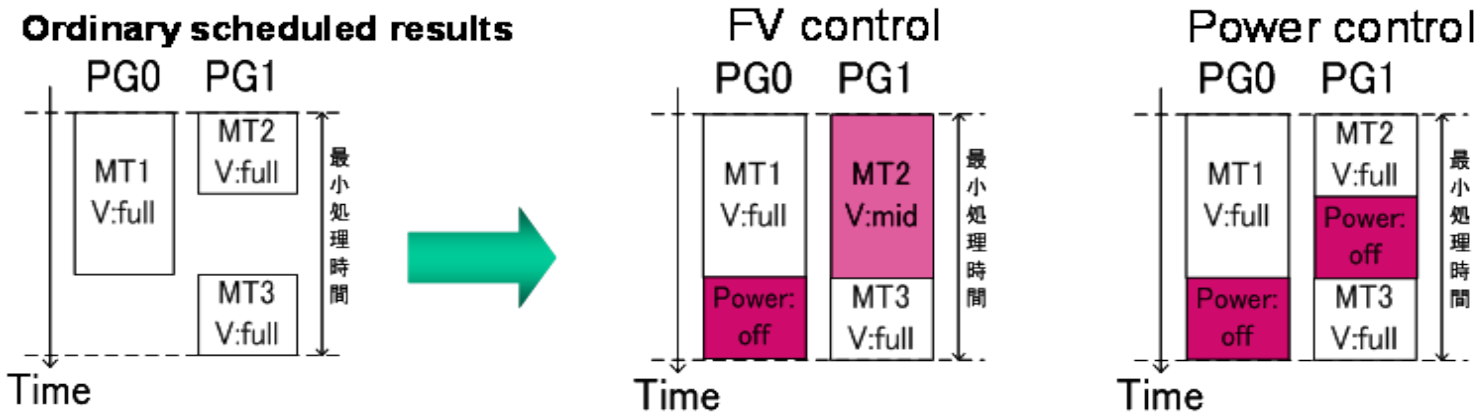
<マルチコア>

8cores をチップに集積すると,
電力は 依然1/8で性能 は2 倍向上

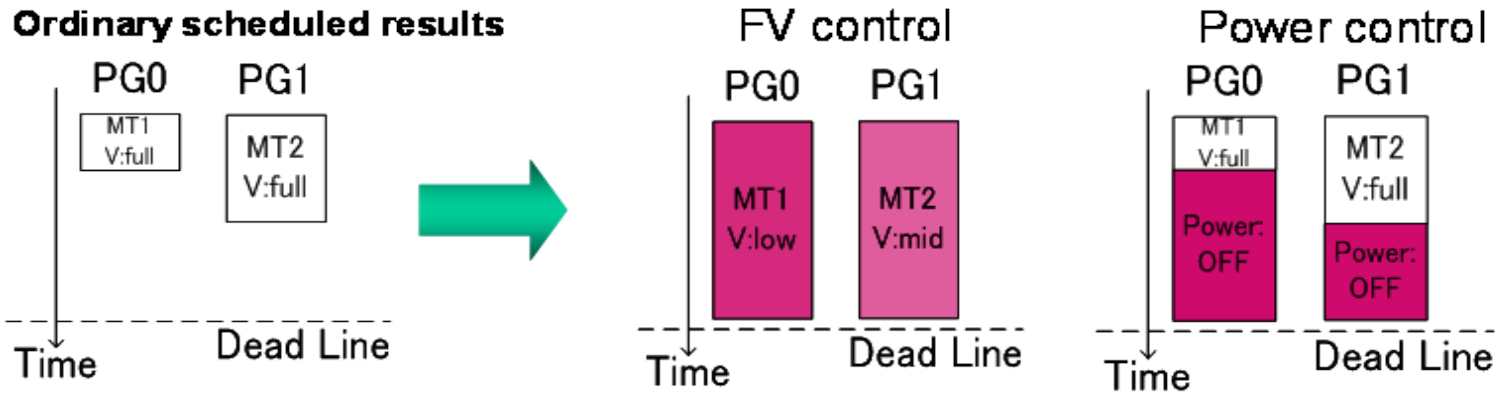
Power Reduction by Power Supply, Clock Frequency and Voltage Control by OSCAR Compiler

Frequency and Voltage (DVFS), Clock and Power gating of each cores are scheduled considering the task schedule since the dynamic power proportional to the cube of F (F^3) and the leakage power (the static power) can be reduced by the power gating (power off).

- **Shortest execution time mode**



- Realtime processing mode with dead line constraints



In this Fig. Frequency Full, Mid, Low

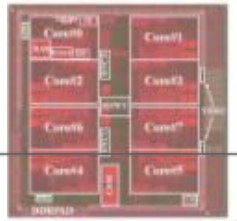
Power OFF: Power Gating

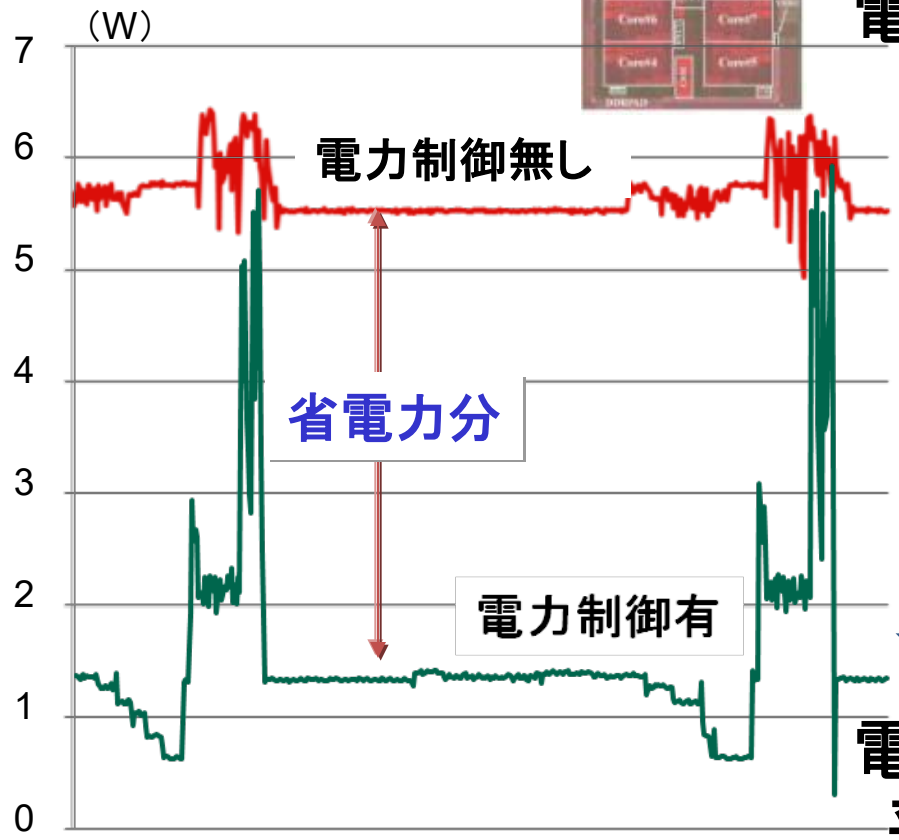
太陽光電力で動作する情報機器

コンピュータの消費電力をHW&SW協調で低減。電源喪失時でも動作することが可能。

リアルタイムMPEG2デコードを、8コアホモジニアス
マルチコアRP2上で、消費電力1/4に削減

世界唯一の差別化技術



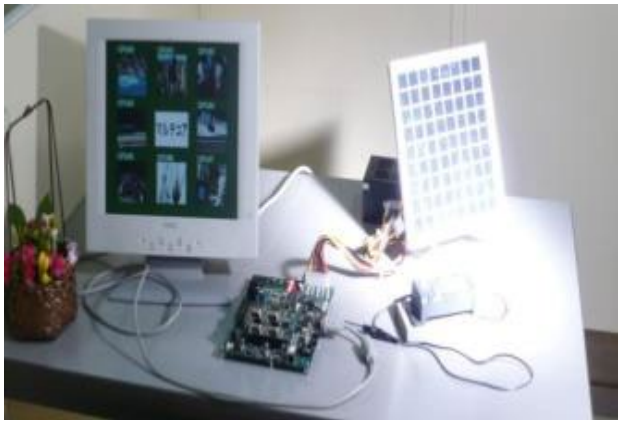


電力制御無し
平均電力
5.73 [W]

電力を
ソフトで
1/4に
削減

電力制御有
平均電力
1.52 [W]

周波数/電圧・電源遮断制御



太陽電池で駆動可

総合科学技術会議（平成20年4月10日）での NEDOリアルタイム情報家電用マルチコアチップ（笠原リーダー）・デモの様子

http://www8.cao.go.jp/cstp/gaiyo/honkaigi/74index.html

第74回総合科学技術会議【平成20年4月10日】

第74回総合科学技術会議の様子(1)

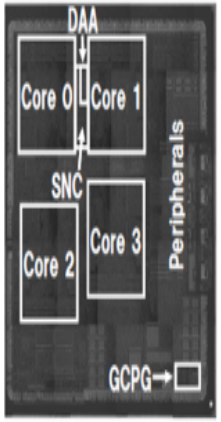
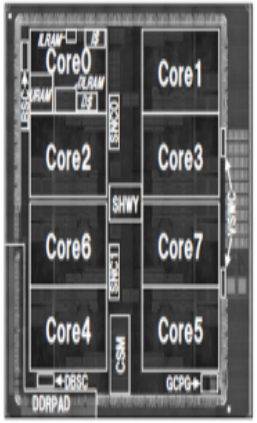
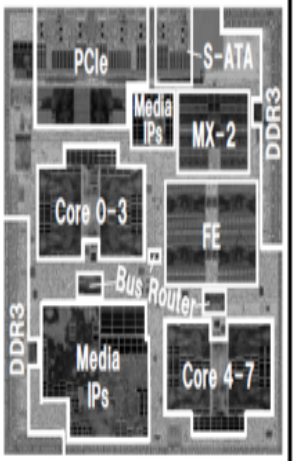
第74回総合科学技術会議の様子(2)

第74回総合科学技術会議の様子(3)

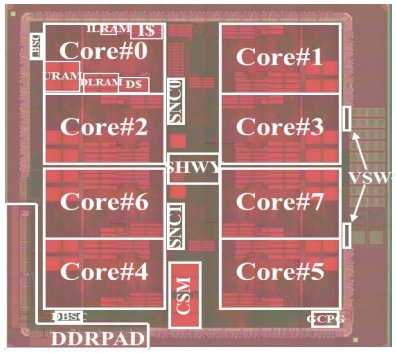
第74回総合科学技術会議の様子(4)

1985年よりコンパイラ（ソフト）・アーキテクチャ（ハード）協調設計マルチプロセッサの研究

4 core multicore RP1 (2007), 8 core multicore RP2 (2008) and 15 core Heterogeneous multicore RPX (2010) developed in NEDO Projects with Hitachi and Renesas

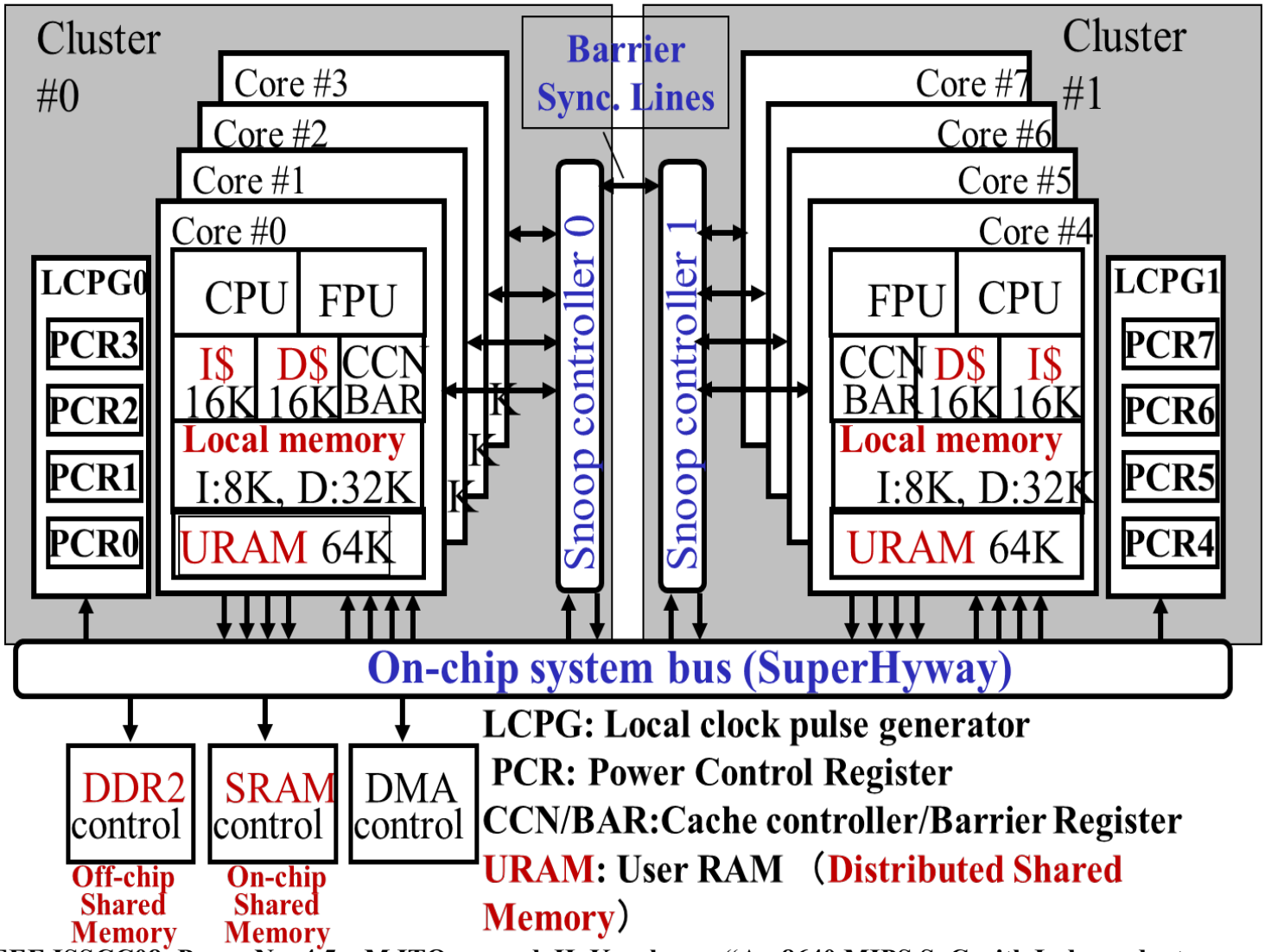
RP-1 (ISSCC2007 #5.3)	*RP-2* (ISSCC2008 #4.5)	*RP-X* (ISSCC2010 #5.3)
		
90nm, 8-layer, triple-Vth, CMOS	90nm, 8-layer, triple-Vth, CMOS	45nm, 8-layer, triple-Vth, CMOS
97.6 mm^2 (9.88 x 9.88 mm)	104.8 mm^2 (10.61 x 9.88 mm)	153.8 mm^2 (12.4 x 12.4 mm)
1.0V (internal), 1.8/3.3V (I/O)	1.0-1.4V (internal), 1.8/3.3V (I/O)	1.0-1.2V (internal), 1.2-3.3V (I/O)
600MHz ,4.32 GIPS,16.8 GFLOPS	600MHz , 8.64 GIPS, 33.6 GFLOPS	648MHz, 13.7GIPS, 115GOPS, 36.2GFLOPS
11.4 GOPS/W (32b換算)	18.3 GOPS/W (32b換算)	37.3 GOPS/W (32b換算)

経済産業省/NEDOプロジェクトにて、早稲田大学・日立製作所・ルネサスエレクトロニクスが共同開発した世界初のコンパイラ協調型グリーンマルチコア RP2 チップ



自動車、スマートホン、データセンター、サーバ等汎用的マルチコアチップとして開発。

各プロセッサ、メモリモジュール等の、周波数電圧制御、電力遮断制御をコンパイラが行うことを可能とした



IEEE ISSCC08: Paper No. 4.5, M.ITO, … and H. Kasahara, "An 8640 MIPS SoC with Independent Power-off Control of 8 CPUs and 8 RAMs by an Automatic Parallelizing Compiler"

世界をリードするマルチコア用コンパイラ技術

OSCARコンパイラの世界唯一技術

1.マルチグレイン並列化（全ての並列性を利用）

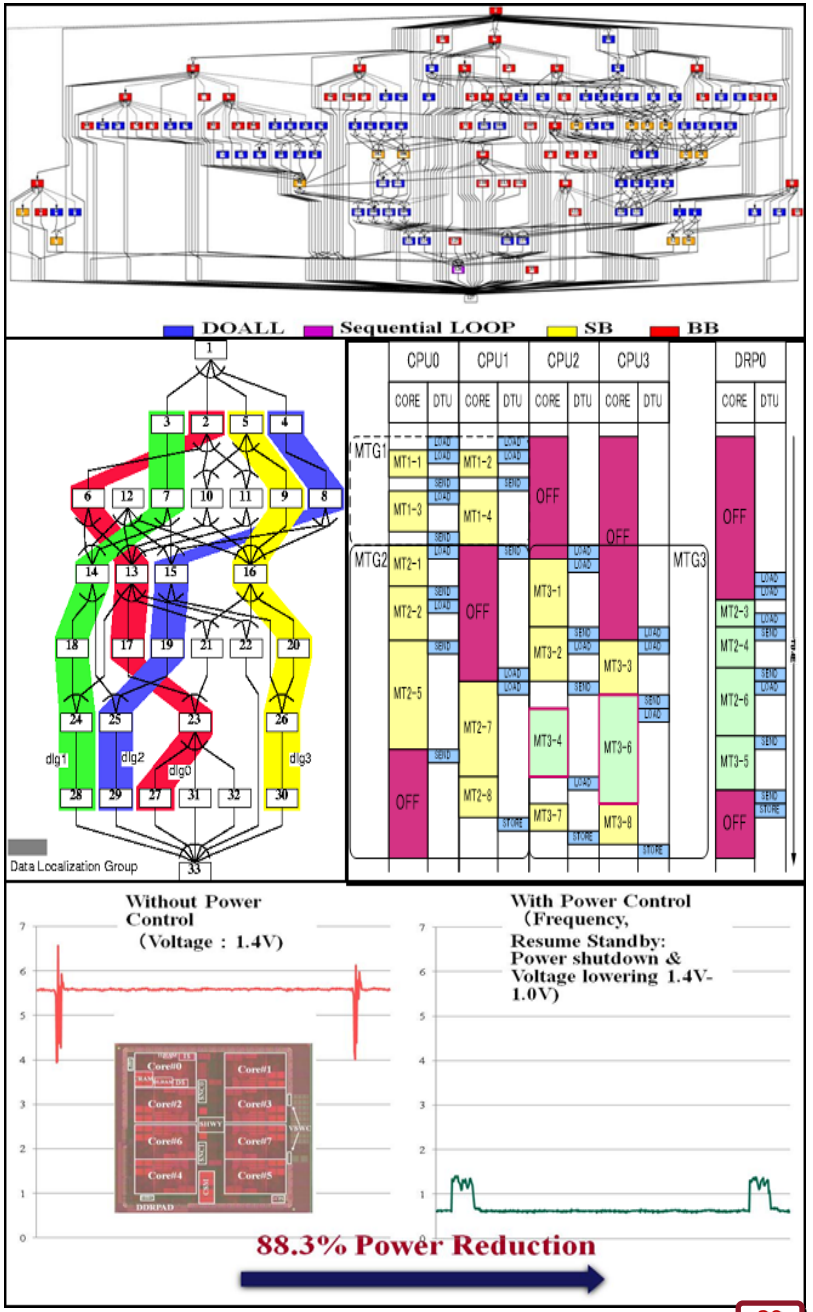
- 粗粒度タスク並列化、ループ並列化、近細粒度並列化によりプログラム全域の並列性を利用するマルチグレイン並列化機能により、従来の命令レベル並列性より大きな並列性を抽出し、複数マルチコアで速度向上

2.プログラム全域にわたるメモリ利用最適化

- コンパイラによるローカルメモリへのデータ分割配置、DMAコントローラによるタスク実行とオーバーラップしたデータ転送によりメモリアクセス・データ転送オーバーヘッド最小化

3.プロセッサ・メモリ・ネットワーク等の停止・動作速度制御による自動省エネ

- コンパイラによる低消費電力制御機能を用いたアプリケーション内でのきめ細かい周波数・電圧制御・電源遮断により消費電力低減



IEEE COMPUTER SOCIETY

https://www.computer.org/product/education/multi-core-video-lectures-bundle

Created by Multicore STC Chair Hironori Kasahara

Multi-Core Lecture Series consists of 11 one-hour lectures by some of the world's leading researchers in the field. This series is not a course and it consists of the presentation for those who are in the research field. This is more intended for research information sharing than educational training. Topics that are covered during these lectures are listed below. This series also includes an hour discussion of the lecturers.

Video Presentations:

- Automatic Parallelization by David Padua
- Autoparallelization for GPUs by Wen-Mei Hwu
- Dependences and Dependence Analysis by Utpal Banerjee
- Dynamic Parallelization by Rudolf Eigenmann
- Instruction Level Parallelization by Alexandru Nicolau
- Multigrain Parallelization and Power Reduction by Hironori Kasahara
- The Polyhedral Model by Paul Feautrier
- Vector Computation by David Kuck
- Vectorization by P. Sadayappan
- Vectorization/Parallelization in the IBM Compiler by Yaoqing Gao
- Vectorization/Parallelization in the Intel Compiler by Peng Tu
- Roundtable Discussion by all presenters

Dependences and Dependence Analysis by Utpal Banerjee Utpal Banerjee's research interests in computer science are in the general area of parallel processing and he has published four books on loop transformations and dependence analysis, with a fifth one on instruction level parallelism on the way.

Multigrain Parallelization and Power Reduction by Hironori Kasahara. Professor Kasahara has been researching on OSCAR Automatic Parallelizing and Power Reducing Compiler and OSCAR Multicore architecture for more than 30 years, and led four Japanese national projects on parallelizing compilers, multicores, and green computing.

実施場所：グリーン・コンピューティング・システム研究開発センター

2011年4月13日竣工，2011年5月13日開所

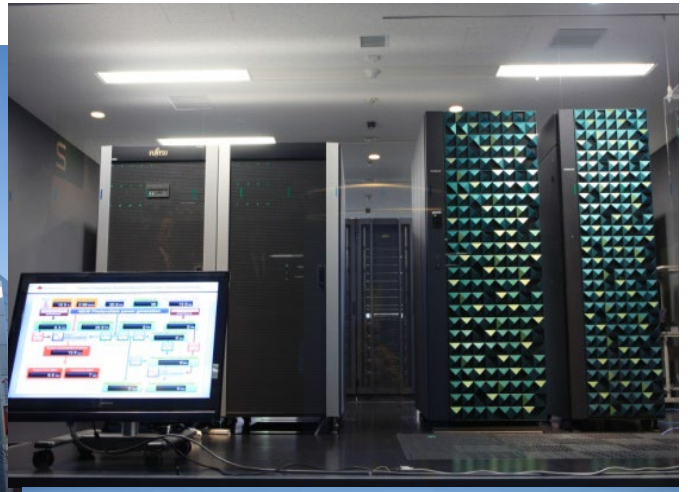
経済産業省「2009年度産業技術研究開発施設整備費補助金」
先端イノベーション拠点整備事業

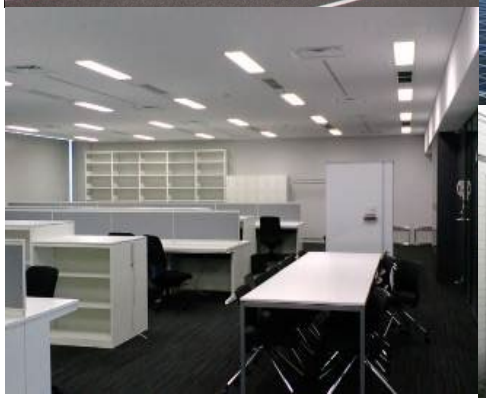
＜目標＞
太陽電池で駆動可能で
冷却ファンが不要な
超低消費電力・高性能マルチコア/
メニーコアプロセッサ*のハードウェア、
ソフトウェア、応用技術の研究開発

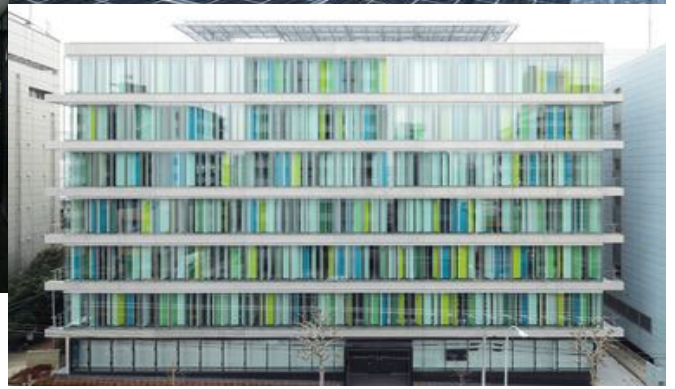
*1チップ上に多数のプロセッサコアを
集積する次世代マルチコアプロセッサ

＜産学連携＞
日立,富士通, ルネサス,NEC, トヨタ,
デンソー，オリンパス,NSITEX、三菱電機,
オスカーテクノロジ等

＜波及効果＞
超低消費電力メニーコア
- CO_2排出量削減
- サーバ国際競争力強化
- 我が国の産業利益を支える
  情報家電,自動車等の高付加価値化







グリーン・コンピューティング： 環境に優しい低消費電力・高性能計算

笠原博徳

制御

交通シミュレーション・信号制御 NTTデータ・日立

環境への貢献
カーボンニュートラル

生命・SDGsへの貢献

木村啓二

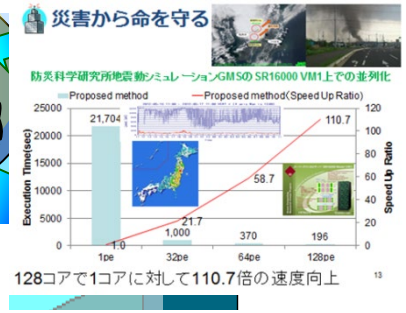
データセンター: 100WM(火力発電所必要)
→ 1000MW=1GW（原子力発電所必要）

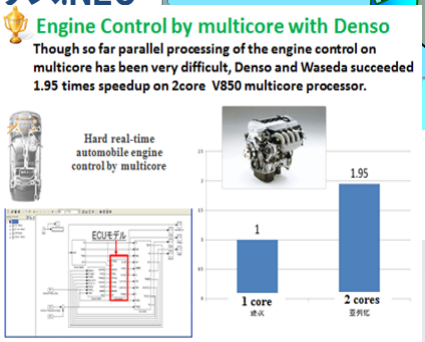
グリーンスパコン

車載(グリーンエンジン制御・自動運転Deep Learning・ADAS・MATLAB/Simulink自動並列化) デンソー, ルネサス,NEC

HPC,AI,BigData高速化・低消費電力化

グリーンデータ・クラウドサーバ

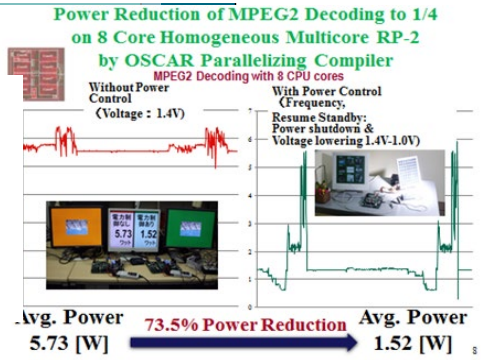




カプセル内視鏡オリンパス

パーソナルスパコン

首都圏直下型地震火災延焼、住民避難指示



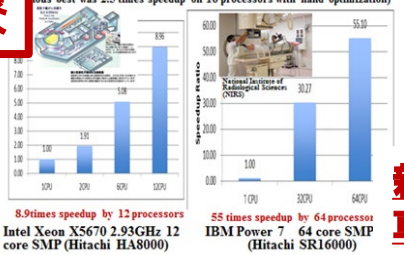
スマホ

高信頼・低コスト・ソフト開発

FA 三菱

カメラ

太陽光駆動



重粒子ガン治療日立

新幹線車体設計・ディープラーニング・日立

世界の人々への貢献
安全安心便利な製品・サービス
（産官学連携・ベンチャー）

高速化

低消費電力化

A Strategic Initiative of Computing: Systems and Applications (SISA)- Integrating HPC, Big Data, AI and Beyond, Jan.18-19, 2017

A Strategic Initiative of Computing:Systems and Applications (SISA) --Integrating HPC, Big Data, AI and Beyond-- Jan. 18-19, 2017

Opening: Prof. Gao, Prof. Kasahara

Waseda VP Shuji Hashimoto

I. Architecture and Applications

Keynote: William J. Dally,
NVIDIA and Stanford University, USA

- Kimihiko Hirao, RIKEN, Japan
- G. W. Yang, Tsinghua Univ. China
- J. Sexton, IBM, USA

II . System Software and Applications

Keynote： Rick. Stevens ANL, USA

- S. Mikhail Smelyanskiy Intel USA
- Fred. Streitz, LLNL USA
- R. Govind, IIS, India
- H. Hironori Kasahara, Waseda Univ,

III. Extreme Scale and Beyond

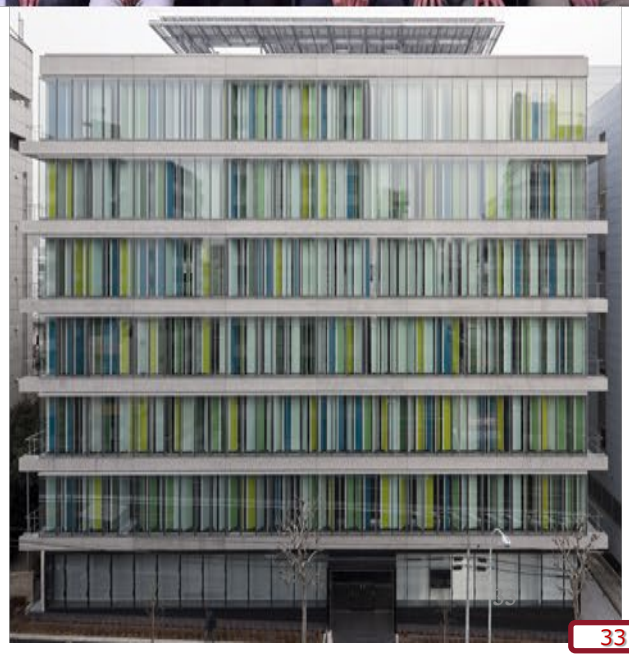
Keynote: Paul Messina ANL, USA

- Motoaki Saito, PEZY, Japan
- Eiji Ishida, MEXT, Japan
- Depei Qian, BUAA, China
- Toshiyuki Shimizu, Fujitsu, Japan

IV. Integration of HPC, Big Data, and AI

Keynote: Thomas Sterling, Indiana Univ., USA

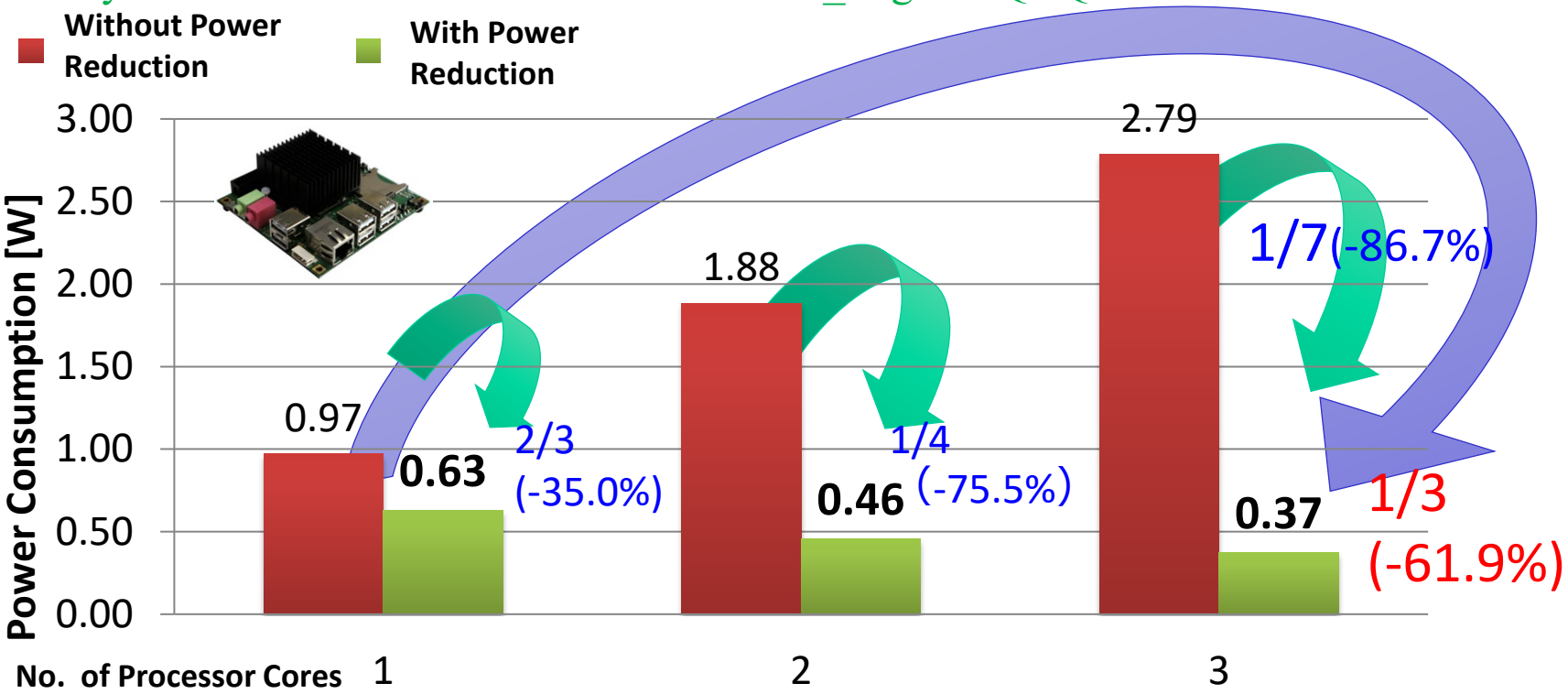
- Masaru Kitsuregawa, NII and Univ. of Tokyo, Japan
- Thomas Schulthess, ETH, Swiss
- Moriyuki Takamura/Toshiaki Kitamura, Oscar Tech, Japan



Automatic Power Reduction for MPEG2 Decode on Android Multicore

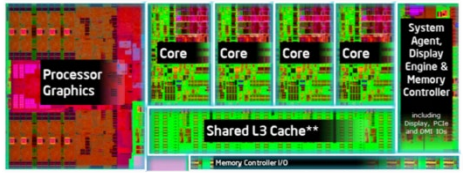
ODROID X2 ARM Cortex-A9 4 cores

http://www.youtube.com/channel/UCS43lNYEIkC8i_KIgFZYQBQ



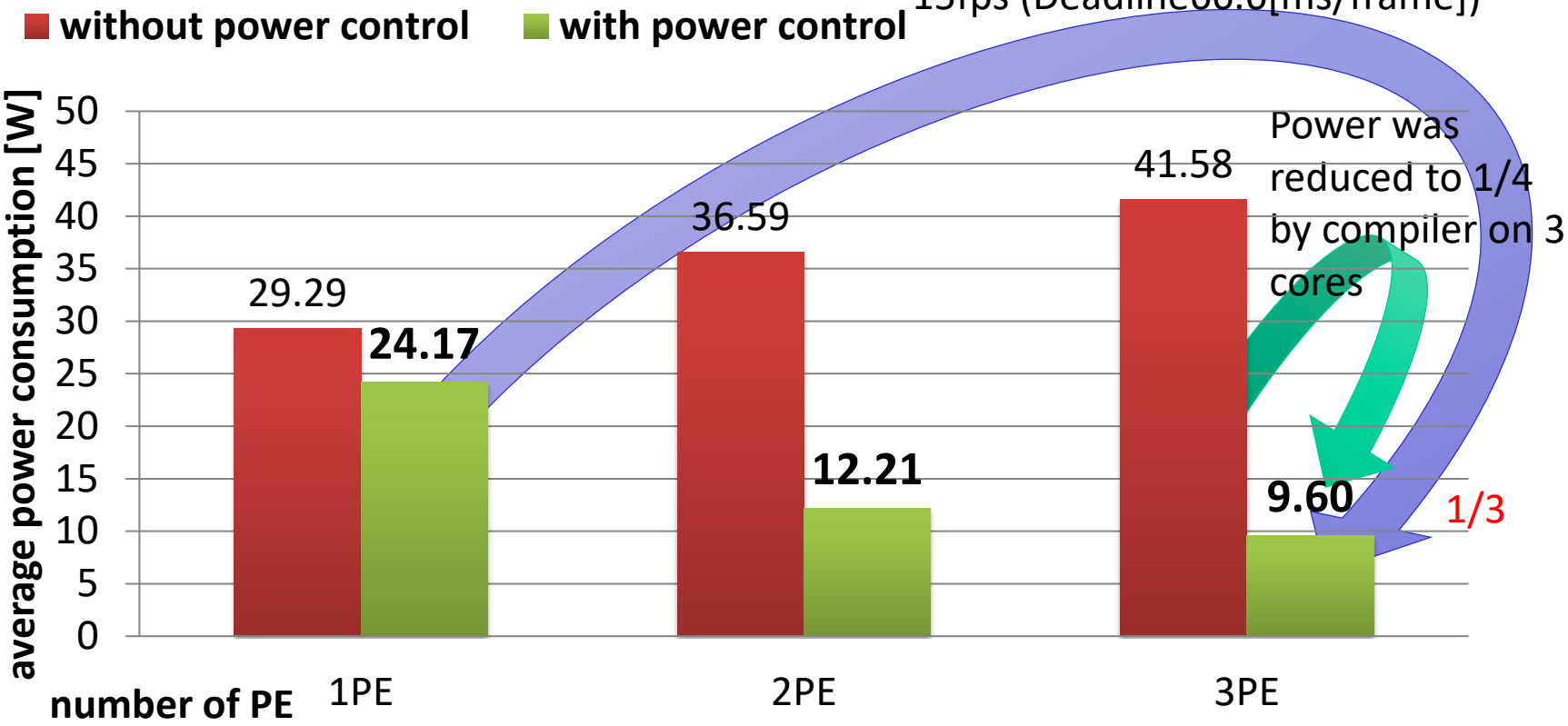
- On 3 cores, Automatic Power Reduction control successfully reduced power to 1/7 against without Power Reduction control.
- 3 cores with the compiler power reduction control reduced power to 1/3 against ordinary 1 core execution.

Power Reduction on Intel Haswell for Real-time Optical Flow



Intel CPU Core i7 4770K

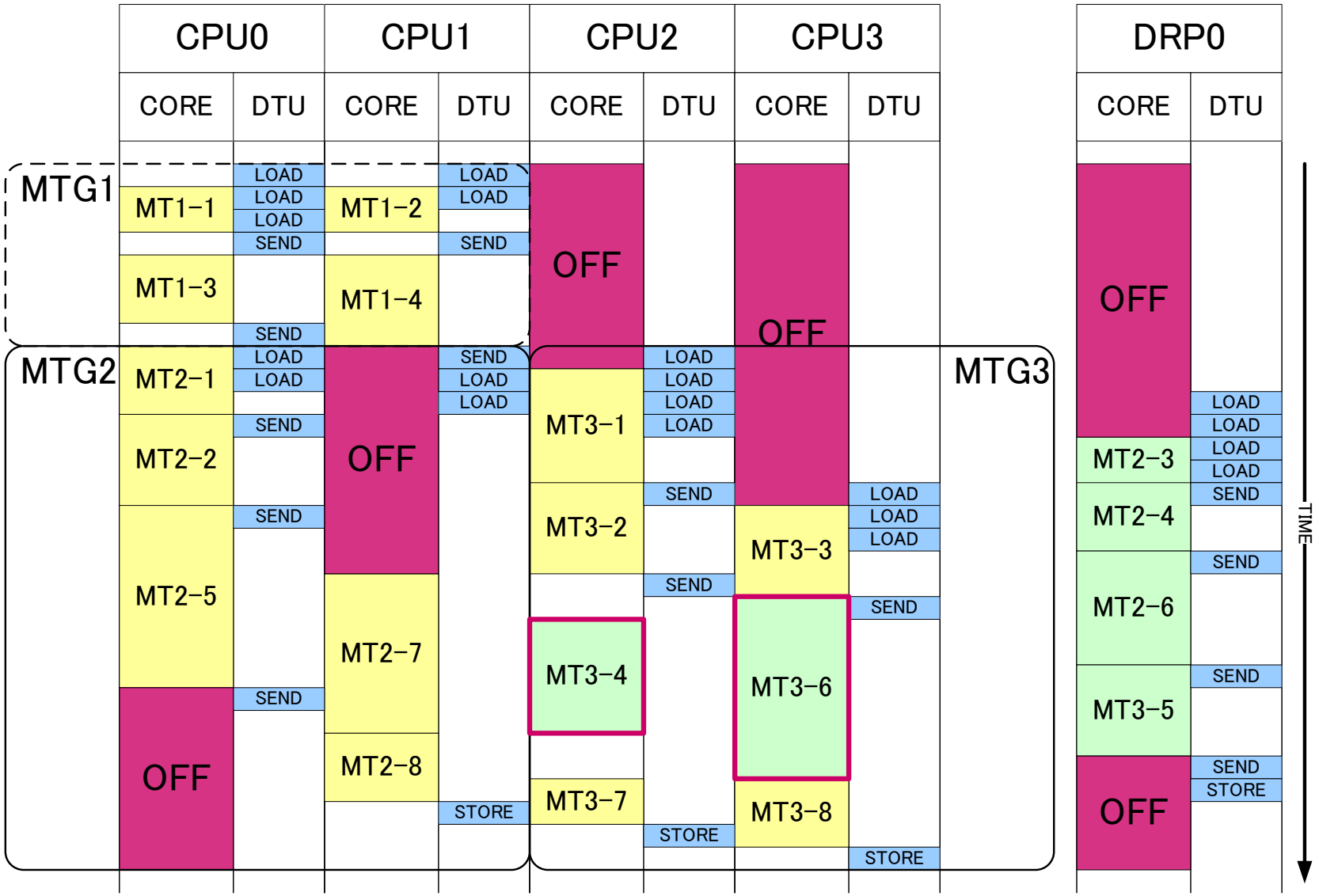
For HD 720p(1280x720) moving pictures
15fps (Deadline66.6[ms/frame])



Power was reduced to 1/4 (9.6W) by the compiler power optimization on the same 3 cores (41.6W).

Power with 3 core was reduced to 1/3 (9.6W) against 1 core (29.3W) .

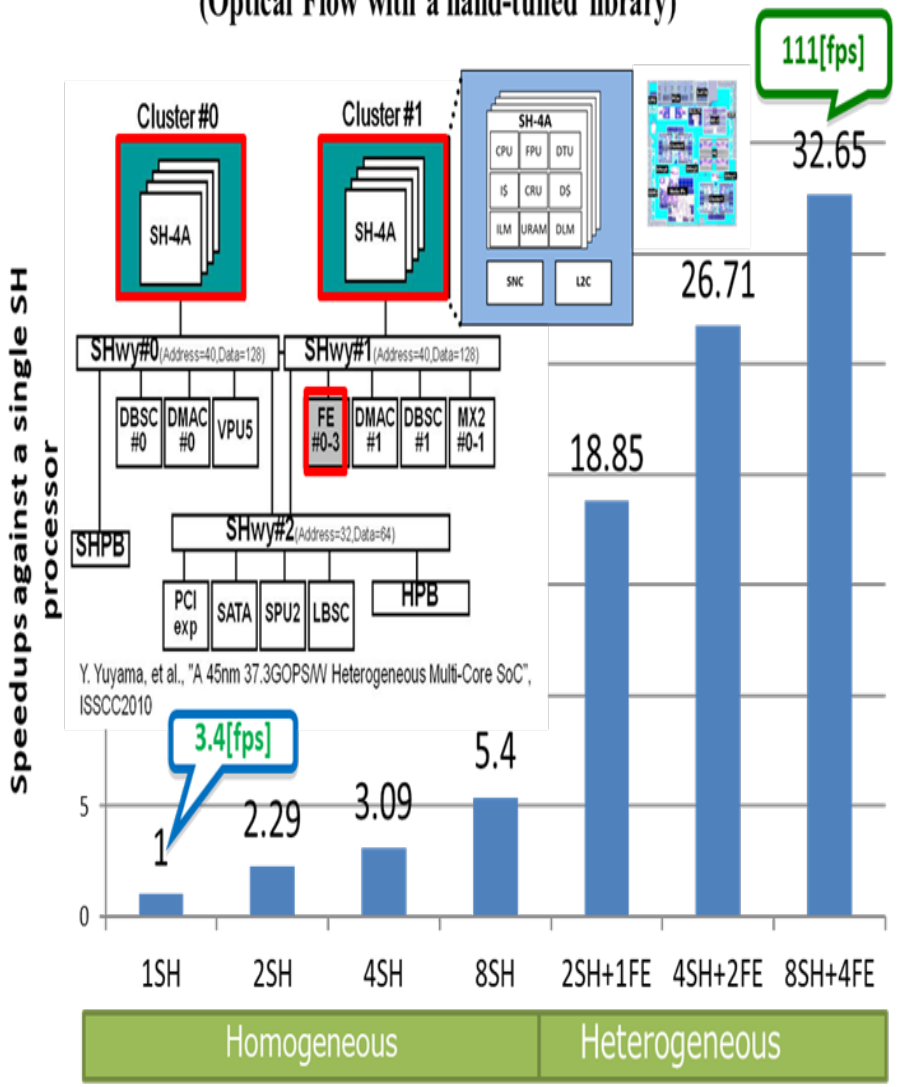
An Image of Static Schedule for Heterogeneous Multi-core with Data Transfer Overlapping and Power Control



Speedups & Power Reduction on RP-X Heterogeneous Multicore with 8 CPUs and 4 DRPs

33 Times Speedup Using OSCAR Compiler and API on Renesas RP-X with 8 CPUs & 4 DRP Accelerators

(Optical Flow with a hand-tuned library)



Power Reduction in a real-time execution controlled by OSCAR Compiler and OSCAR API on RP-X (Optical Flow with a hand-tuned library)

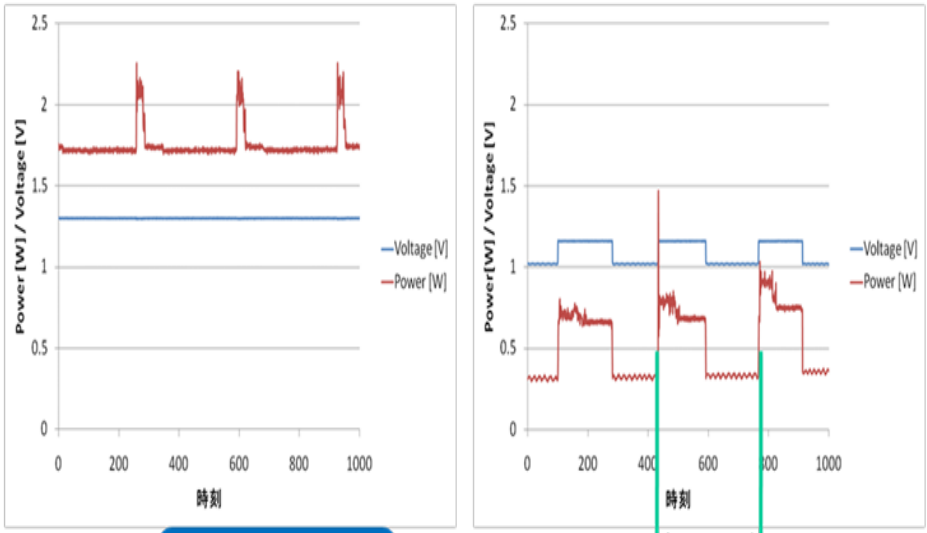
Without Power Reduction

With Power Reduction by OSCAR Compiler

70% of power reduction

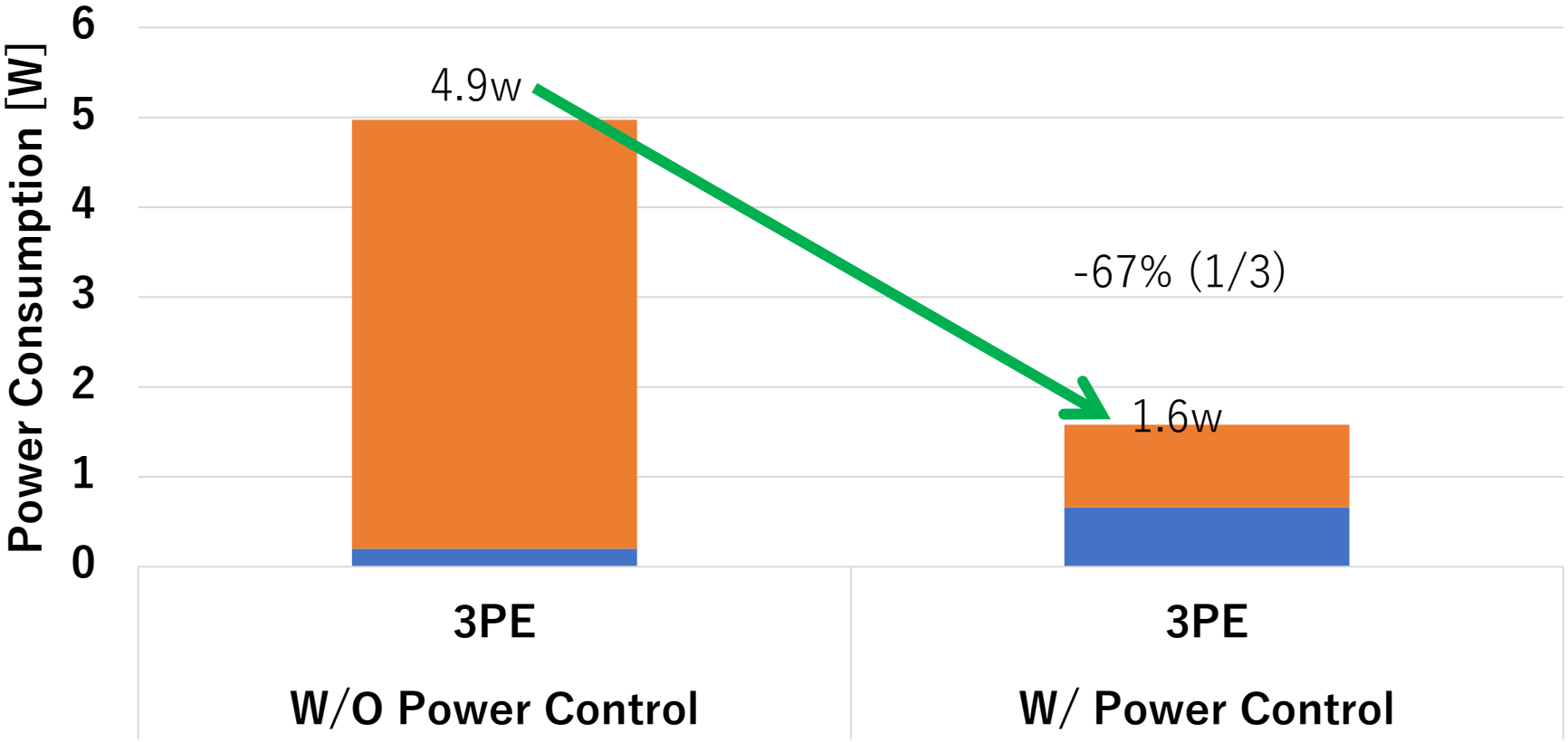
Average:1.76[W]

Average:0.54[W]



1cycle : 33[ms]
→30[fps]

Automatic Power Reduction of OpenCV Face Detection on big.LITTLE ARM Processor



- ODROID-XU3
  - Samsung Exynos 5422 Processor
    - 4x Cortex-A15 2.0GHz, 4x Cortex-A7 1.4GHz big.LITTLE Architecture
    - 2GB LPDDR3 RAM

Frequency can be changed by each cluster unit

ソーラーパワー・パーソナル・スパコン：新アクセラレータ・グリーンマルチコア

（AI、ビッグデータ、自動運転車、交通制御、ガン治療、地震、ロボット）

世界最高性能・低電力化機能OSCARコンパイラとの協調

ベクトルアクセラレータ併置・
共有メモリ型マルチコアシステム

性能：8TFLOPS, 主メモリ：8TB

電力：40W, 効率：200GFLOPS/W

- 命令拡張などのプロセッサにも付加できるベクトルアクセラレータ
  - 低消費電力で高速に立ち上がるベクトルで、低コスト設計
- コンパイラによる自動ベクトル・並列化及び自動電力削減
  - 周波数・電源電圧制御機能
  - バリア高速同期・ローカル分散メモリで無駄削減
  - ローカルメモリ利用で低メモリコスト
  - 誰でもチューニングなく使用でき、低コスト短期間ソフト開発可能

ISCA2025, June 21-25, 2025, Waseda University, Tokyo, Japan

General Co-Chairs: Jean-Luc Gaudiot (Prof. UCI)
Hironori Kasahara (Prof. Waseda)

ACM SIGARCH

IEEE COMPUTER SOCIETY TCCA
Technical Committee on Computer Architecture

About Tokyo

Easily accessible from all parts of the world
Tokyo provides the best access for travelers from all over the world. It is served by two international airports: Narita and Haneda. Narita International Airport offers over 1,600 international flights every week, connecting to 90 cities around the world, while Haneda Airport offers over 1,300 international flights weekly, serving 59 cities across the globe.

North and Central America · Europe · Asia · Middle East · Africa · South America · Oceania & South Pacific

A metropolis full of attractions like no other
Tokyo is one of the world's largest cities offering visitors a uniquely eclectic mix of traditional and contemporary attractions with something for everyone. In every corner of the city, there is a new and exciting discovery. From historical temples to high-tech museums to traditional gardens, there are numerous places to visit and enjoy. Tokyo will definitely provide an unforgettable experience for all.

TOKYO METROPOLITAN GOVERNMENT

東京 Tokyo

INVITATION to

ISCA 2025 TOKYO
June 21-25, 2025
Venue: Waseda University
Okuma Auditorium & Research innovation Center

General Co-Chairs:
Jean-Luc Gaudiot *Prof. UCI*
Hironori Kasahara *Prof. Waseda*

Greetings from the Governor of Tokyo

On behalf of the 14 million citizens of Tokyo, I look forward to welcoming you to our city for the 52nd International Symposium on Computer Architecture (ISCA2025) in TOKYO in 2025.

With a history of over 400 years as an economic and political center, Tokyo is a city that has its own distinct character and inherited unique traditions for a one-of-a-kind wellspring of culture.

As a leading international meeting destination, Tokyo can cater to the needs of any organizer and has all the amenities necessary to host a successful event. The city boasts a state-of-the-art telecommunications network and a sophisticated public transport system, which runs on precise timetables from early morning to late at night.

Tokyo is a fascinating destination with a mix of tradition and innovation. The traditional culture from the Edo period in the 17th to 19th centuries and the latest cutting-edge technology stand side by side. From the most popular tourist spots like the iconic Shibuya crossing to the Tama area's rich nature and the islands of Tokyo, a wide variety of options awaits visitors. We are confident that the conference attendees will enjoy Tokyo's many attractions, including the arts, shopping, and exquisite Japanese and global cuisine.

ISCA2025 will not only be a resounding success but a memorable experience for all delegates. I hope that the June 2025 meeting in Tokyo will lead to further development in the field of Computer Architecture worldwide.

Yuriko Koike
Governor of Tokyo

Greetings from ISCA 2025 General Co-Chair

Greetings, I am Professor Hironori Kasahara, a General Chair of the ISCA 2025, Tokyo, with Professor Jean-Luc Gaudiot from the University of California, Irvine. I served as the president of the IEEE Computer Society in 2018. Jean-Luc served in 2017. I also worked as the SEVP at Waseda University from 2018 to 2022.

I am pleased to welcome next year's ACM/IEEE ISCA participants, on June 21st to June 25th, 2025, to Waseda University, Tokyo, Japan. It is a great honor for Japan's architecture community to organize the "ISCA 52 @Japan" in 2025, 39 years after the "ISCA 13 @Japan" held in 1986.

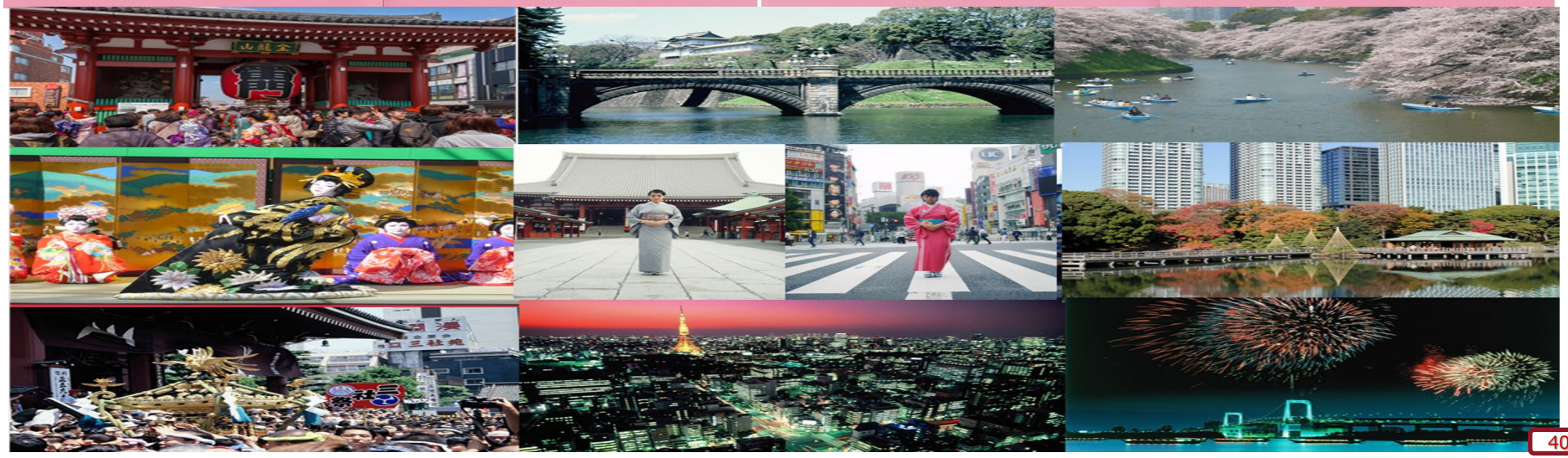
Waseda University is located in Shinjuku, also home to Tokyo Metropolitan Government. The symposium will be held in the heart of Waseda University, the Okuma Auditorium, where many international heads of state and entrepreneurs have given talks, and in a brand-new Research Innovation Center for establishing an Open Innovation Ecosystem.

ISCA 2025 will provide advanced technical papers, presentations, posters, and discussions alongside students' travel grants, featuring an exclusive excursion that captures the heart of Tokyo.

Fortunately, international participants will enjoy traveling to Japan and going on traditional or modern tours of our country at a cost-effective rate. Tokyo Metropolitan Government will gladly assist with various family programs throughout the symposium via the TCVB, which is preparing an information desk at ISCA 2024 in Buenos Aires. We look forward to seeing you in Tokyo next year!

Prof. Hironori Kasahara,
Waseda University

ACM SIGARCH TCCA



What Are the Most Cited ISCA Papers?

by David Patterson on Jun 15, 2023 https://www.sigarch.org/what-are-the-most-cited-isca-papers/

Rank	Citations	Year	Title (★ means it won the ISCA Influential Paper Award)	First Author + HOF Authors	Type	Topic
1	5351	1995	The SPLASH-2 programs: Characterization and methodological considerations	Stephen Woo, *Anoop Gupta*	Tool	Benchmark
2	4214	2017	In-datacenter performance analysis of a Tensor Processing Unit	*Norm Jouppi, David Patterson*	Arch	Machine Learning
3	3834	2000	★ Wattch: A framework for architectural-level power analysis and optimizations	*David Brooks, Margaret Martonosi*	Tool	Power
4	3386	1993	★ Transactional memory: Architectural support for lock-free data structures	Maurice Herlihy	Micro	Parallelism
5	2690	2016	EIE: Efficient inference engine on compressed deep neural network	Song Han, *Bill Dally, Mark Horowitz*	Arch	Machine Learning
6	2620	2007	★ Power provisioning for a warehouse-sized computer	Xiaobo Fan, *Luiz Barroso*	Micro	Power
7	2507	1992	Active messages: a mechanism for integrated communication and computation	Thorsten von Eiken	Micro	Parallelism
8	2391	2011	Dark silicon and the end of multicore scaling	*Hadi Esmaeilzadeh, Doug Burger, Karthikeyan Sankaralingam*	Micro	Parallelism
9	2352	1995	★ Simultaneous multithreading: Maximizing on-chip parallelism	*Dean Tullsen, Susan Eggers, Hank Levy*	Micro	Parallelism
10	2243	1990	★ Improving direct-mapped cache performance by the addition of a small fully-associative cache and prefetch buffers	*Norm Jouppi*	Micro	Cache
11	1801	2009	Architecting phase change memory as a scalable DRAM Alternative	Benjamin Lee, *Doug Burger, Engin Ipek, Onur Mutlu*	Micro	NV RAM
12	1790	1990	Memory consistency and event ordering in scalable shared-memory multiprocessors	*Kourosh Gharachorloo, Anoop Gupta, John Hennessy*	Micro	Consistency/ Coherence
13	1769	2009	Scalable high performance main memory system using phase-change memory technology	*Moinuddin Qureshi*	Micro	NV RAM
14	1659	2016	ISAAC: A convolutional neural network accelerator with in-situ analog arithmetic in crossbars	Ali Shafiee, *Rajeev Balasubramonian, Naveen Muralimanohar*	Arch	Machine Learning
15	1643	2003	★ Temperature-aware microarchitecture	Kevin Skadron	Micro	Power
16	1557	2016	Eyeriss: A spatial architecture for energy-efficient dataflow for convolutional neural networks	Yu-Hsin Chen, *Joel Emer*	Micro	Machine Learning
17	1420	2016	Prime: A novel processing-in-memory architecture for neural network computation in ReRAM-based main memory	Ping Chi, *Yuan Xie*	Arch	Machine Learning
18	1401	2014	A reconfigurable fabric for accelerating large-scale datacenter services	Andrew Putnam, *Hadi Esmaeilzadeh*	Micro	Interconnect
19	1374	1992	The turn model for adaptive routing	Christopher Glass	Micro	Interconnect
20	1350	1995	Multiscalar processors	*Guri Sohi, T. N. Vijaykumar*	Micro	Parallelism
21	1302	2000	Memory access scheduling	Andrew Putnam, *Bill Dally*	Micro	Parallelism
22	1284	1997	★ Complexity-effective superscalar processors	Subbarao Palacharla, *Norm Jouppi, Jim Smith*	Micro	Parallelism
23	1221	2002	★ Drowsy caches: simple techniques for reducing leakage power	Krisztián Flautner, *Nam Sung Kim, Trevor Mudge*	Micro	Power
24	1210	1996	★ Exploiting choice: Instruction fetch and issue on an implementable simultaneous multithreading processor	*Hank Levy, Susan Eggers, Joel Emer, Dean Tullsen*	Micro	Parallelism
25	1201	1997	A Study of Branch Prediction Strategies	*Jim Smith*	Micro	Parallelism
26	1201	1997	The SGI Origin: A ccNUMA highly scalable server	James Laudon	Arch	Consistency/ Coherence
27	1177	2009	A durable and energy efficient main memory using phase change memory technology	Ping Zhou	Tool	Benchmark
28	1175	2014	Flipping bits in memory without accessing them: An experimental study of DRAM disturbance errors	Yoongu Kim, *Onur Mutlu, Chris Wilkerson*	Micro	Security
29	1166	2010	Debunking the 100X GPU vs. CPU myth: an evaluation of throughput computing on CPU and GPU	Victor Lee	Tool	Simulator
30	1104	2017	SCNN: An accelerator for compressed-sparse convolutional neural networks	Angshuman Parashar, *Joel Emer, Bill Dally, Steve Keckler*	Arch	Machine Learning
31	1070	2015	ShiDianNao: Shifting vision processing closer to the sensor	Zidong Du	Arch	Machine Learning
32	1051	1994	★ The Stanford FLASH multiprocessor	Jeffrey Kuskin, *Kourosh Gharachorloo, Anoop Gupta, John Hennessy, Mark Horowitz*	Arch	Parallelism
33	1027	2004	★ Transactional memory coherence and consistency	Lance Hammond, *Christos Kozyrakis, Kunle Olukotun*	Micro	Consistency/ Coherence
34	1021	1992	Lazy release consistency for software distributed shared memory	Pete Keleher	Micro	Consistency/ Coherence
35	1006	2001	Cache decay: Exploiting generational behavior to reduce cache leakage power	*Stefanos Kaxiras, Margaret Martonosi*	Micro	Power
36	993	1990	The directory-based cache coherence protocol for the DASH multiprocessor	Daniel Lenoski, *Kourosh Gharachorloo, Anoop Gupta, John Hennessy*	Micro	Consistency/ Coherence
37	991	2000	Clock rate versus IPC: The end of the road for conventional microarchitectures	Vikas Agarwal, *Doug Burger, Steve Keckler*	Micro	Parallelism
38	980	1990	Weak ordering—a new definition	*Sarita Adve, Mark Hill*	Micro	Consistency/ Coherence
39	957	2008	Technology-driven, highly-scalable dragonfly topology	*John Kim, Bill Dally*	Micro	Interconnect
40	938	2007	Adaptive insertion policies for high performance caching	*Moinuddin Qureshi, Joel Emer, Yale Patt*	Micro	Cache
41	935	1973	Banyan networks for partitioning multiprocessor systems	Rodney Goke, *Jack Lipovski*	Micro	Interconnect
42	911	2008	3D-Stacked Memory Architectures for Multi-core Processors	*Gabriel Loh*	Micro	Cache
43	895	2010	High performance cache replacement using re-reference interval prediction (RRIP)	*Aamer Jaleel, Joel Emer*	Micro	Cache
44	877	2015	A scalable processing-in-memory accelerator for parallel graph processing	Junwhan Ahn, *Onur Mutlu*	Arch	Parallelism
45	873	2000	Transient fault detection via simultaneous multithreading	*Steven Reinhardt*	Micro	Reliability
46	868	2008	Corona: System implications of emerging nanophotonic technology	Dana Vantrease, *Norm Jouppi*	Micro	Interconnect
47	863	2009	An analytical model for a GPU architecture with memory-level and thread-level parallelism awareness	Sunpyo Hong	Tool	Parallelism
48	859	2004	Single-ISA heterogeneous multi-core architectures for multithreaded workload performance	*Rakesh Kumar, Norm Jouppi, Partha Ranganathan & Dean Tullsen*	Micro	Parallelism
49	854	1974	A Preliminary Architecture for a Basic Data Flow Processor	Jack Dennis	Arch	Parallelism
50	854	1983	Very Long Instruction Word Architectures and the ELI-512	Josh Fisher	Arch	Parallelism

Future Multicore Products with Automatic Parallelizing Compiler

Next Generation Automobiles

- Safer, more comfortable, energy efficient, environment friendly
- Cameras, radar, car2car communication, internet information integrated brake, steering, engine, moter control

Smart phones

-From everyday recharging to less than once a week
- Solar powered operation in emergency condition
- Keep health

Advanced medical systems

Cancer treatment,
Drinkable inner camera

- Emergency solar powered
- No cooling fun, No dust , clean usable inside OP room

Personal / Regional Supercomputers

Solar powered with more than 100 times power efficient : FLOPS/W

- Regional Disaster Simulators saving lives from tornadoes, localized heavy rain, fires with earth quakes