グリーンコンピューティングに貢献する並列化コンパイラとコンパイラ協調型マルチコアアーキテクチャに関する先駆的研究への貢献

早稲田大学　副総長（研究推進）笠原博徳

IEEE Computer Society President 2018

1980 早大電気工学科卒，1982同修士了
1985 早大大学院博士課程了　工学博士
　　カリフォルニア大学バークレー客員研究員
1986 早大理工専任講師，1988年 助教授
1989～1990 イリノイ大学Center for
　　Supercomputing R&D客員研究員
1997 教授、現在 理工学術院情報理工学科
2004　アドバンストマルチコア研究所所長
2017 日本工学アカデミー会員（2020より理事），
　日本学術会議連携会員
2018　IEEE Computer Society President，早大副総長

1987 IFAC World Congress Young Author Prize
1997 情報処理学会坂井記念特別賞
2005 半導体理工学研究センタ共同研究賞
2008 LSI・オブ・ザ・イヤー 2008 準グランプリ，
　　Intel Asia Academic Forum Best Research Award
2010 IEEE CS Golden Core　Member Award
2014 文部科学大臣表彰科学技術賞研究部門
2015 情報処理学会フェロー，
2017 IEEE Fellow，2017 IEEE Eta-Kappa-Nu
2019 IEEE CS　Spirit of Computer Society Award
2020 情報処理学会功績賞，
テレコム先端技術研究支援センター(SCAT)表彰 会長大賞

査読付き論文222件，招待講演197件，
国際特許取得62件(米国・英国・中国・日本等)，
新聞・Web記事・TV等メディア掲載 660件

政府・学会委員等歴任数　265件
IEEE Computer Society President 2018, Executive Committee委員長，理事(2009-14)，戦略的計画委員長，Nomination Committee委員長，Multicore STC 委員長，IEEE CS Japan委員長 (2005-07)，IEEE技術委員，IEEE Medal選定委員，ACM/IEEE SC'21基調講演選定委員等
【経済産業省・NEDO】 情報家電用マルチコア・アドバンスト並列化コンパイラ・グリーンコンピューティング・プロジェクトリーダ，NEDOコンピュータ戦略委員長等
【内閣府】スーパーコンピュータ戦略委員，政府調達苦情検討委員，総合科学技術会議情報通信PT 研究開発基盤領域&セキュリティ・ソフト検討委，日本国際賞選定委
【文部科学省・海洋研】地球シミュレータ(ES)中間評価委員、情報科学技術委員，HPCI計画推進委員，次世代スパコン(京)中間評価委員・概念設計評価委員，地球シミュレータES2導入技術アドバイザイリー委員長等，
JST ムーンショット G3 ロボット & AI Vice Chair，
【COCN】産業競争力懇談会理事，等

第110回テレコム技術情報セミナー（PART-III）
SCAT会長大賞受賞講演　2021年7月7日

Some of papers in and just after Ph.D. Course in Waseda U.

IEEE TRANSACTIONS ON COMPUTERS, VOL. C-33, NO. 11, NOVEMBER 1984 1023

Practical Multiprocessor Scheduling Algorithms for Efficient Parallel Processing

HIRONORI KASAHARA, MEMBER, IEEE, AND SEINOSUKE NARITA, SENIOR MEMBER, IEEE

Courtesy of dexchao - Fotolia.com

104 IEEE JOURNAL OF ROBOTICS AND AUTOMATION, VOL. RA-1, NO. 2, JUNE 1985

Parallel Processing of Robot-Arm Control Computation on a Multimicroprocessor System

HIRONORI KASAHARA MEMBER, IEEE, AND SEINOSUKE NARITA, SENIOR MEMBER, IEEE

2nd International Conference on Superecomputing
Santa Clara, CA, USA May 3-8,1987

A PARALLEL PROCESSING SCHEME FOR THE SOLUTION OF SPARSE LINEAR EQUATIONS USING STATIC OPTIMAL-MULTIPROCESSOR-SCHEDULING ALGORITHMS

H.Kasahara*, T.Fujii*, H.Nakayama*, S.Narita*, and Leon O.Chua**

* Dept. of Electrical Eng., Waseda University, Tokyo, 160, Japan
** Dept. of Electrical Eng. and Computer Sciences, University of California, Berkeley, CA 94720, U.S.A.

Copyright © IFAC 10th Triennial World Congress, Munich, FRG, 1987

PARALLEL PROCESSING OF ROBOT MOTION SIMULATION

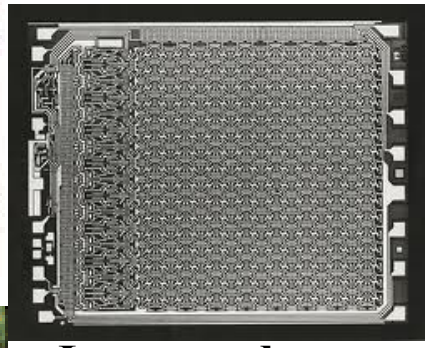
H. Kasahara, H. Fujii and M. Iwata

Department of Electrical Engineering, Waseda University, 3–4–1 Ohkubo Shinjuku-ku, Tokyo 160, Japan

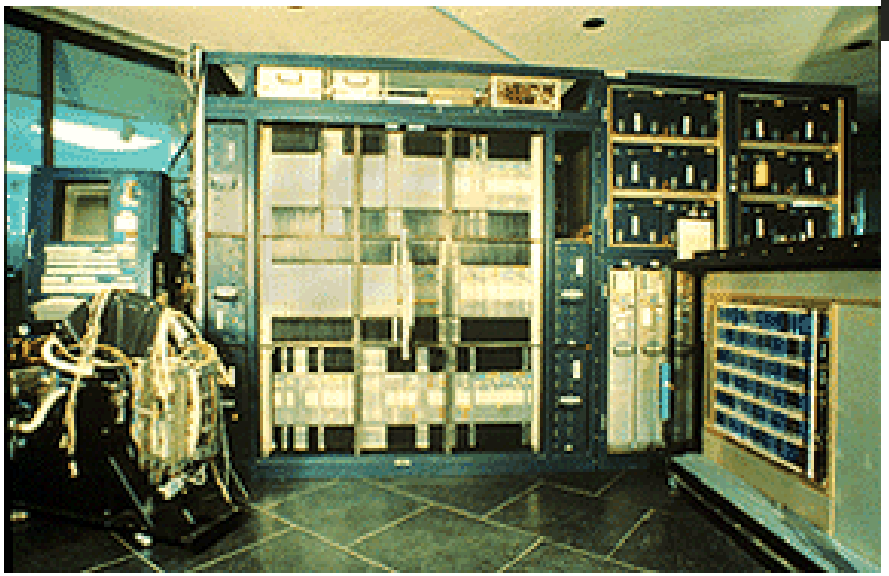
ILLIAC IV, Univ. Illinois at Urbana-Champaign & Burroughs

SIMD
64 Processor Element, Processor Array

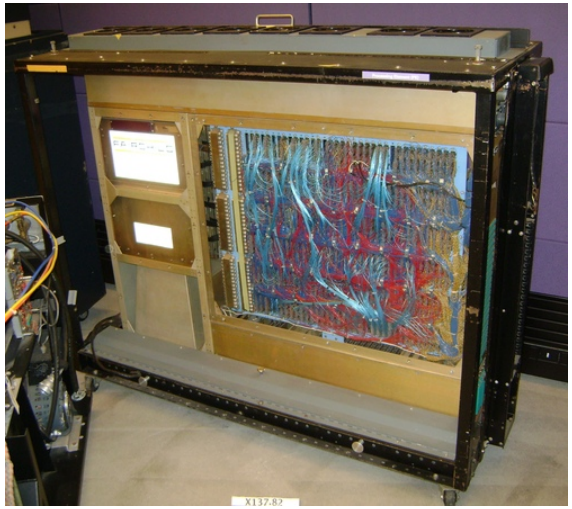
1972-3, NASA
200 MIPS,
300 MOPS,
1 billion bits per second of I/O transfer



Integrated circuits



Processing Element

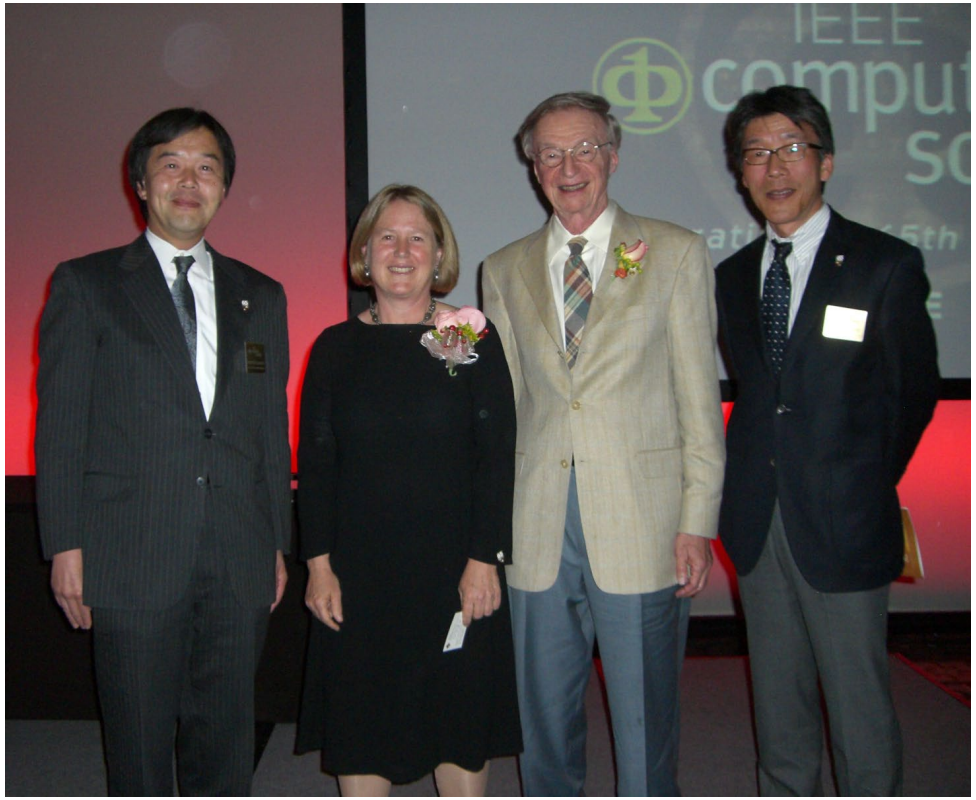


Prof. David J Kuck (Univ. Illinois, Intel)

IEEE Computer Pioneer Award 2011

Ms. Diane B. Greene (VMware Cofounder & CEO)

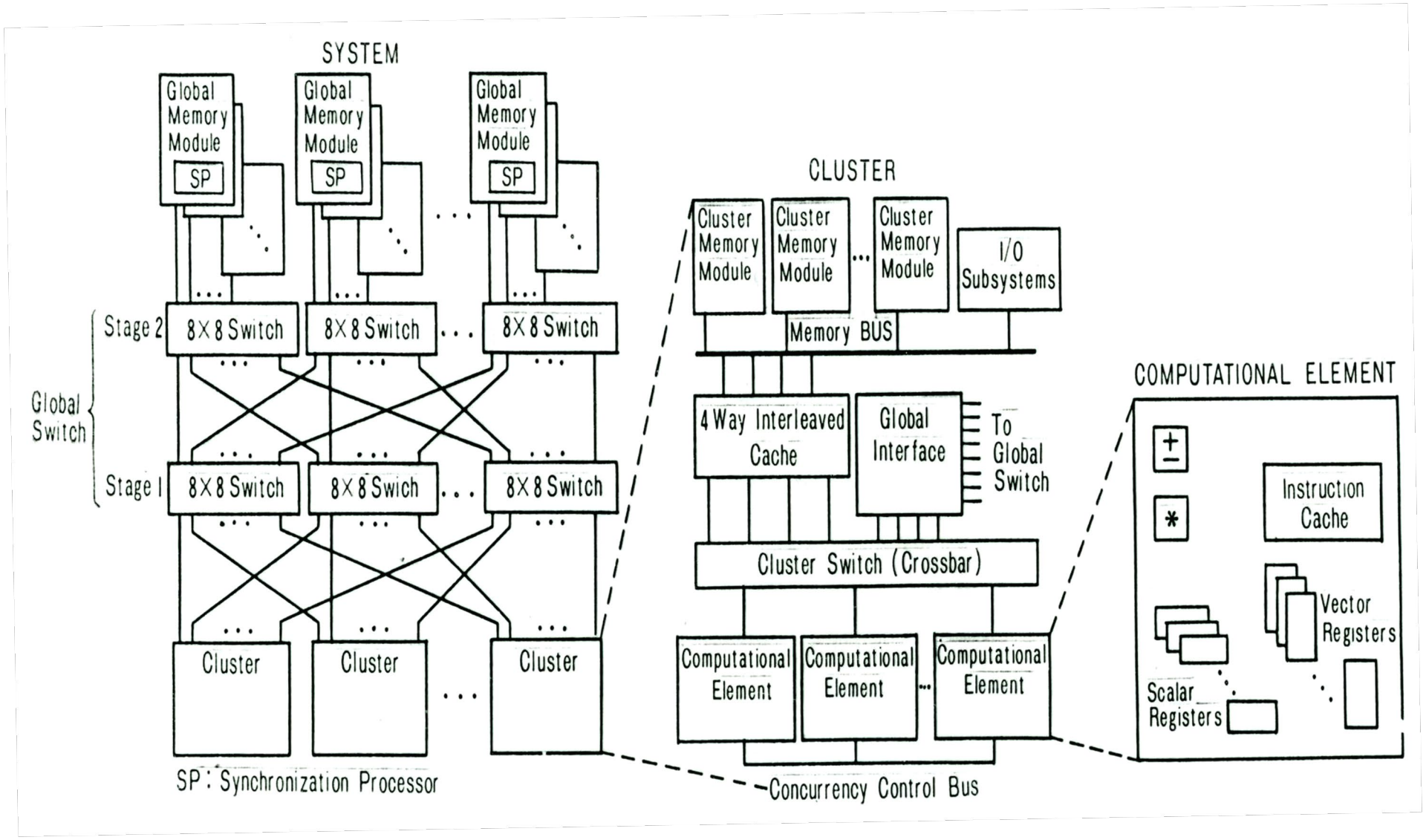
IEEE Computer Society Computer Entrepreneur Award 2011



2018.03.08 WasedaUniv. Symposium on Future of High Performance Green Computing 2018 (HPGC2018)

Cedar Supercomputer

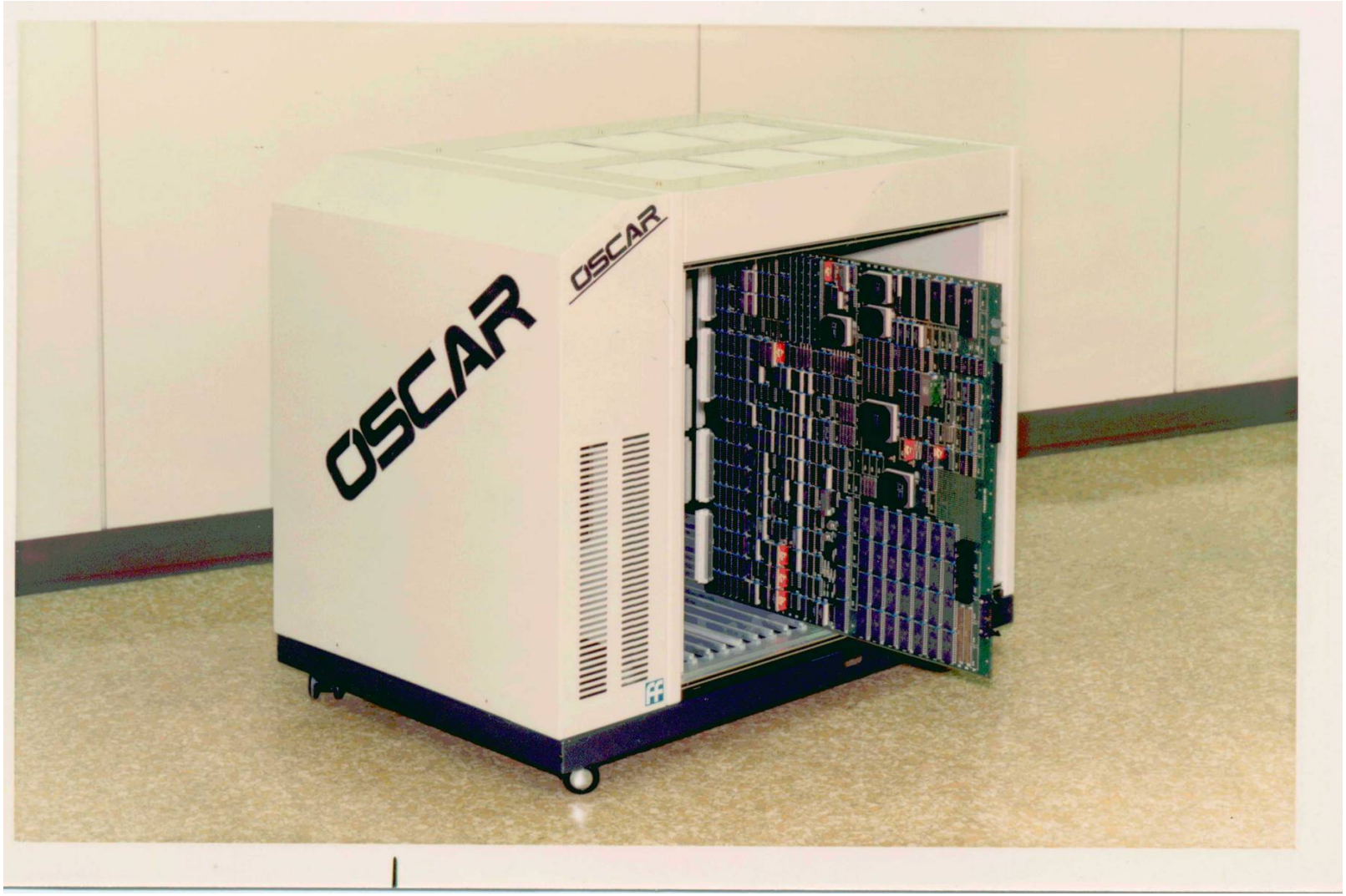
University of Illinois at Urbana-Champaign, CSRD (Center for Supercomputing R&D)



1987 OSCAR(Optimally Scheduled Advanced Multiprocessor)

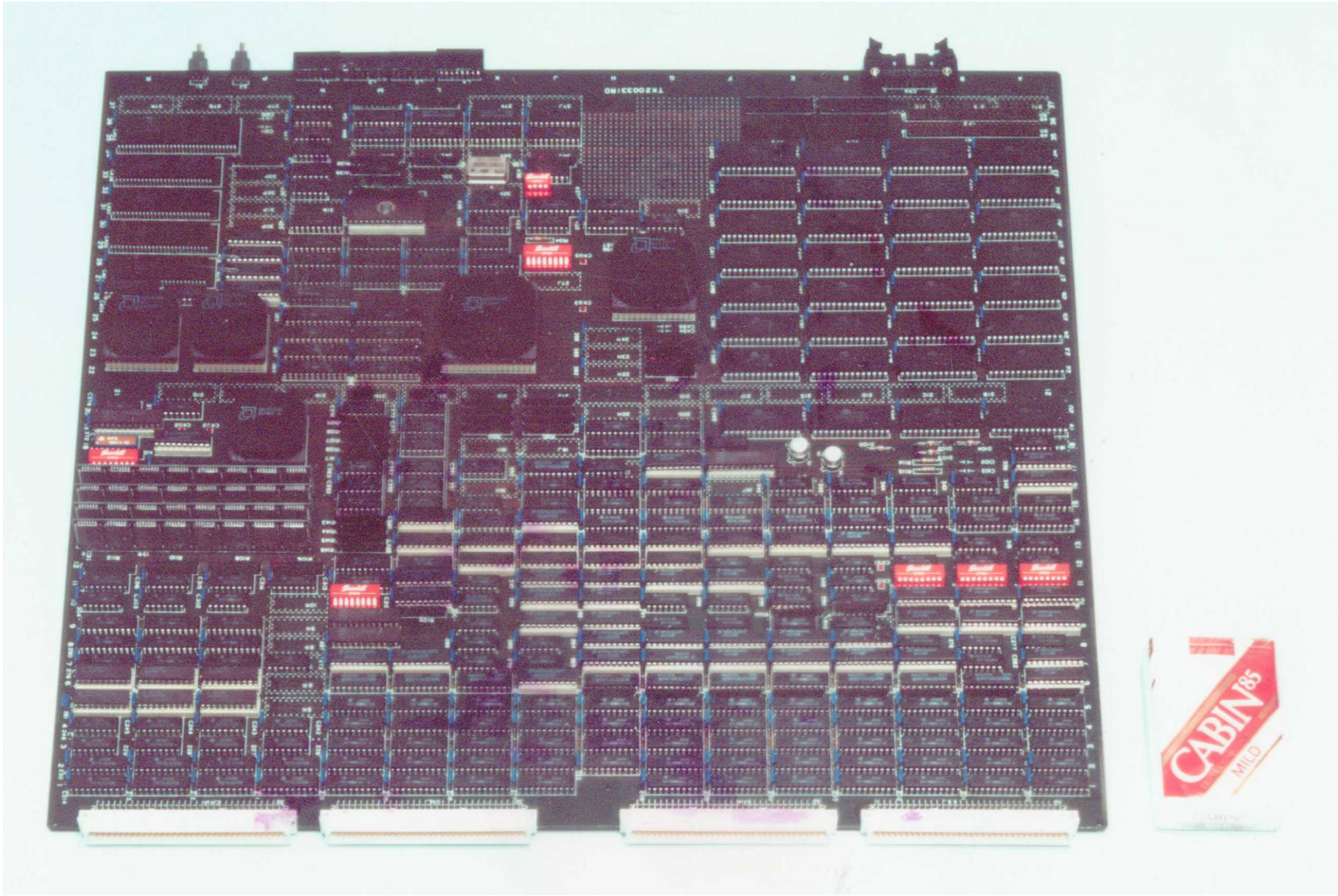
Co-design of Compiler and Architecture

Looking at various applications, design a parallelizing compiler and design a multiprocessor/multicore-processor to support compiler optimization

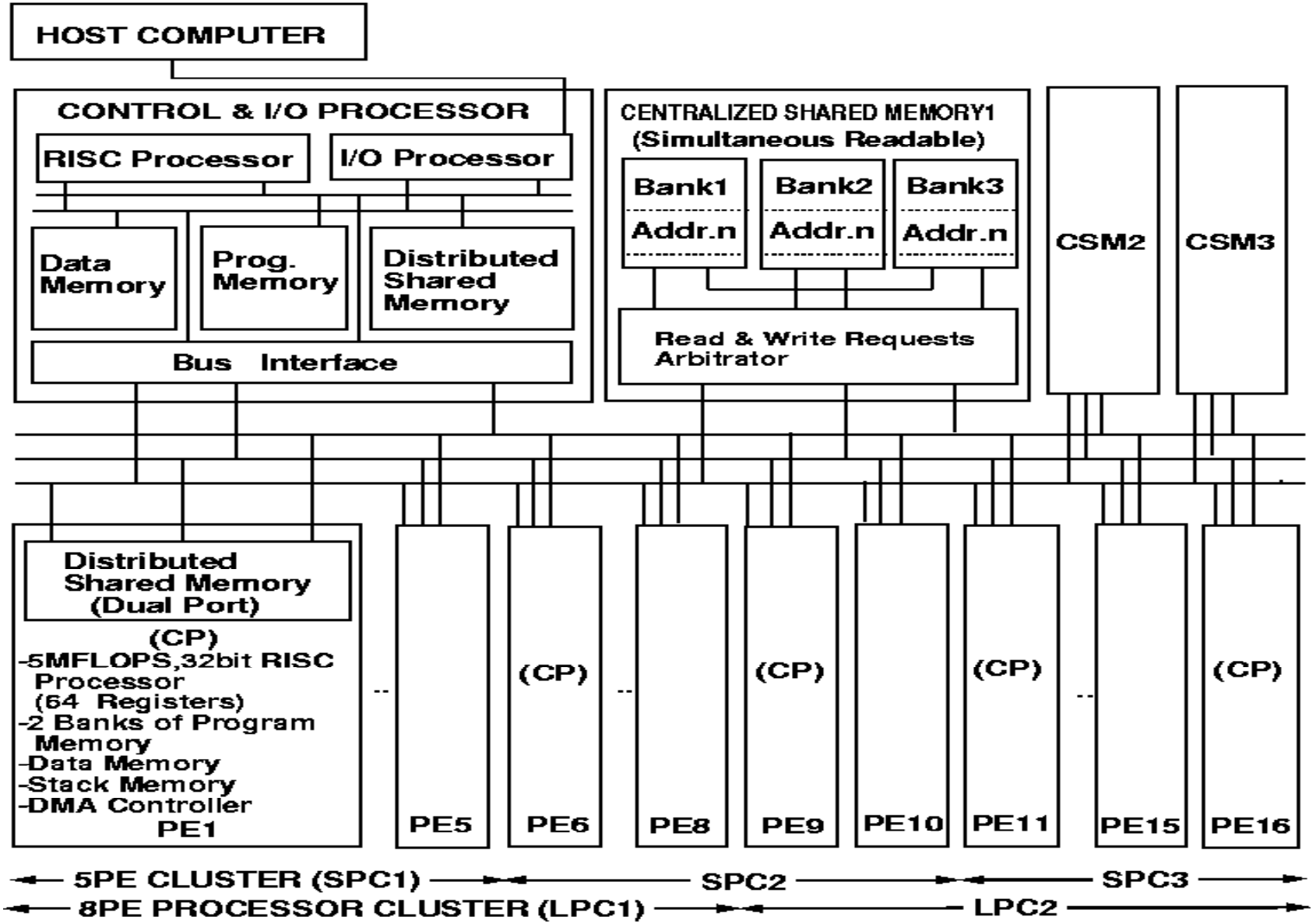


1987 OSCAR PE Board

(32bit RISC: Reduced Instruction Set Computer)



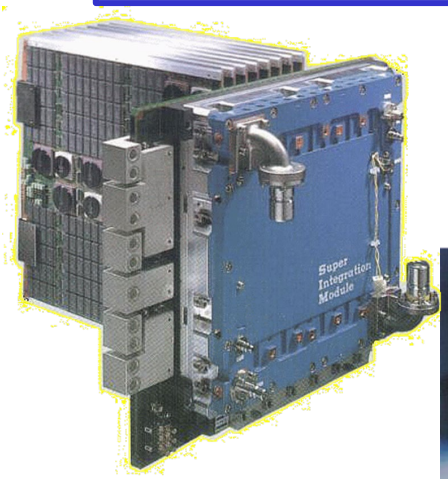
OSCAR(Optimally Scheduled Advanced Multiprocessor)

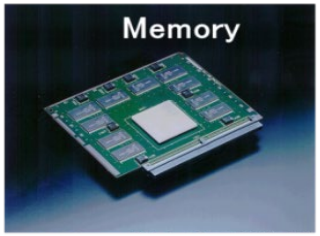


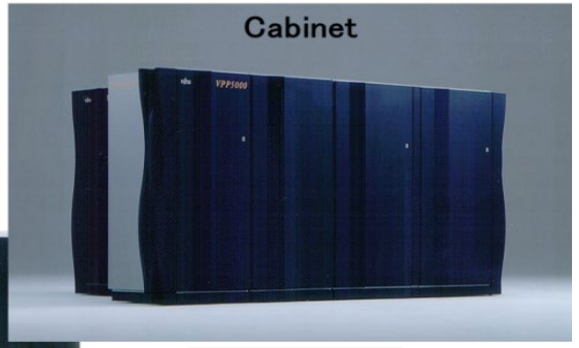
1993年 スーパーコンピュータVPP500、数値風洞(NWT)

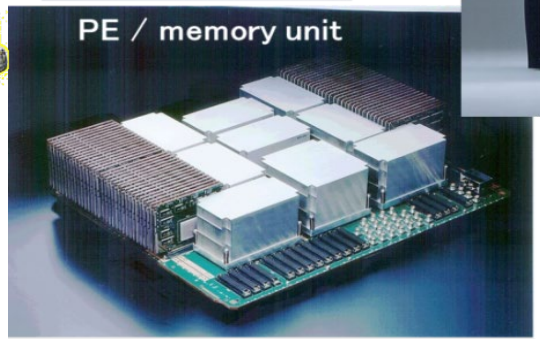
Mr. Hajime Miyoshi

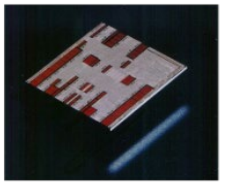
ACM/IEEE SC '94: Washington, D.C. November, 1994にて発表



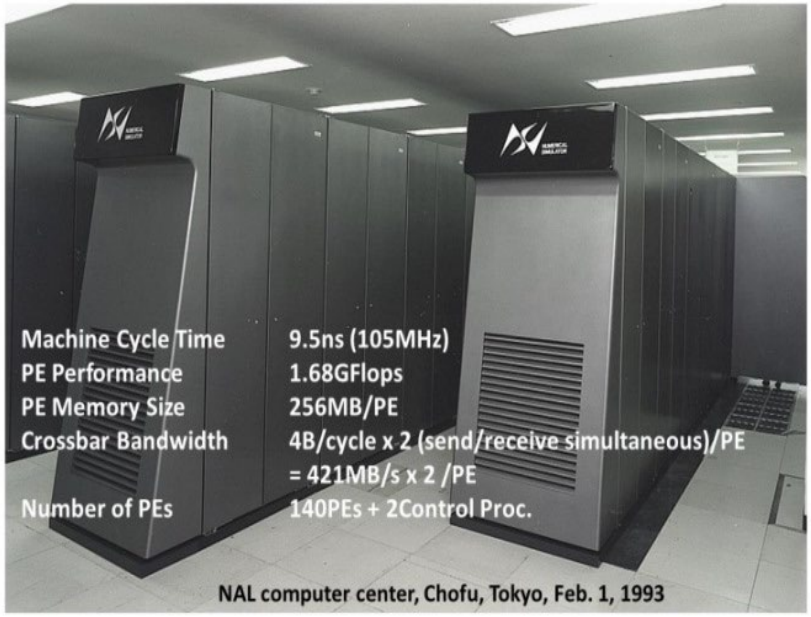




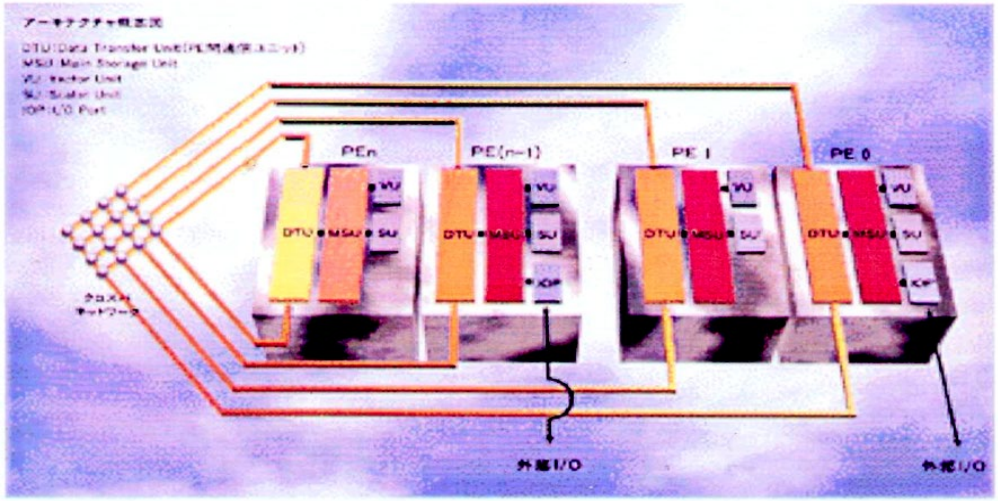




スパーコンピュータNWTの外観



商用VPP5000 (仏気象庁他)



OSCAR Parallelizing Compiler

To improve effective performance, cost-performance and software productivity and reduce power

Multigrain Parallelization (LCPC1991,2001,04)

coarse-grain parallelism among loops and subroutines (2000 on SMP), near fine grain parallelism among statements (1992) in addition to loop parallelism

Data Localization

Automatic data management for distributed shared memory, cache and local memory
(Local Memory 1995, 2016 on RP2,Cache2001,03)
Software Coherent Control (2017)

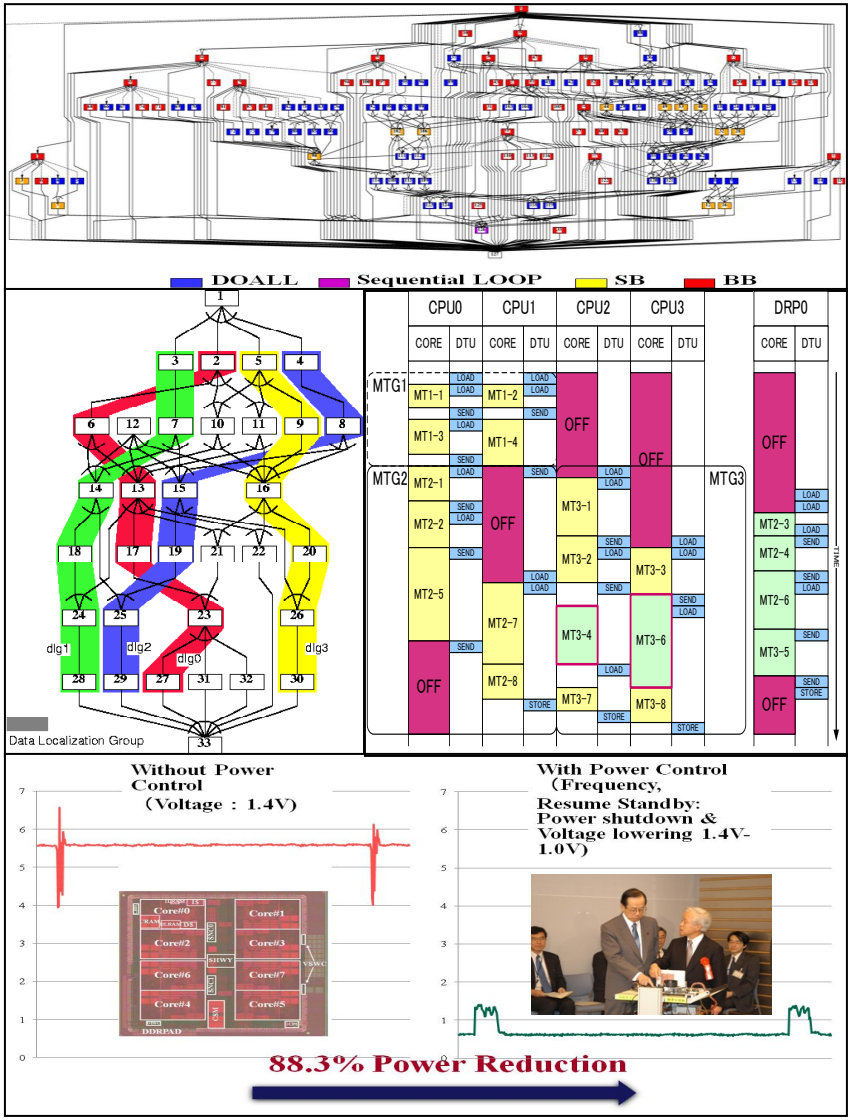
Data Transfer Overlapping (2016 partially)

Data transfer overlapping using Data Transfer Controllers (DMAs)

Power Reduction

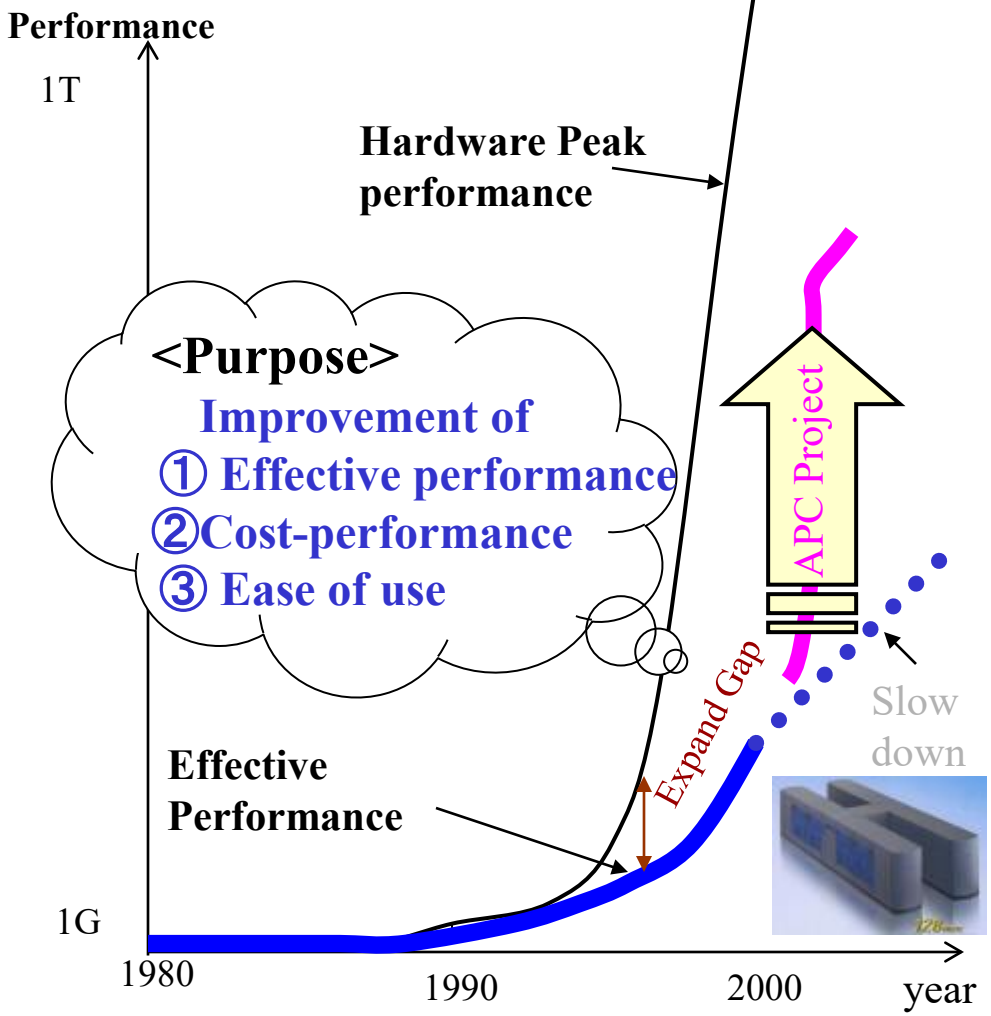
(2005 for Multicore, 2011 Multi-processes, 2013 on ARM)

Reduction of consumed power by compiler control DVFS and Power gating with hardware supports.



METI/NEDO Advanced Parallelizing Compiler Technology Project

Millenium Project IT21 2000.9.8 –2003.3.31
Waseda Univ., Fujitsu, Hitachi, AIST



Theoretical maximum performance vs. Effective performance of HPC

Background and Problems

①Adoption of parallel processing as a core technology on PC to HPC
② Increase of importance of software on IT
③ Need for improvement of cost-performance and usability

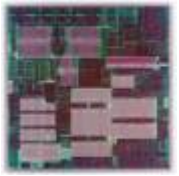
Contents of Research and Development

① R & D of advanced parallelizing compiler
Multigrain, Data localization, Overhead hiding
② R & D of Performance evaluation technology for parallelizing compilers

Goal: Double the effective performance

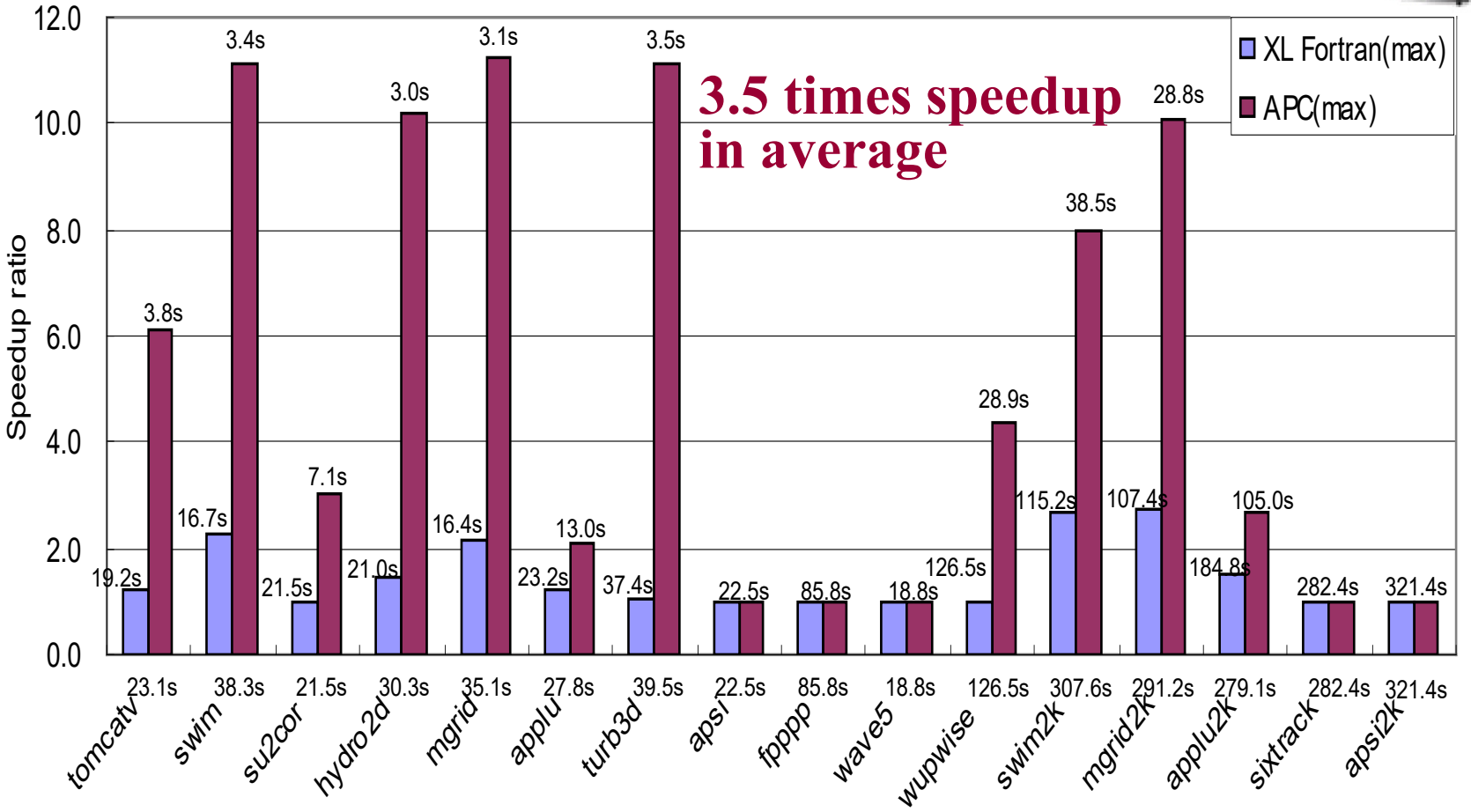
Ripple Effect

① Development of competitive next generation PC and HPC
② Putting the innovative automatic parallelizing compiler technology to practical use
③ Development and market acquisition of future single-chip multiprocessors
④ Boosting R&D in the following many fields:
IT, Bio-tech., Device, Earth environment, Next-generation VLSI design, Financial engineering, Weather forecast, New clean energy, Space development, Automobile, Electric Commerce, etc

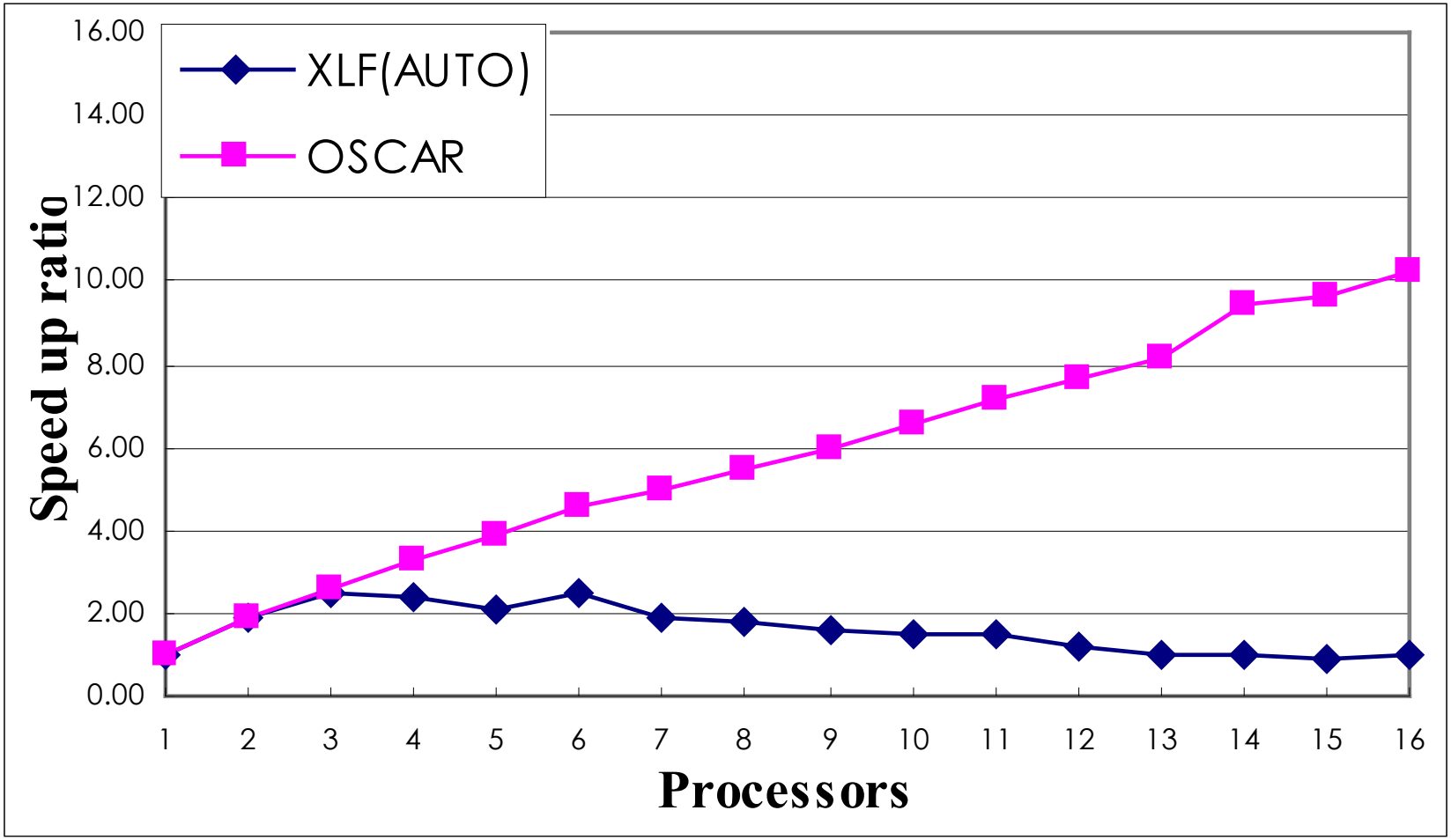


Performance of APC Compiler on IBM pSeries690 16 Processors High-end Server

- IBM XL Fortran for AIX Version 8.1
  - Sequential execution : -O5 -qarch=pwr4
  - Automatic loop parallelization : -O5 -qsmp=auto -qarch=pwr4
  - OSCAR compiler : -O5 -qsmp=noauto -qarch=pwr4 (su2cor: -O4 -qstrict)

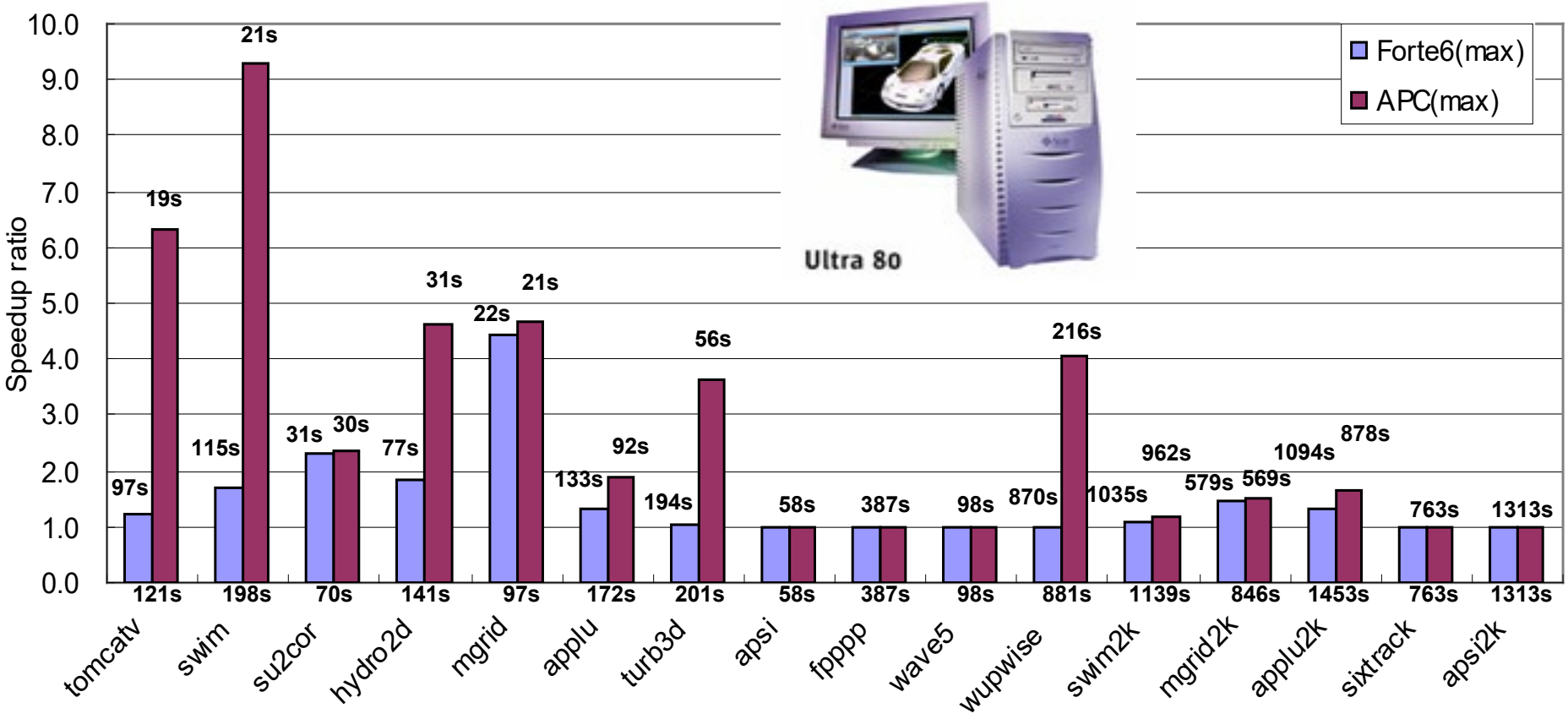


Performance of Multigrain Parallel Processing for 102.swim on IBM pSeries690

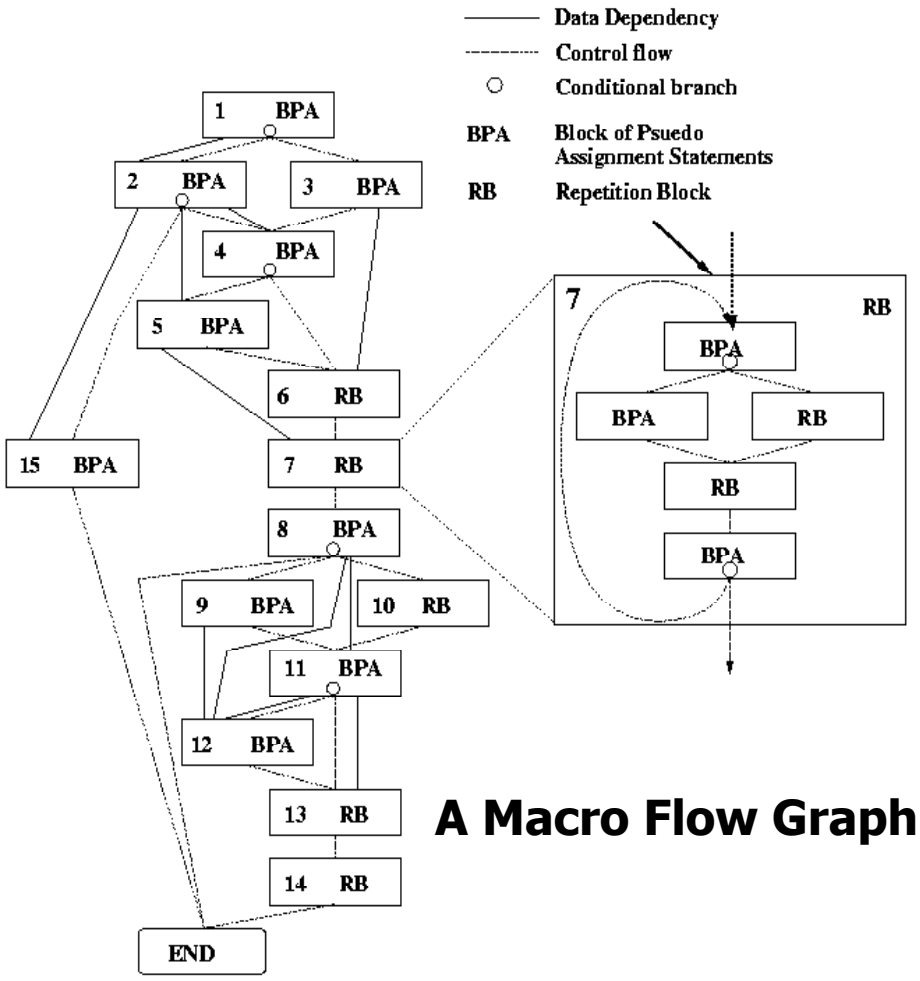


Performance of APC Compiler on Sun Ultra80 4 Processor Workstation

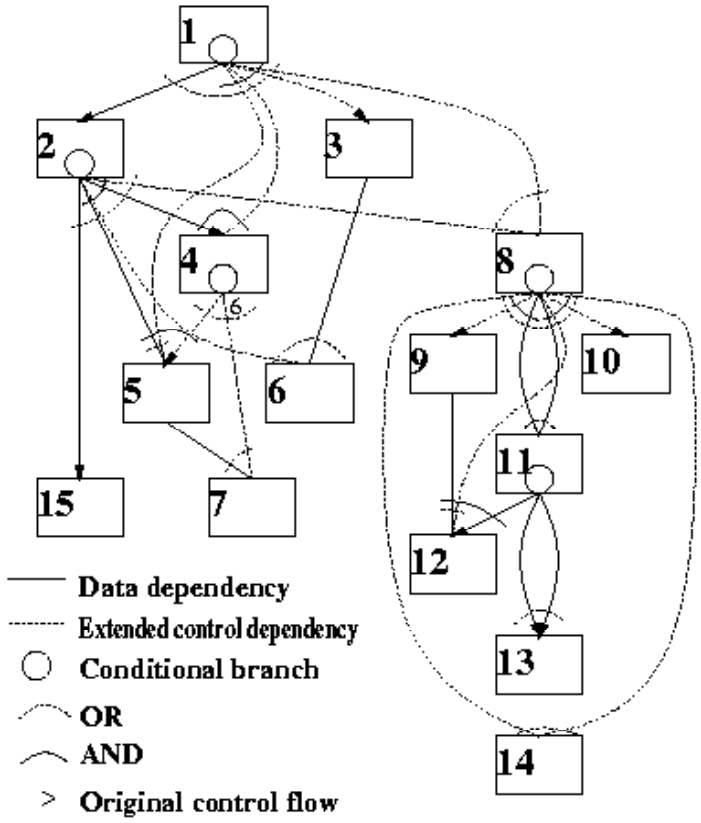
- Sun Forte Developer 6 Update 2
  - Sequential execution : -fast
  - Automatic loop parallelization : -fast -autopar -reduction -stackvar
  - OSCAR compiler : -fast -explicitpar -mp=openmp -stackvar



Earliest Executable Condition Analysis for coarse grain tasks (Macro-tasks)



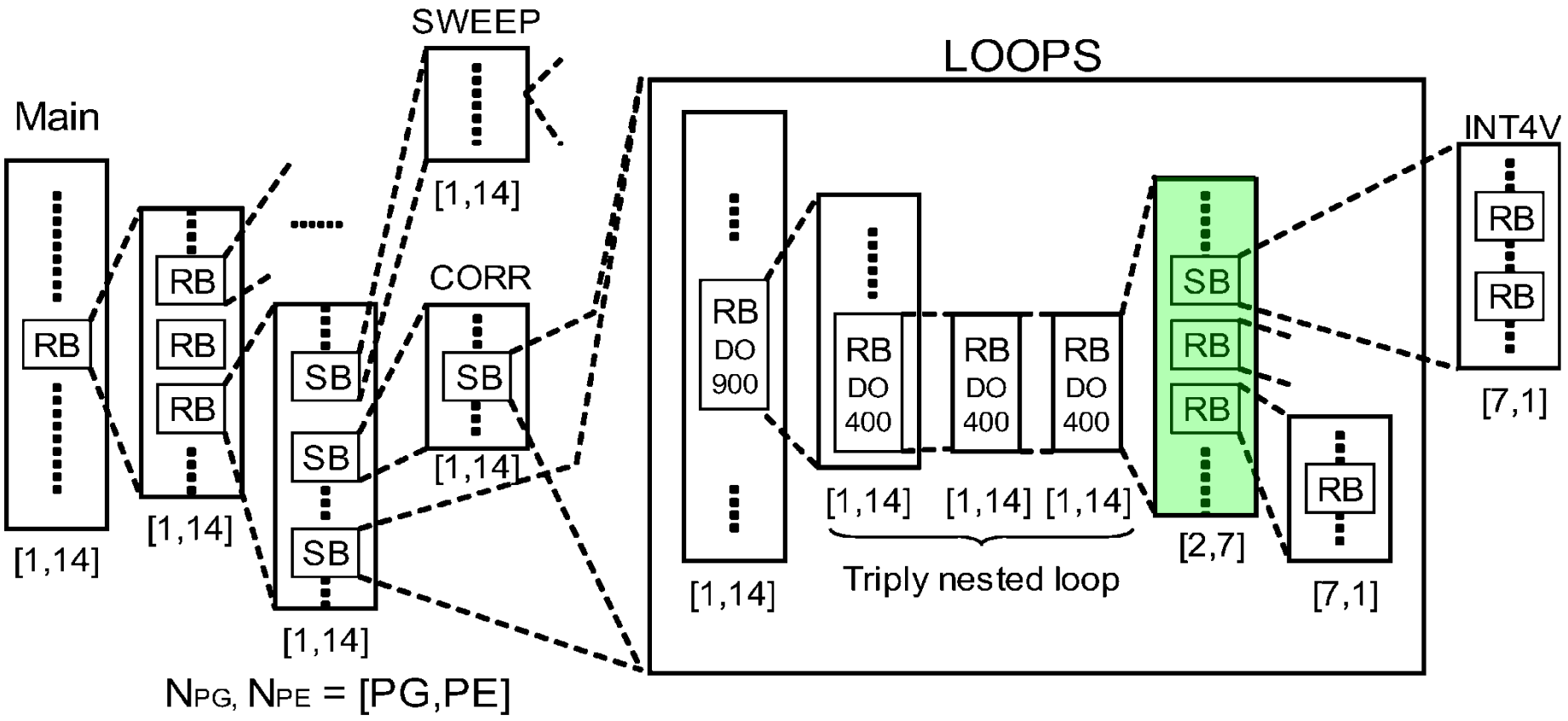
A Macro Flow Graph



A Macro Task Graph

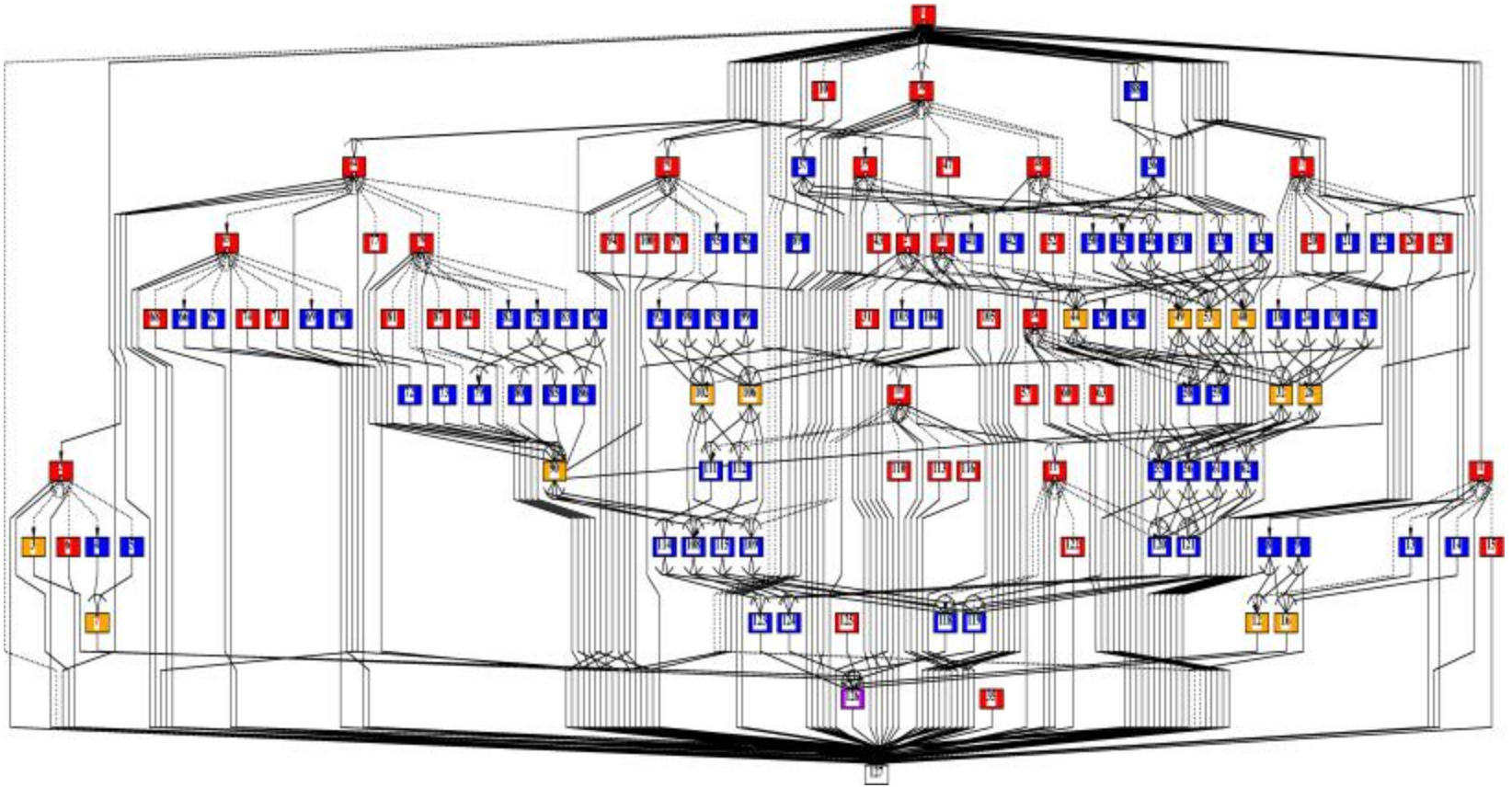
Automatic processor assignment in 103.su2cor

- **Using 14 processors**
  - **Coarse grain parallelization within DO400 of subroutine LOOPS**



MTG of Su2cor-LOOPS-DO400

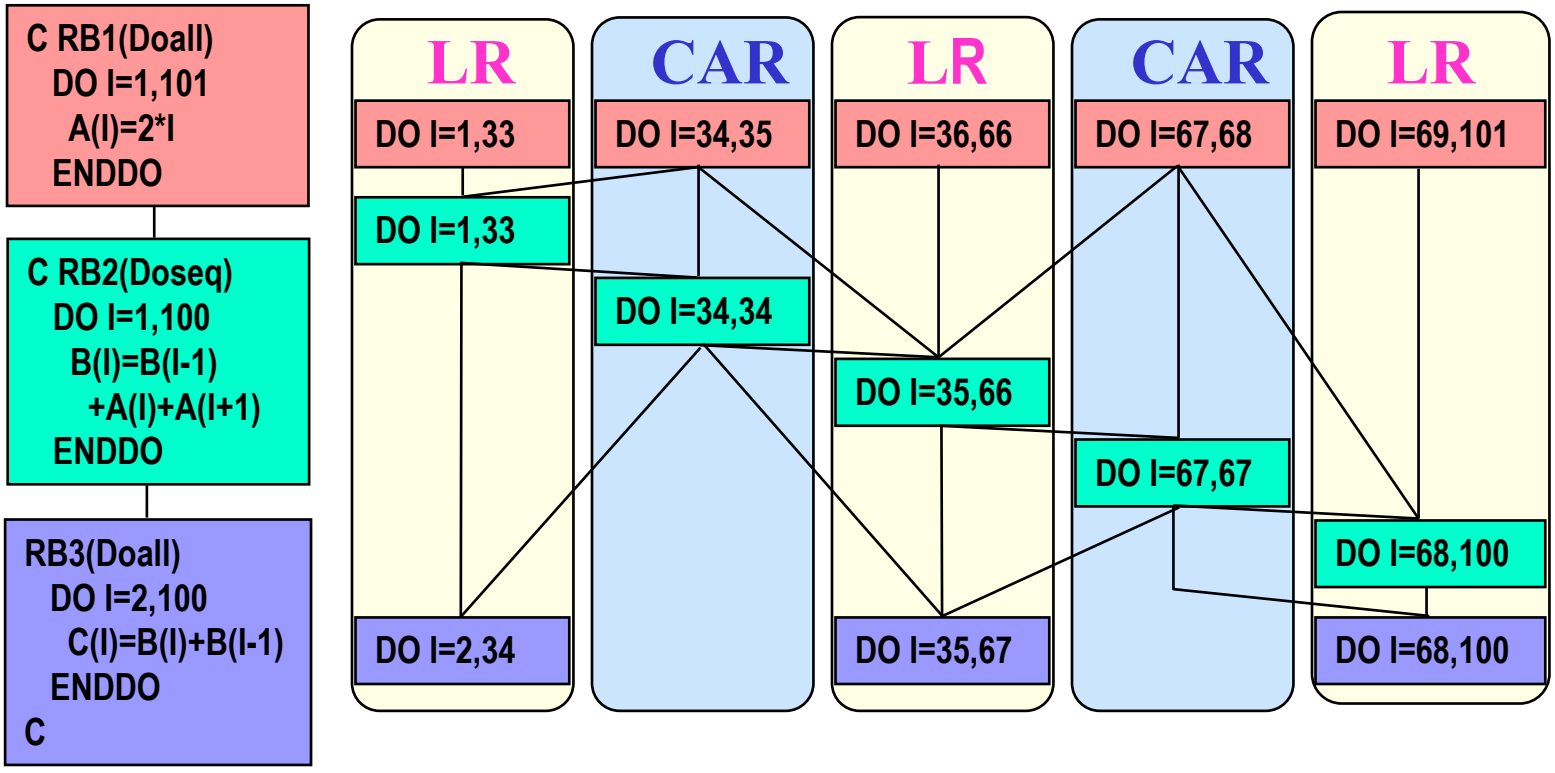
- Coarse grain parallelism PARA_ALD = 4.3



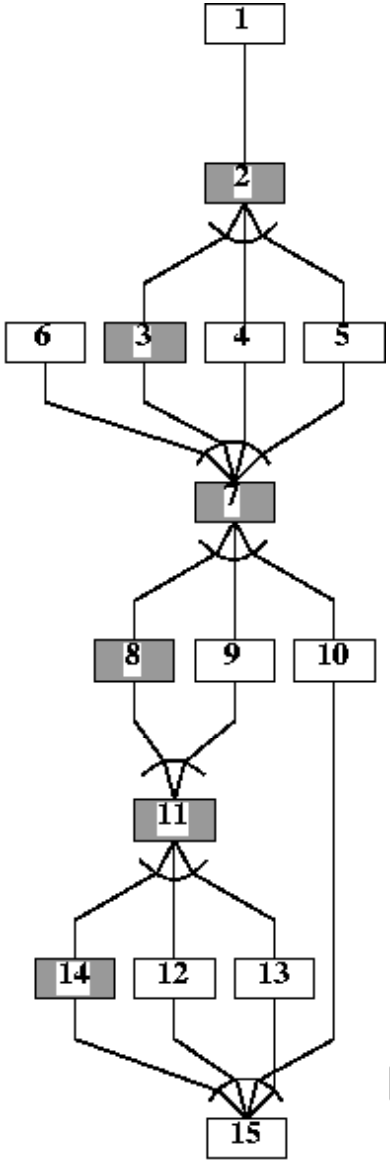
DOALL Sequential LOOP SB BB

Data-Localization
Loop Aligned Decomposition

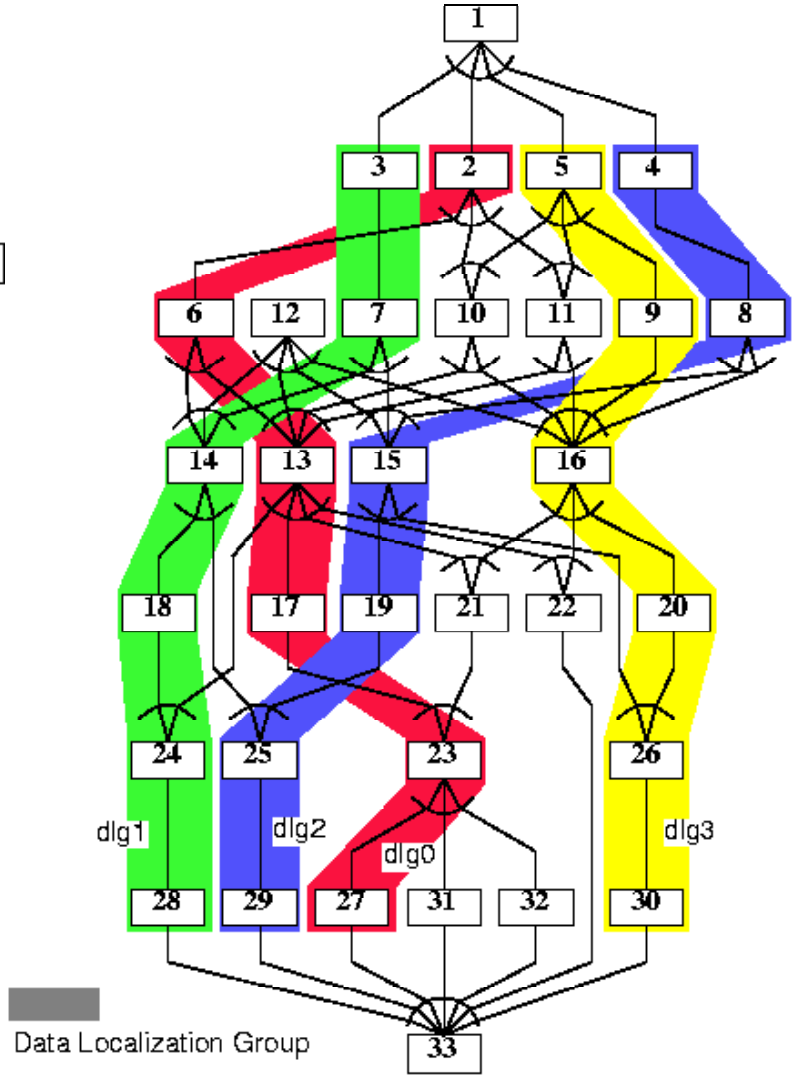
- Decompose multiple loop (Doall and Seq) into CARs and LRs considering inter-loop data dependence.
  - Most data in LR can be passed through LM.
  - LR: Localizable Region, CAR: Commonly Accessed Region



Data Localization



MTG

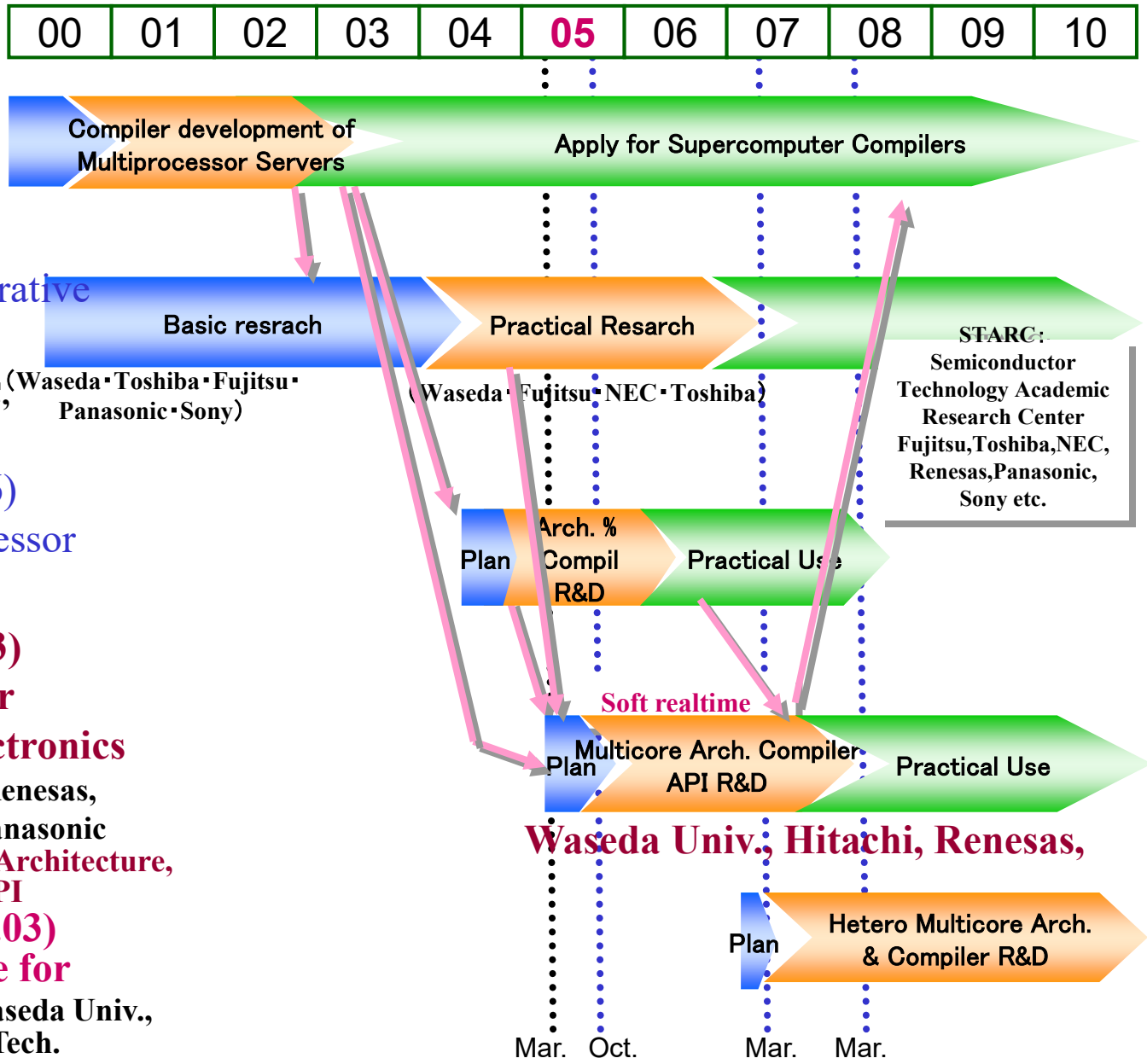


MTG after Division

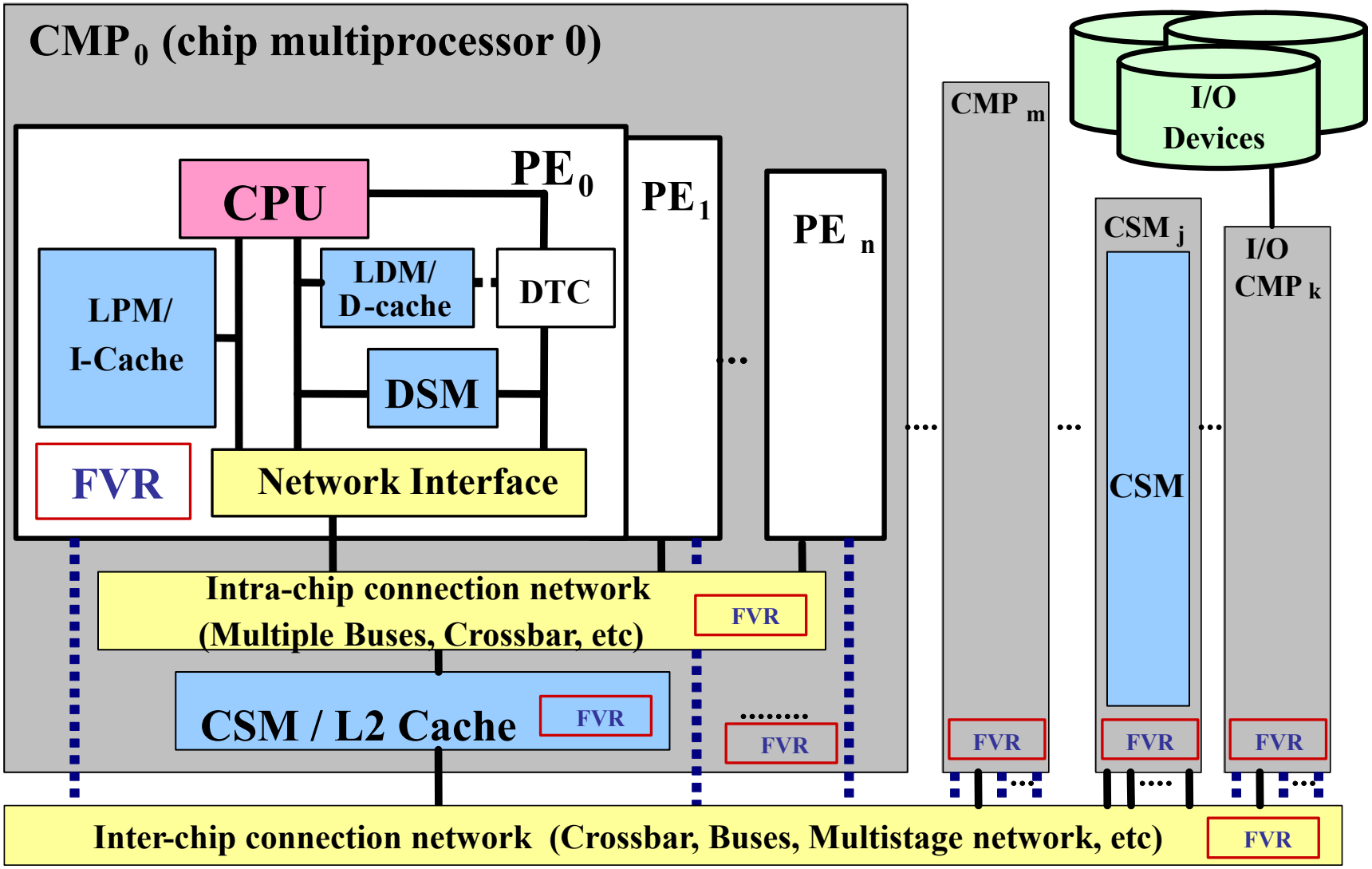
A schedule for two processors

Roadmap of compiler cooperative multicore project

- Millennium Project IT21 NEDO Advanced Parallelizing Compiler
  (Waseda Univ. Fujitsu,Hitachi, JIPDEC,AIST)
- STARC Compiler Cooperative Chip Multiprocessor
  (Waseda Univ., Fujitsu, NEC, Toshiba, Panasonic,Sony)
- NEDO (2004.07-2007.06) Heterogeneous Multiprocessor
  (Waseda Univ., Hitachi)
- **NEDO (2005.06-2008.03) Multicore Technology for Realtime Consumer Electronics**
  - Waseda Univ., Hitachi, Renesas, Fujitsu, NEC, Toshiba, Panasonic
    - ➢Power Saving Multicore Architecture, Parallelizing Compiler,API
- **NEDO (2007.02- 2010.03) Heterogeneous Multicore for Consumer Electronics** Waseda Univ., Hitachi, Renesas, Tokyo Inst, of Tech.



OSCAR Multi-Core Architecture



CSM: central shared mem.

DSM: distributed shared mem.

DTC: Data Transfer Controller

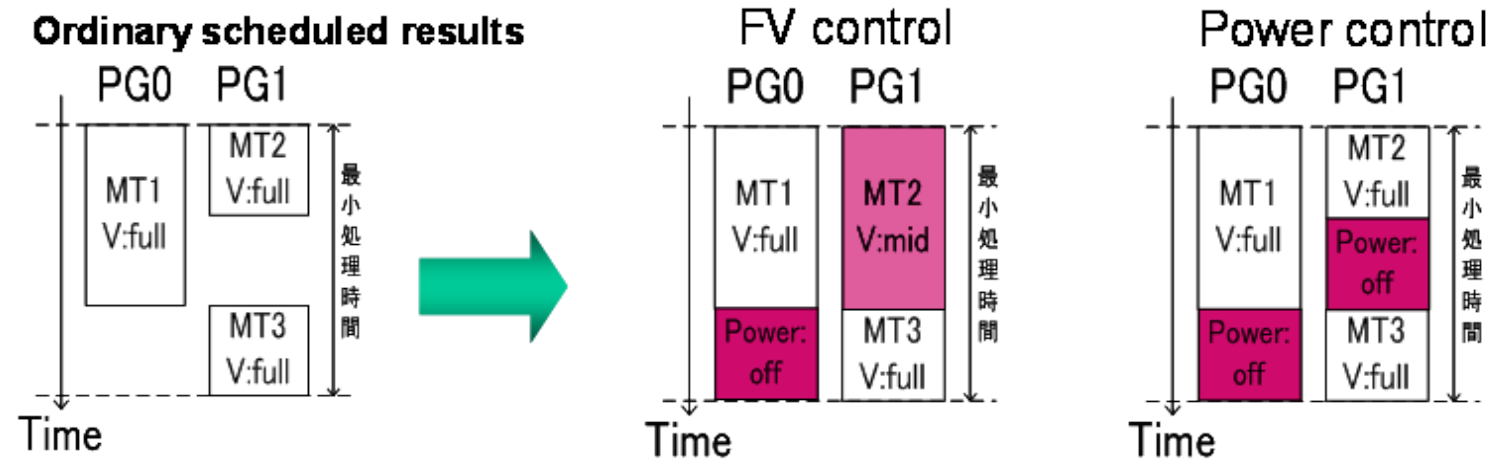
LDM : local data mem.

LPM : local program mem.

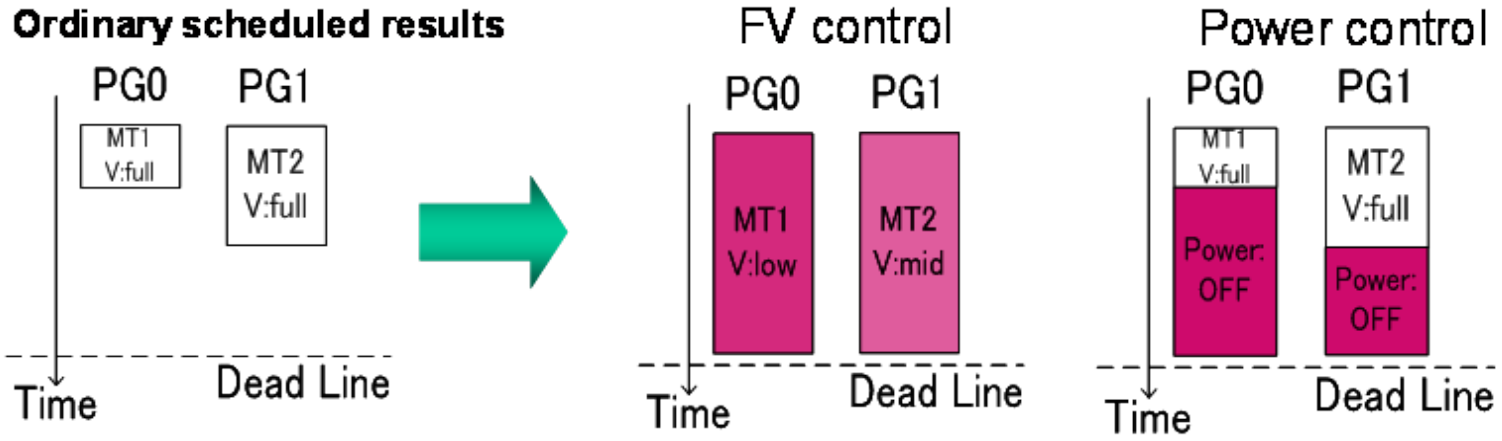
FVR: frequency / voltage control register

Power Reduction by Power Supply, Clock Frequency and Voltage Control by OSCAR Compiler

- Shortest execution time mode



- Realtime processing mode with dead line constraints



METI/NEDO National Project

Multi-core for Real-time Consumer Electronics

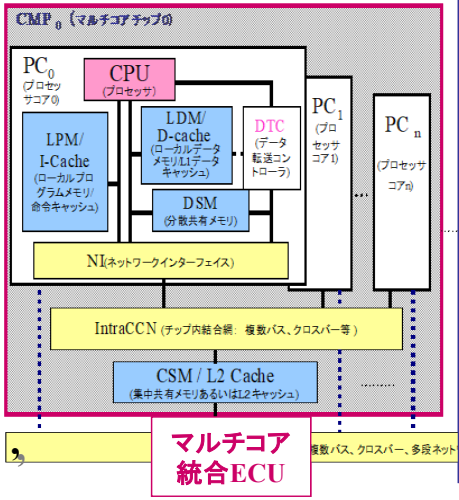
<Goal> R&D of compiler cooperative multi-core processor technology for consumer electronics like Mobile phones, Games, DVD, Digital TV, Car navigation systems.

<Period> From July 2005 to March 2008 (2005.7～2008.3)**

<Features>

- Good cost performance
- Short hardware and software development periods
- Low power consumption
- Scalable performance improvement with the advancement of semiconductor
- Use of the same parallelizing compiler for multi-cores from different vendors using newly developed API

API : Application Programming Interface



新マルチコアプロセッサ

- 高性能
- 低消費電力
- 短HW/SW開発期間
- 各チップ間でアプリケーション共用可
- 高信頼性
- 半導体集積度と共に性能向上

開発マルチコアチップは情報家電へ

**Hitachi, Renesas, Fujitsu, Toshiba, Panasonic, NEC

Multicore Program Development Using OSCAR API V2.0

Sequential Application Program in Fortran or C
(Consumer Electronics, Automobiles, Medical, Scientific computation, etc.)

Homogeneous

Hetero

Manual parallelization / power reduction

Accelerator Compiler/ User
Add "hint" directives before a loop or a function to specify it is executable by the accelerator with how many clocks

Waseda OSCAR Parallelizing Compiler
- Coarse grain task parallelization
- Data Localization
- DMAC data transfer
- Power reduction using DVFS, Clock/ Power gating

OSCAR API for Homogeneous and/or Heterogeneous Multicores and manycores
Directives for thread generation, memory, data transfer using DMA, power managements

Parallelized API F or C program

Proc0
Code with directives
Thread 0

Proc1
Code with directives
Thread 1

Accelerator 1
Code

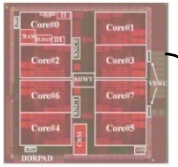
Accelerator 2
Code

Low Power Homogeneous Multicore Code Generation
API Analyzer | Existing sequential compiler

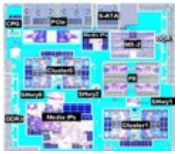
Low Power Heterogeneous Multicore Code Generation
API Analyzer (Available from Waseda) | Existing sequential compiler

Server Code Generation
OpenMP Compiler

Generation of parallel machine codes using sequential compilers



Homegeneous Multicore s from Vendor A (SMP servers)



Heterogeneous Multicores from Vendor B

Shred memory servers

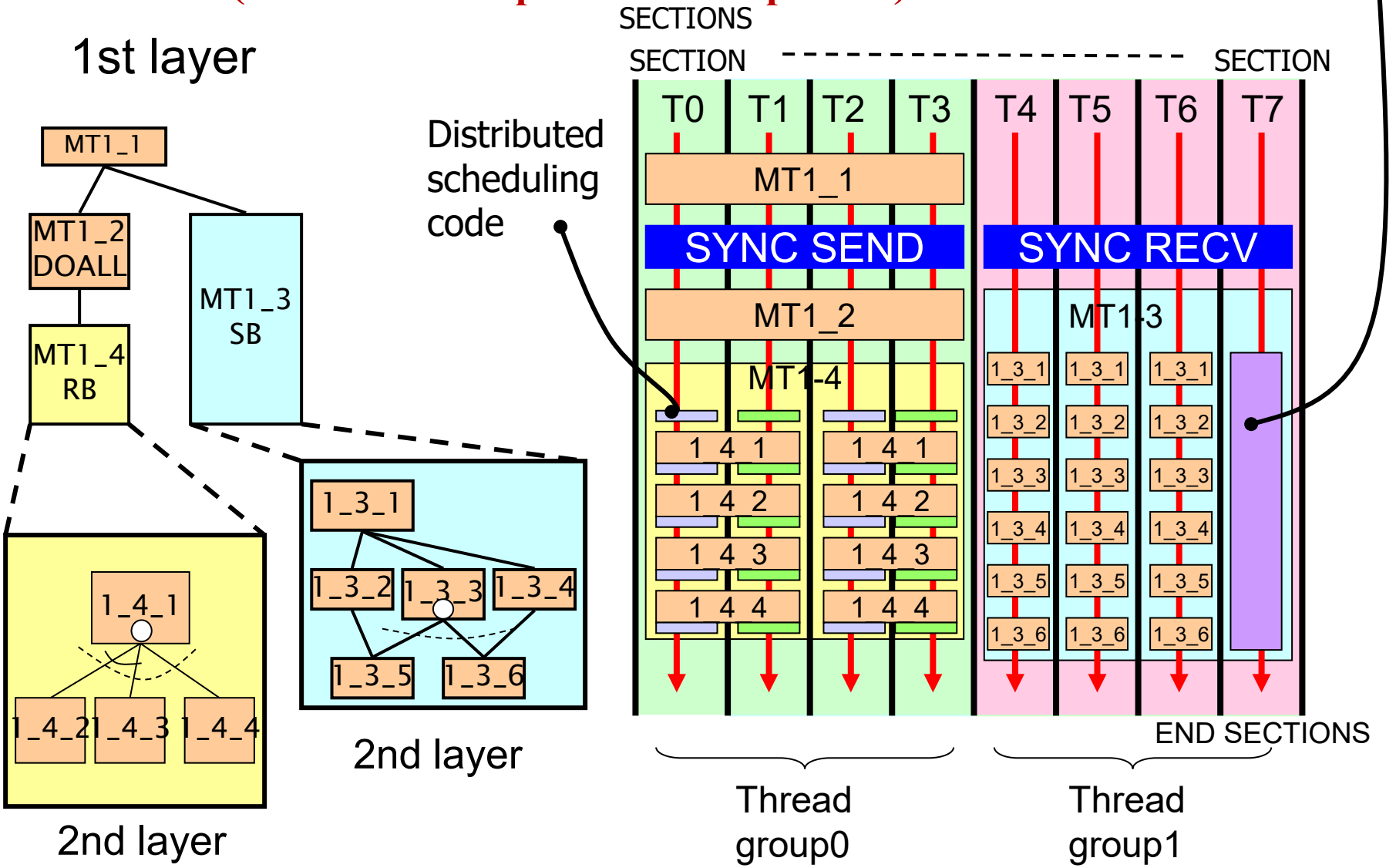
Executable on various multicores

Hitachi, Renesas, NEC, Fujitsu, Toshiba, Denso, Olympus, Mitsubishi, Esol, Cats, Gaio, 3 univ.

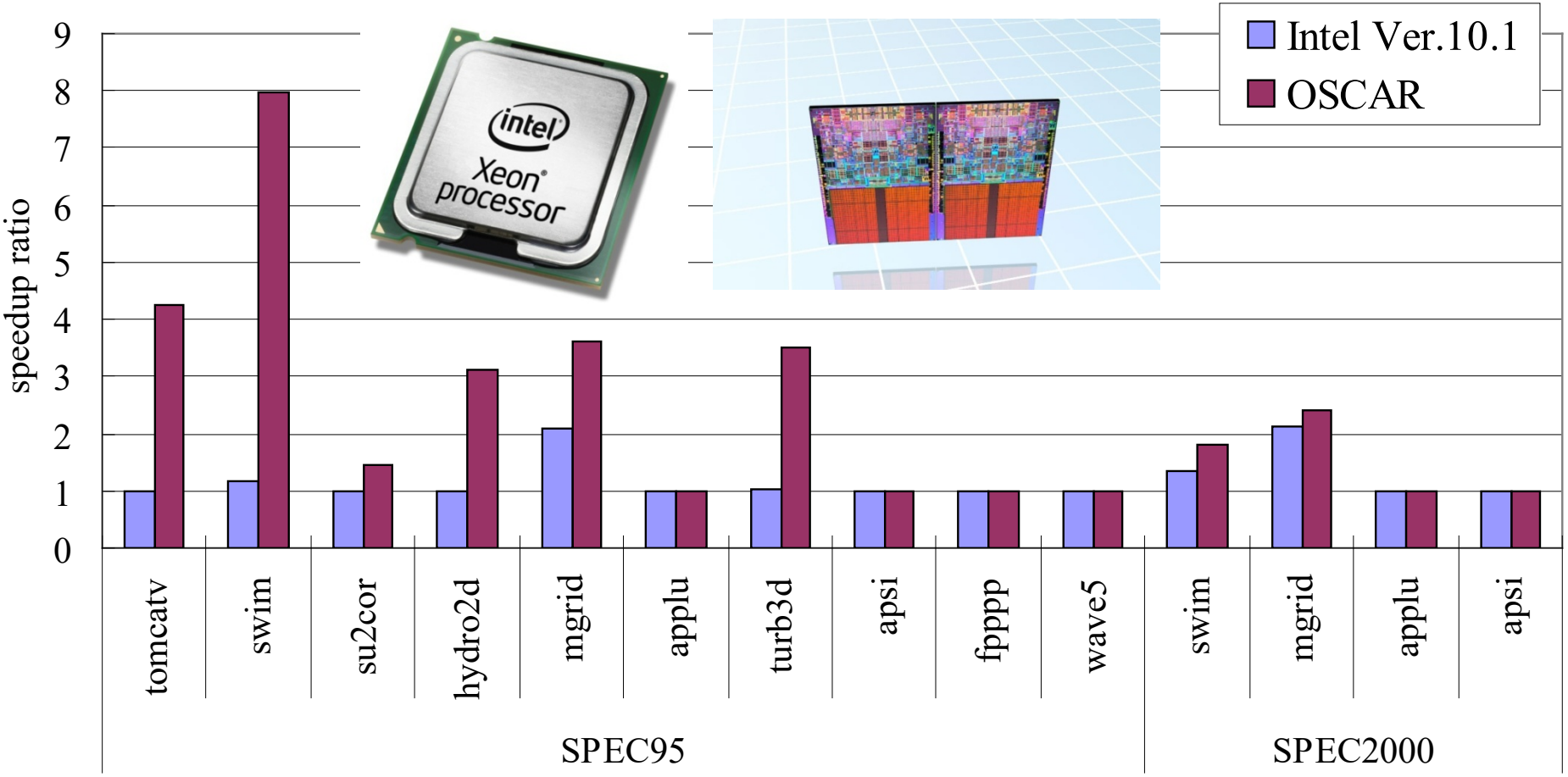
OSCAR: Optimally Scheduled Advanced Multiprocessor
API : Application Program Interface

Image of Generated Multigrain Parallelized Code using the developed Multicore API

(The API is compatible with OpenMP)

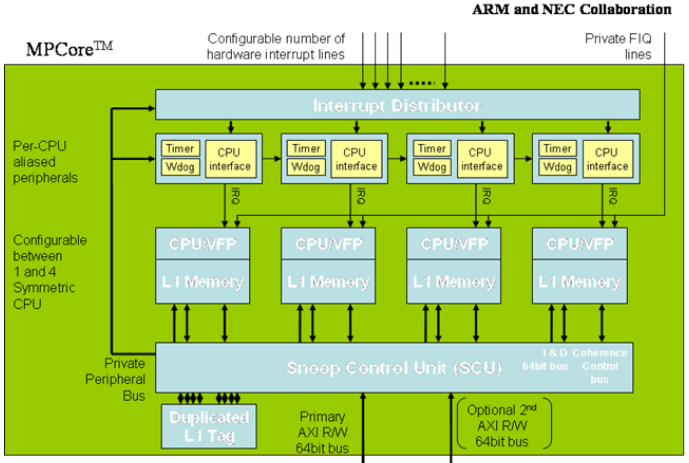


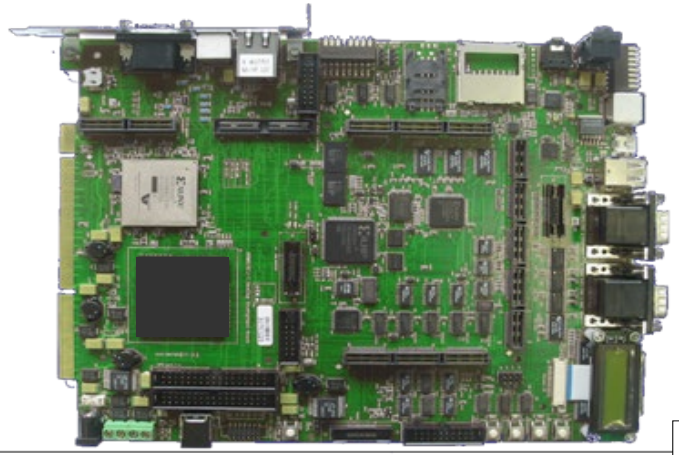
Performance of OSCAR Compiler Using the Multicore API on Intel Quad-core Xeon

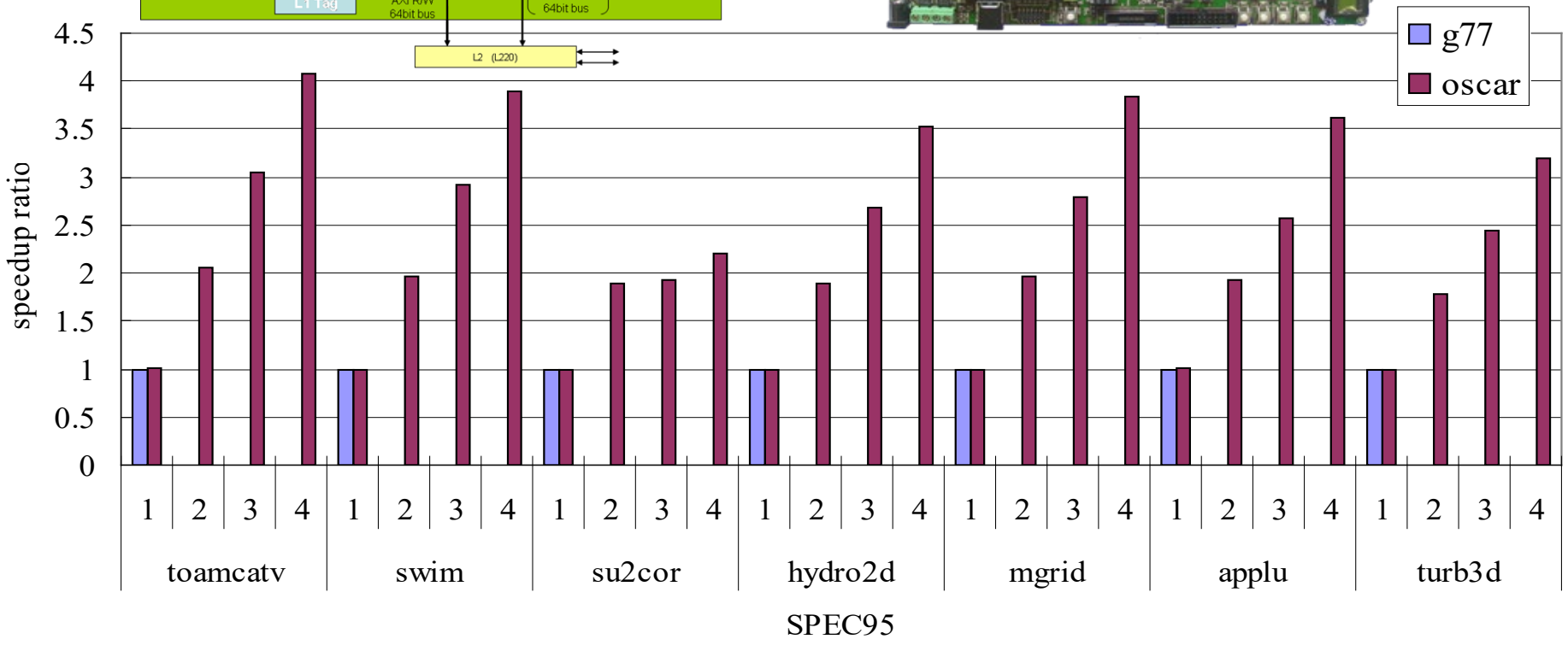


- **OSCAR Compiler gives us 2.09 times speedup on the average against Intel Compiler ver.10.1**

NEC/ARM MPCore Embedded 4 core SMP



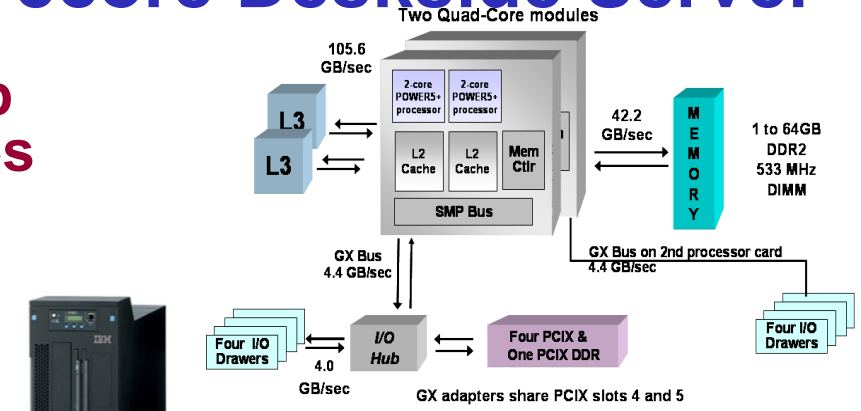




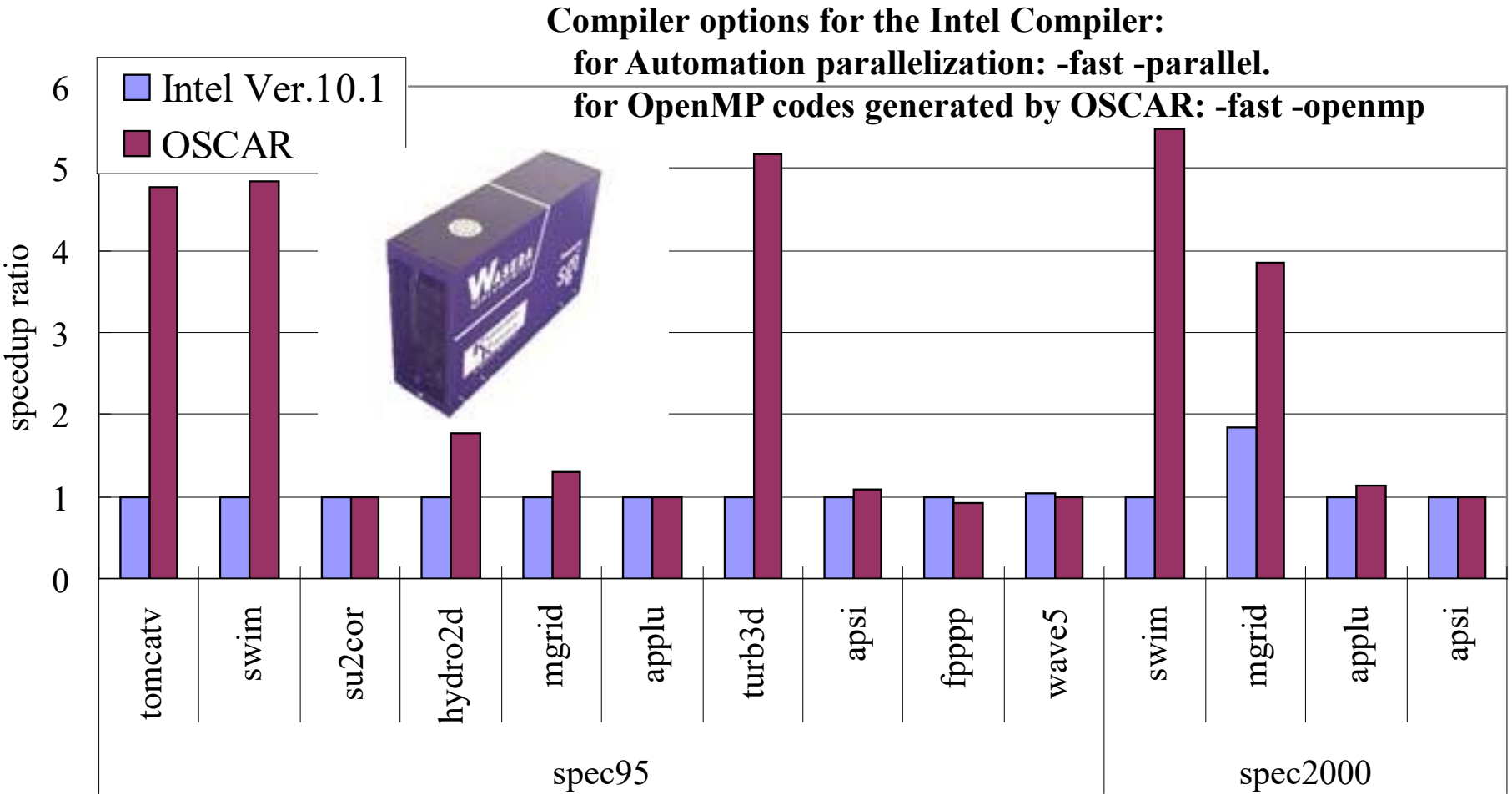
3.48 times speedup by OSCAR compiler against sequential processing

Performance OSCAR Multigrain Parallelizing Compiler on a IBM p550q 8core Deskside Server

- 2.7 times speedup against loop parallelizing compiler on 8 cores

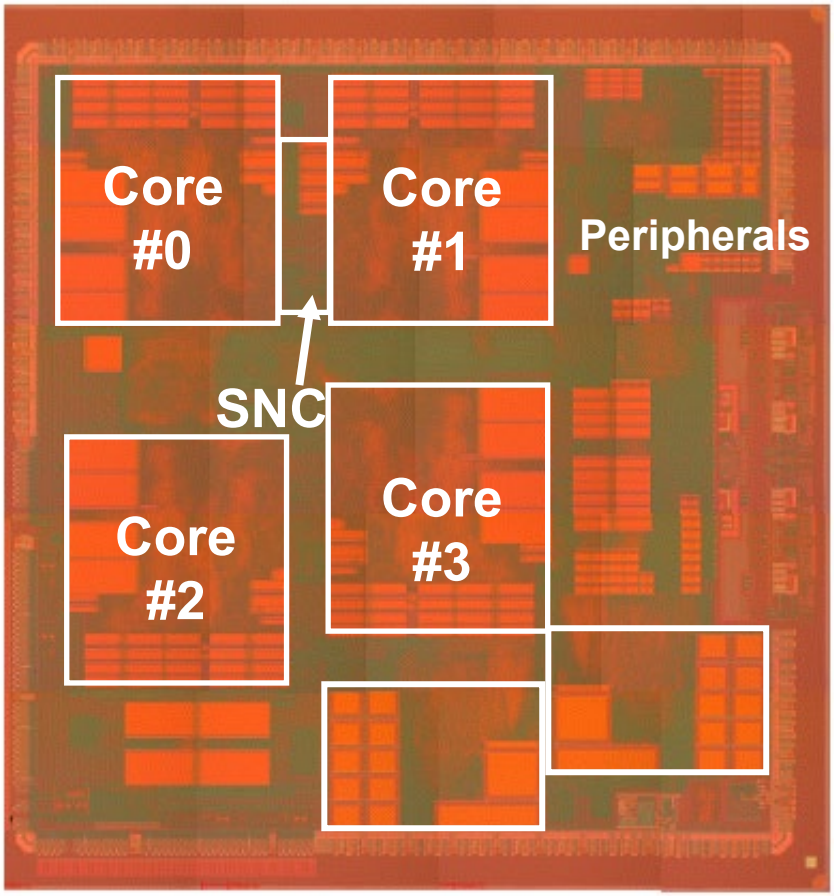


Performance of OSCAR compiler on 16 cores SGI Altix 450 Montvale server



- **OSCAR compiler gave us 2.32 times speedup against Intel Fortran Itanium Compiler revision 10.1**

Chip Overview

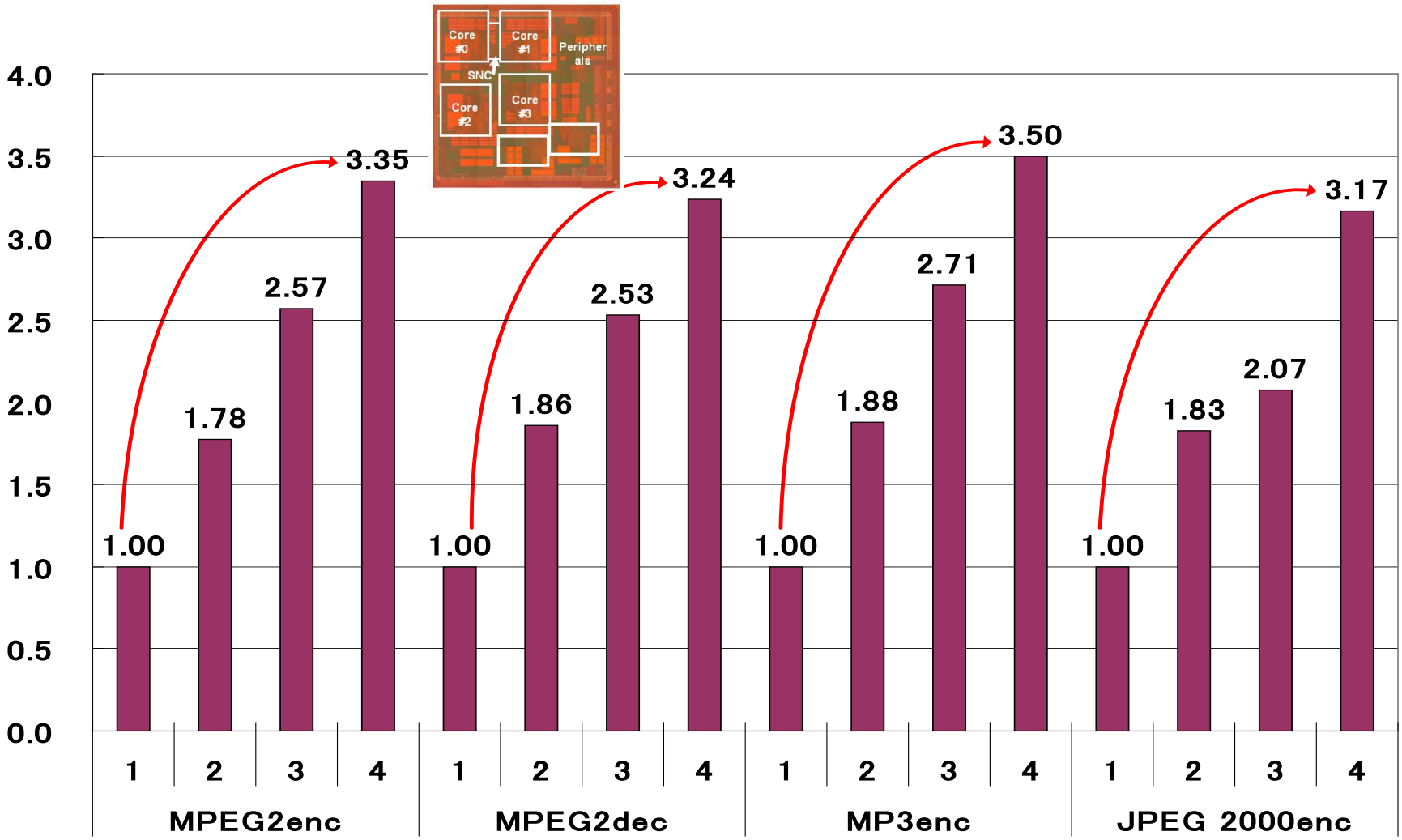


SH4A Multicore SoC Chip

Process Technology	90nm, 8-layer, triple-Vth, CMOS
Chip Size	97.6mm^2 (9.88mm x 9.88mm)
Supply Voltage	1.0V (internal), 1.8/3.3V (I/O)
Power Consumption	0.6 mW/MHz/CPU @ 600MHz (90nm G)
Clock Frequency	600MHz
CPU Performance	4320 MIPS (Dhrystone 2.1)
FPU Performance	16.8 GFLOPS
I/D Cache	32KB 4way set-associative (each)
ILRAM/OLRAM	8KB/16KB (each CPU)
URAM	128KB (each CPU)
Package	FCBGA 554pin, 29mm x 29mm

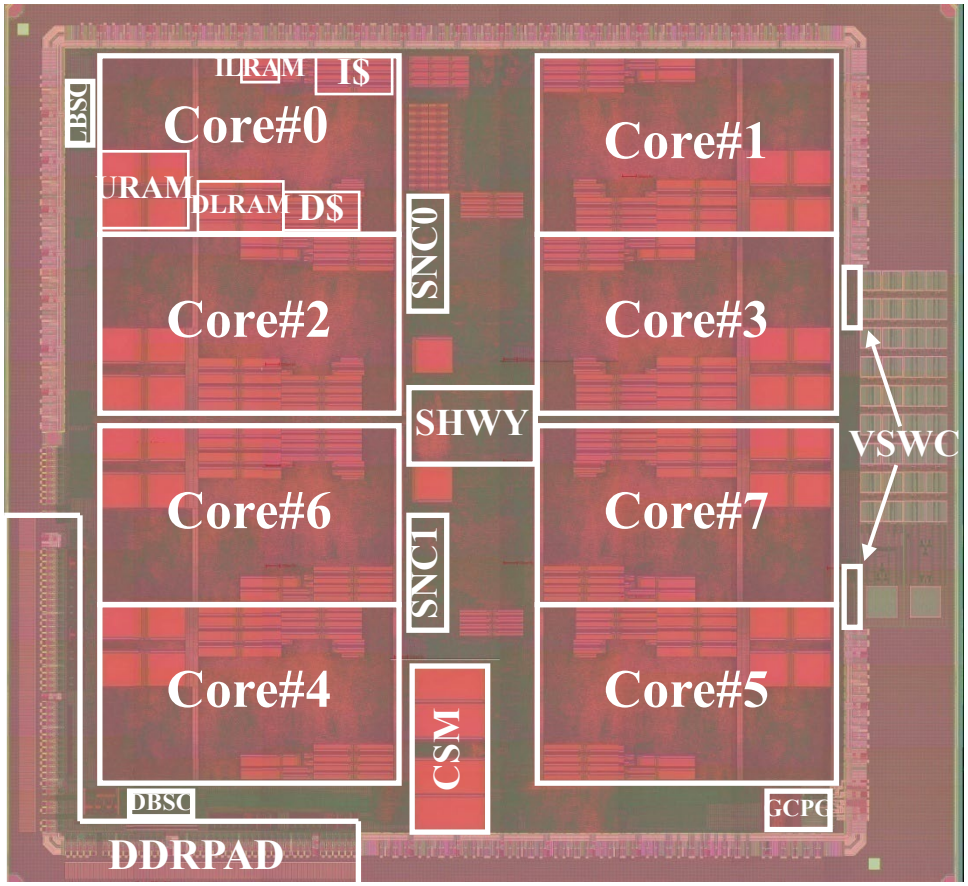
ISSCC07 Paper No.5.3, Y. Yoshida, et al., "A 4320MIPS Four-Processor Core SMP/AMP with Individually Managed Clock Frequency for Low Power Consumption"

Performance of OSCAR Compiler Using the Developed API on 4 core (SH4A) OSCAR Type Multicore



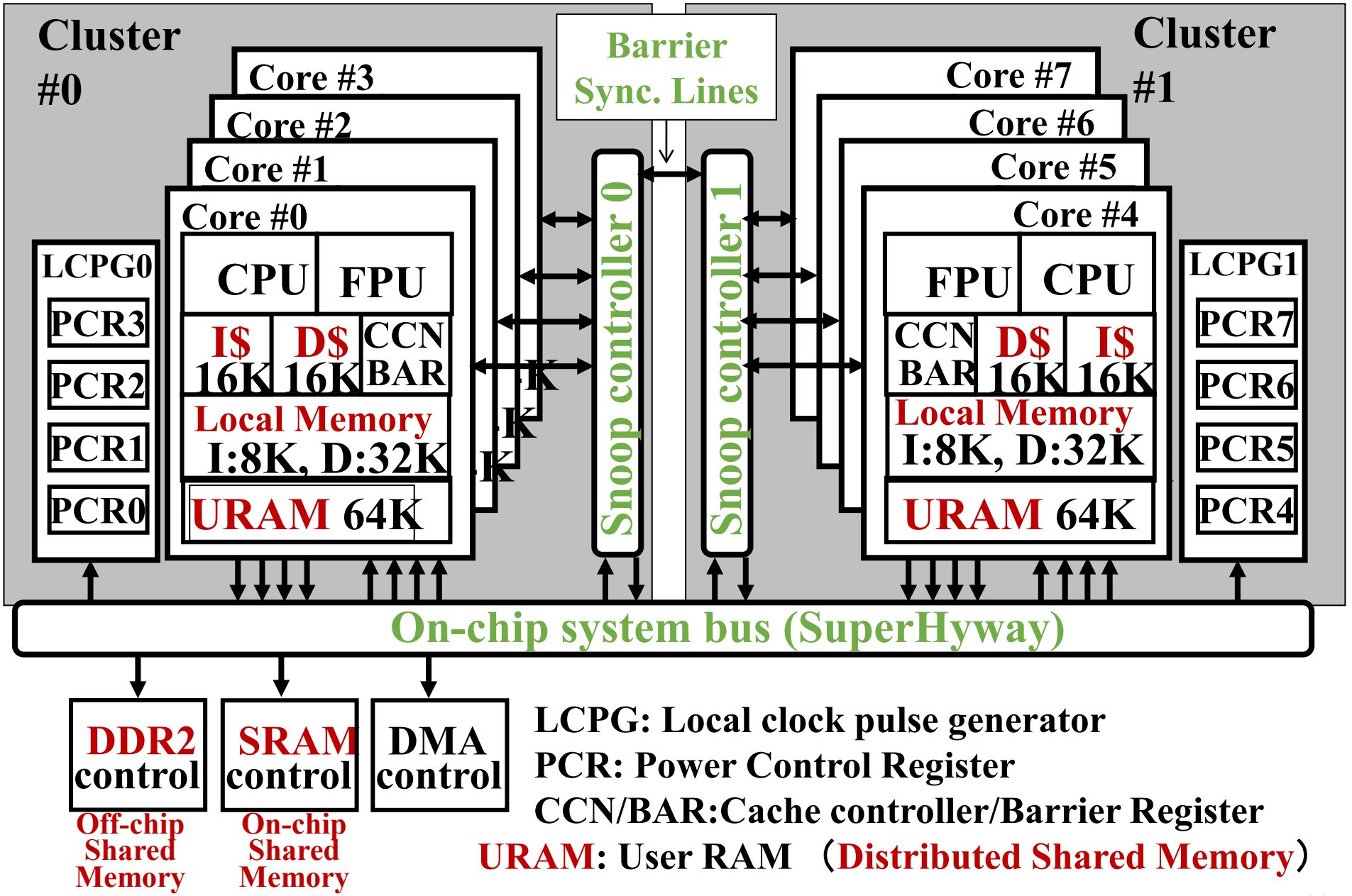
3.31 times speedup on the average for 4cores against 1core

RP2 Chip Photo and Specifications



Process Technology	90nm, 8-layer, triple-Vth, CMOS
Chip Size	104.8mm^2 (10.61mm x 9.88mm)
CPU Core Size	6.6mm^2 (3.36mm x 1.96mm)
Supply Voltage	1.0V–1.4V (internal), 1.8/3.3V (I/O)
Power Domains	17 (8 CPUs, 8 URAMs, common)

8 Core RP2 Chip Block Diagram

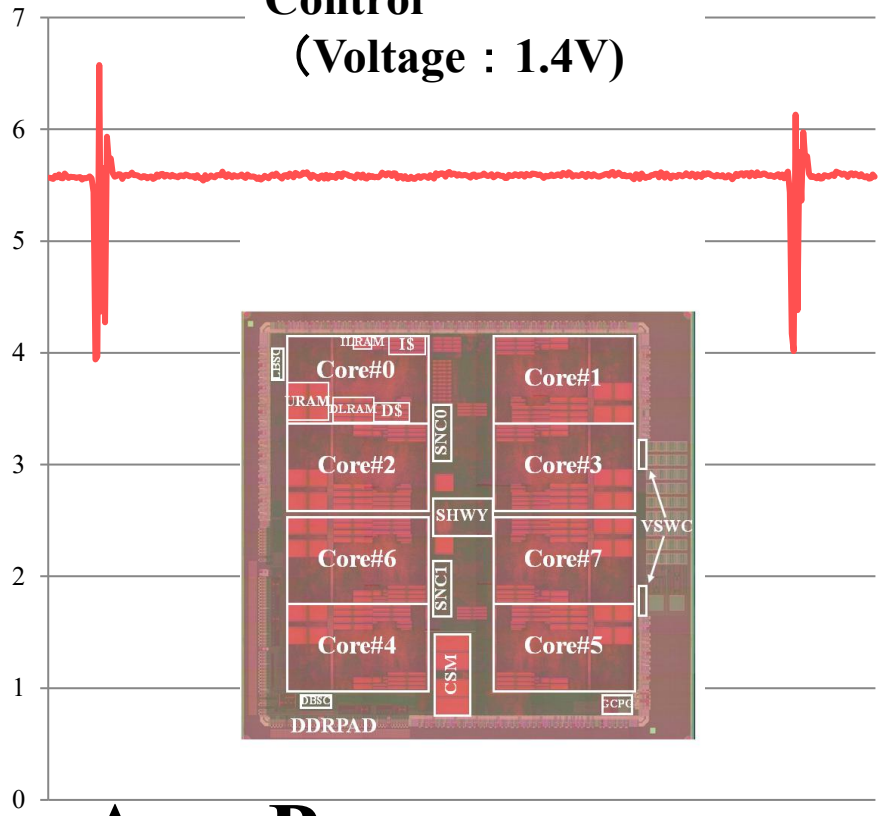


LCPG: Local clock pulse generator
PCR: Power Control Register
CCN/BAR:Cache controller/Barrier Register
URAM: User RAM （Distributed Shared Memory）

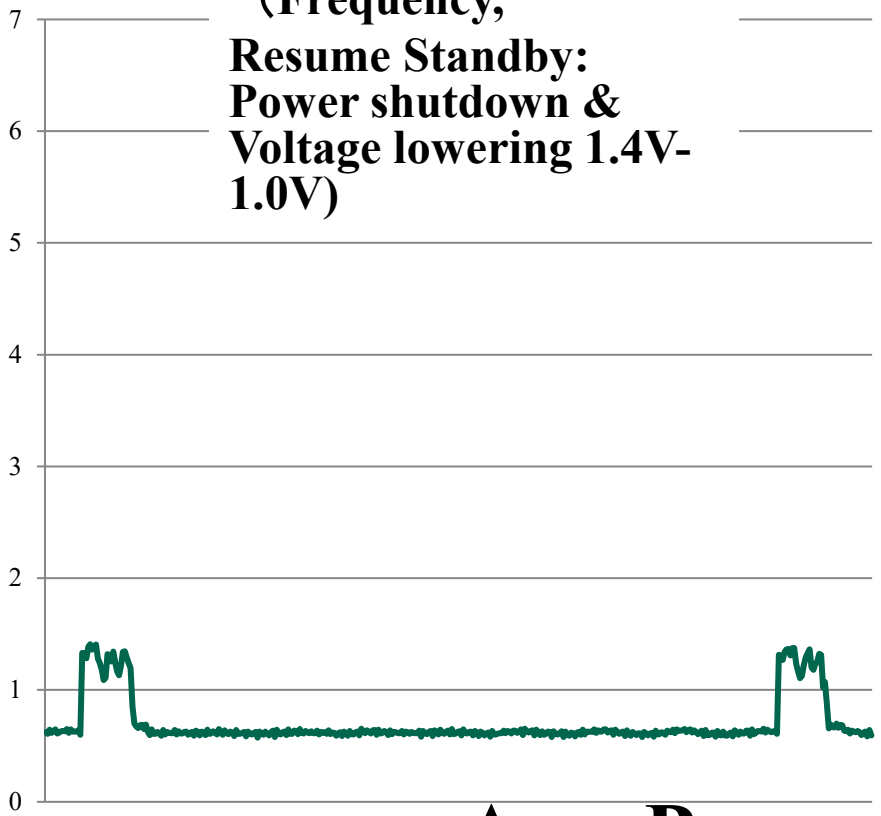
Power Reduction by OSCAR Parallelizing Compiler for Secure Audio Encoding

AAC Encoding + AES Encryption with 8 CPU cores

Without Power Control (Voltage : 1.4V)



With Power Control (Frequency, Resume Standby: Power shutdown & Voltage lowering 1.4V-1.0V)



Avg. Power 5.68 [W]

88.3% Power Reduction

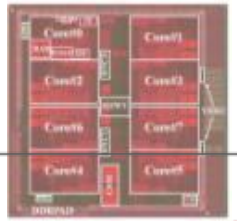
Avg. Power 0.67 [W]

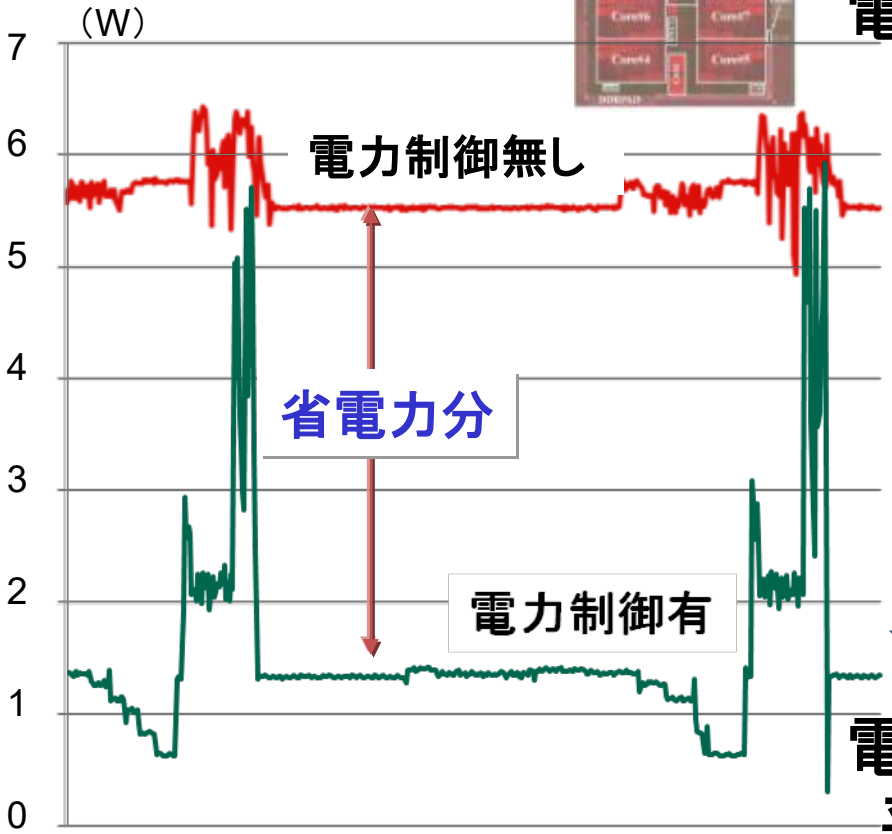
太陽光電力で動作する情報機器

コンピュータの消費電力をHW&SW協調で低減。電源喪失時でも動作することが可能。

リアルタイムMPEG2デコードを、8コアホモジニアス
マルチコアRP2上で、消費電力1/4に削減

世界唯一の差別化技術



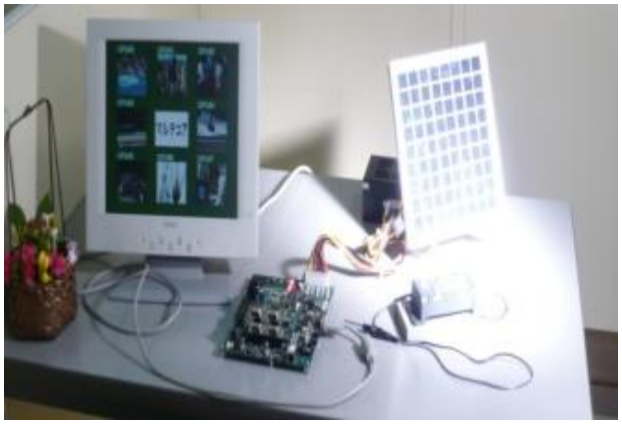


電力制御無し
平均電力
5.73 [W]

電力を
ソフトで
1/4に
削減

電力制御有
平均電力
1.52 [W]

周波数/電圧・電源遮断制御



太陽電池で駆動可

総合科学技術会議（平成20年4月10日）での NEDOリアルタイム情報家電用マルチコアチップ（笠原リーダー）・デモの様子

http://www8.cao.go.jp/cstp/gaiyo/honkaigi/74index.html

第74回総合科学技術会議【平成20年4月10日】

第74回総合科学技術会議の様子(1)

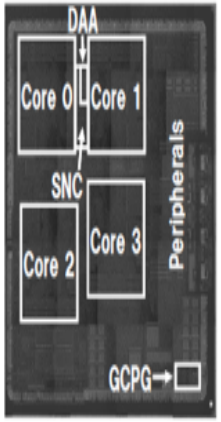
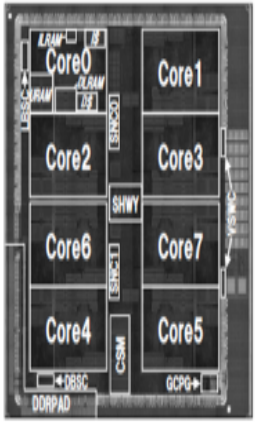
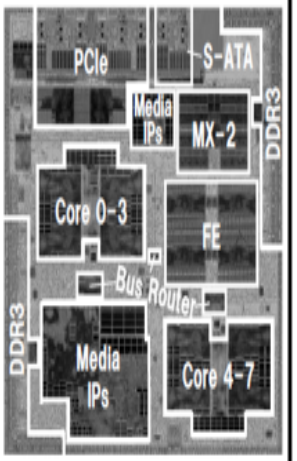
第74回総合科学技術会議の様子(2)

第74回総合科学技術会議の様子(3)

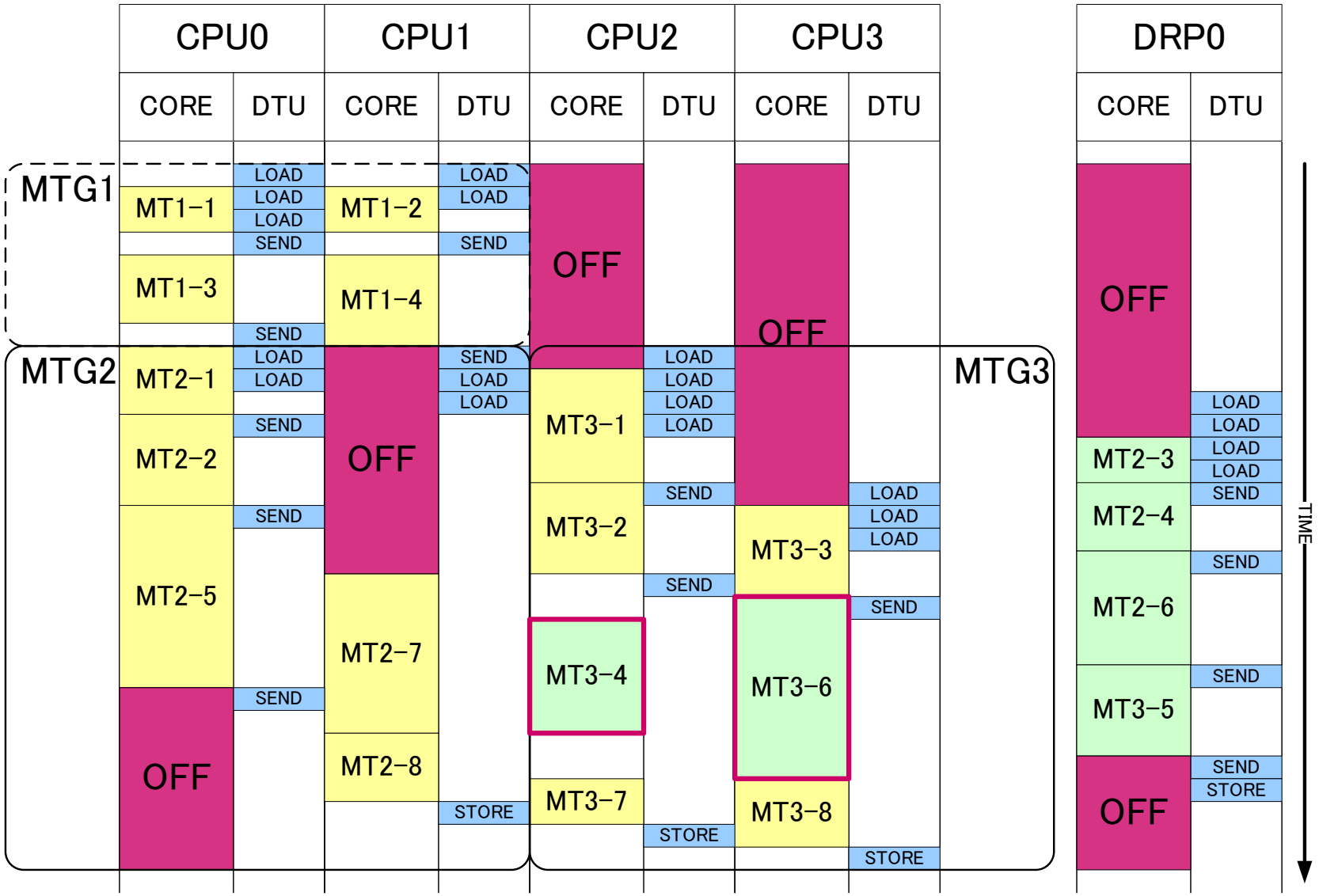
第74回総合科学技術会議の様子(4)

1985年よりコンパイラ（ソフト）・アーキテクチャ（ハード）協調設計マルチプロセッサの研究

4 core multicore RP1 (2007), 8 core multicore RP2 (2008) and 15 core Heterogeneous multicore RPX (2010) developed in NEDO Projects with Hitachi and Renesas

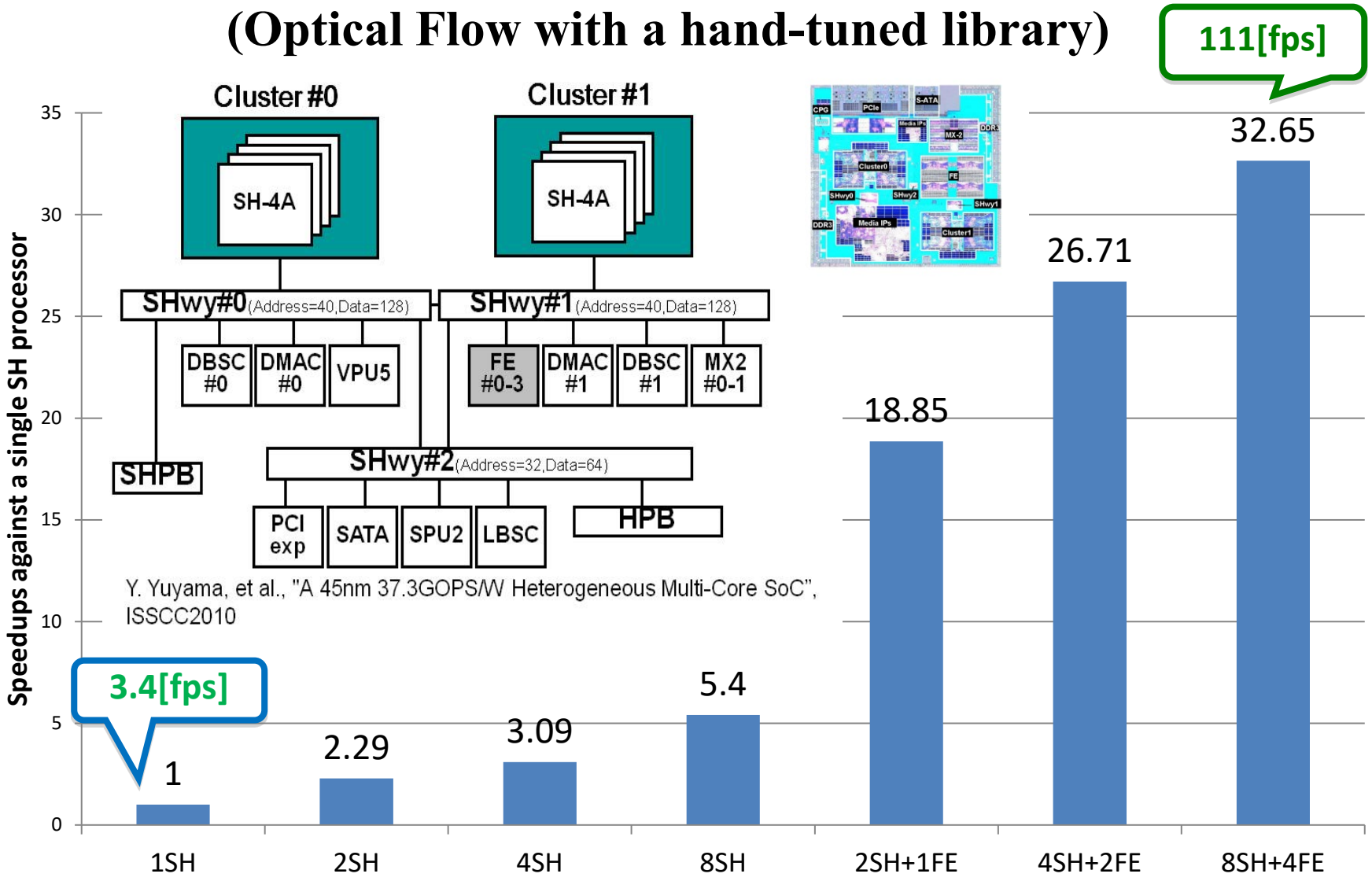
RP-1 (ISSCC2007 #5.3)	*RP-2* (ISSCC2008 #4.5)	*RP-X* (ISSCC2010 #5.3)
		
90nm, 8-layer, triple-Vth, CMOS	90nm, 8-layer, triple-Vth, CMOS	45nm, 8-layer, triple-Vth, CMOS
97.6 mm^2 (9.88 x 9.88 mm)	104.8 mm^2 (10.61 x 9.88 mm)	153.8 mm^2 (12.4 x 12.4 mm)
1.0V (internal), 1.8/3.3V (I/O)	1.0-1.4V (internal), 1.8/3.3V (I/O)	1.0-1.2V (internal), 1.2-3.3V (I/O)
600MHz ,4.32 GIPS,16.8 GFLOPS	600MHz , 8.64 GIPS, 33.6 GFLOPS	648MHz, 13.7GIPS, 115GOPS, 36.2GFLOPS
11.4 GOPS/W (32b換算)	18.3 GOPS/W (32b換算)	37.3 GOPS/W (32b換算)

An Image of Static Schedule for Heterogeneous Multi-core with Data Transfer Overlapping and Power Control



33 Times Speedup Using OSCAR Compiler and OSCAR API on RP-X

(Optical Flow with a hand-tuned library)



実施場所：グリーン・コンピューティング・システム研究開発センター

2011年4月13日竣工，2011年5月13日開所

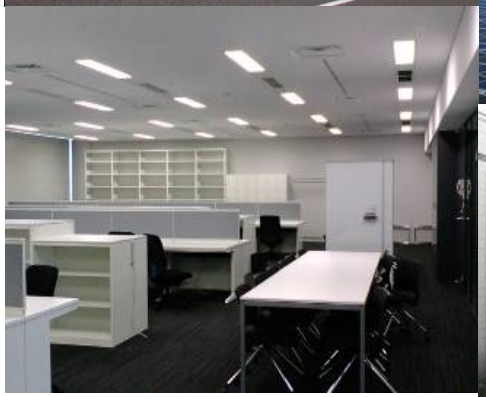
経済産業省「2009年度産業技術研究開発施設整備費補助金」
先端イノベーション拠点整備事業

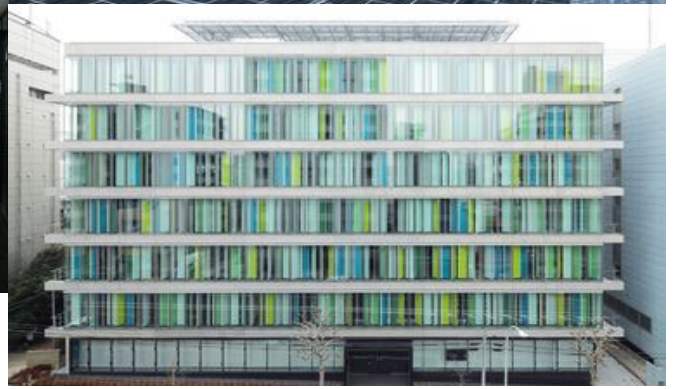
＜目標＞
太陽電池で駆動可能で
冷却ファンが不要な
超低消費電力・高性能マルチコア/
メニーコアプロセッサ*のハードウェア、
ソフトウェア、応用技術の研究開発

*1チップ上に多数のプロセッサコアを
集積する次世代マルチコアプロセッサ

＜産学連携＞
日立,富士通, ルネサス,NEC, トヨタ,
デンソー，オリンパス,NSITEX、三菱電機,
オスカーテクノロジ等

＜波及効果＞
超低消費電力メニーコア
- CO_2排出量削減
- サーバ国際競争力強化
- 我が国の産業利益を支える
  情報家電,自動車等の高付加価値化





笠原・木村研究室：アドバンストマルチコアプロセッサ研究所

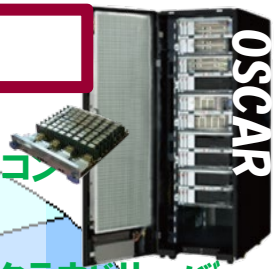
制御

車載（エンジン制御・自動運転Deep Learning・ADAS・MATLAB/Simulink自動並列化）デンソー，ルネサス,NEC

交通シミュレーション・信号制御　NTTデータ・日立

環境を守る

命を守る



グリーンスパコン

グリーンクラウドサーバ

アドバンストマルチコアプロセッサ研究所

OSCARマルチコア/メニーコア
&コンパイラ　オスカー

OSCAR
Many-core
OS
API

産業

生活

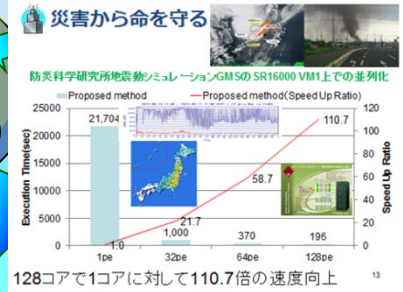
災害

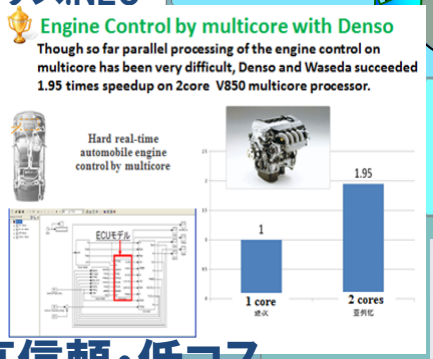
医療

ホーム・産業系メニーコア

サーバ系メニーコア

デスクトップスパコン





高信頼・低コスト・ソフト開発

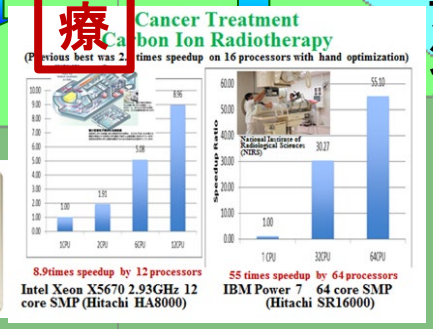
FA　三菱

カプセル内視鏡オリンパス

スマートフォン

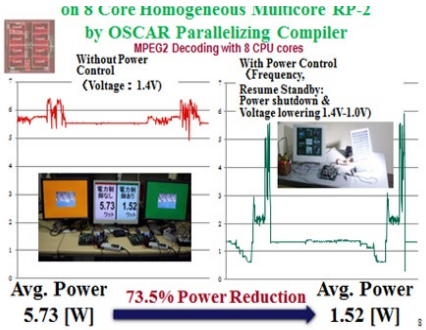
カメラ

太陽電池駆動・週1以下の充電



医用画像処理等専用サーバ（医療・重粒子線照射計画）日立

首都圏直下型地震火災延焼、
住民避難指示



新幹線車体設計・ディープラーニング・日立

企業　持続的高付加価値製品の開発　大学

高速化

低消費電力化

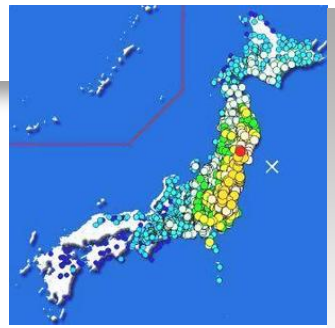
産業競争力を守る

グリーンコンピューティングセンターでの国際イベント

The 25th International Workshop on Languages and Compilers for Parallel Computing (LCPC2012), September 11-13, 2012

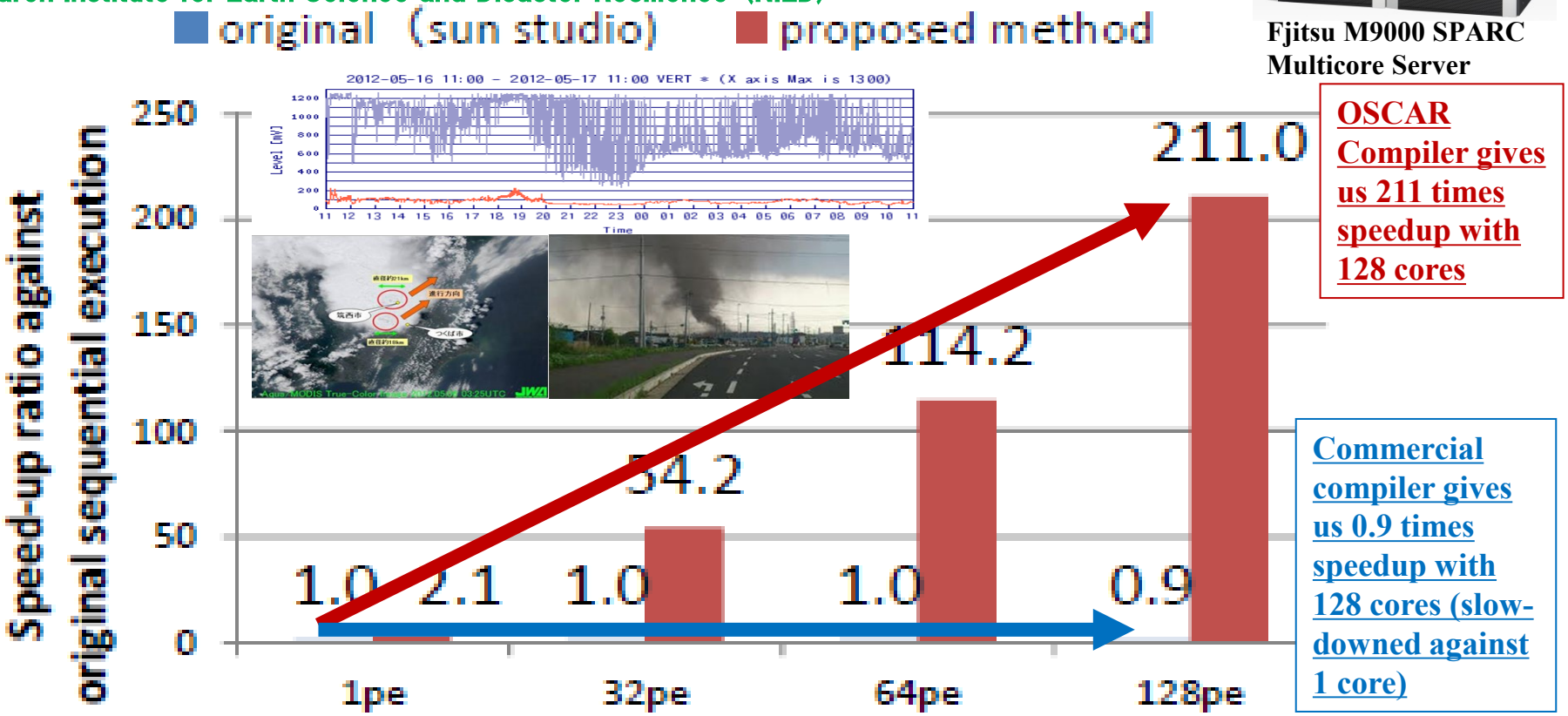
Parallel Soft is important for scalable performance of multicore (LCPC2015)

- Just more cores don't give us speedup
- Development cost and period of parallel software are getting a bottleneck of development of embedded systems, eg. IoT, Automobile



Fjitsu M9000 SPARC Multicore Server

Earthquake wave propagation simulation GMS developed by National Research Institute for Earth Science and Disaster Resilience (NIED)



OSCAR Compiler gives us 211 times speedup with 128 cores

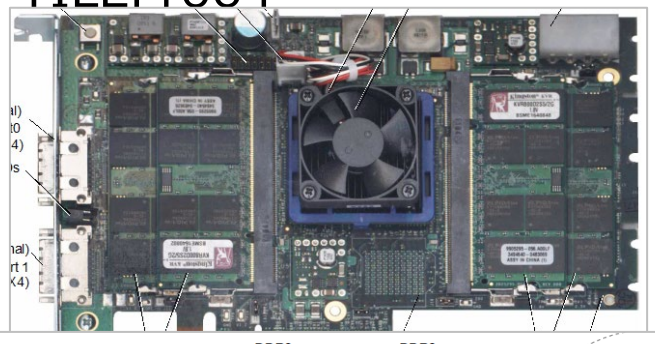
Commercial compiler gives us 0.9 times speedup with 128 cores (slow-downed against 1 core)

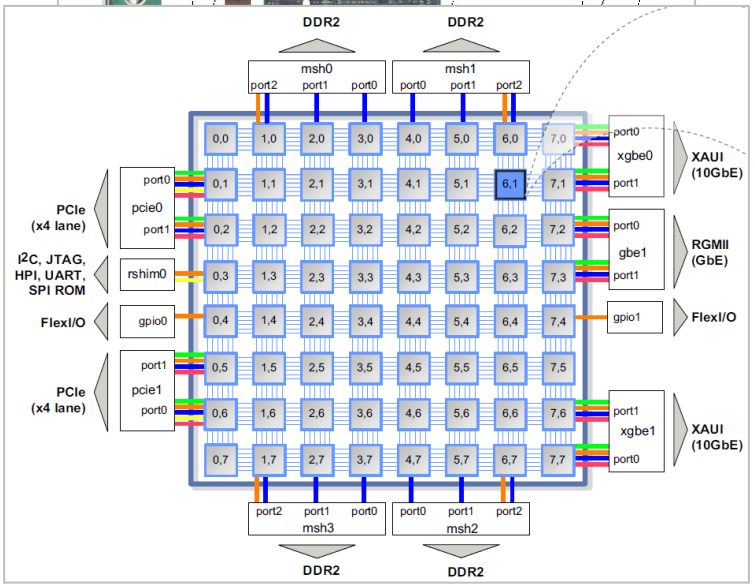
- Automatic parallelizing compiler available on the market gave us no speedup against execution time on 1 core on 64 cores
  - Execution time with 128 cores was slower than 1 core (0.9 times speedup)
- Advanced OSCAR parallelizing compiler gave us 211 times speedup with 128cores against execution time with 1 core using commercial compiler
  - OSCAR compiler gave us 2.1 times speedup on 1 core against commercial compiler by global cache optimization

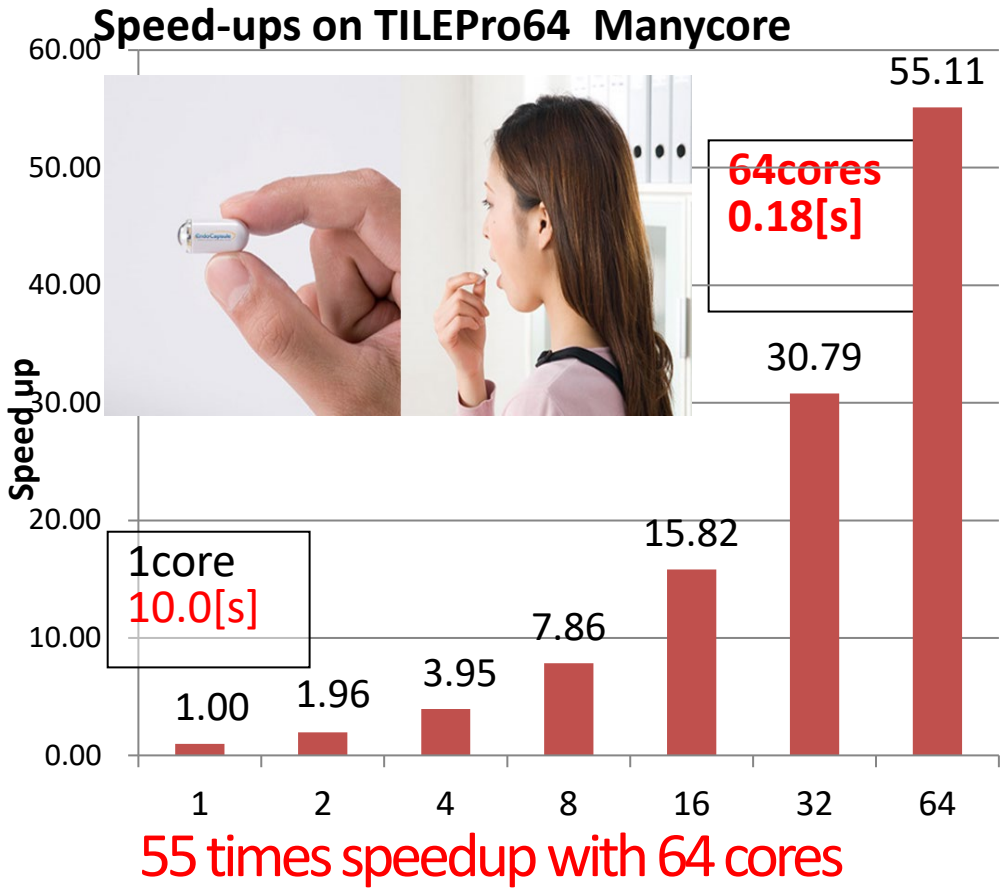
Automatic Parallelization of JPEG-XR for Drinkable Inner Camera (Endo Capsule)

10 times more speedup needed after parallelization for 128 cores of Power 7. Less than 35mW power consumption is required.

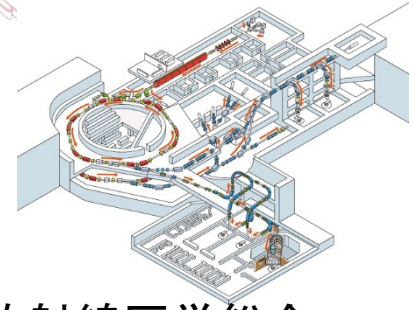
- TILEPro64





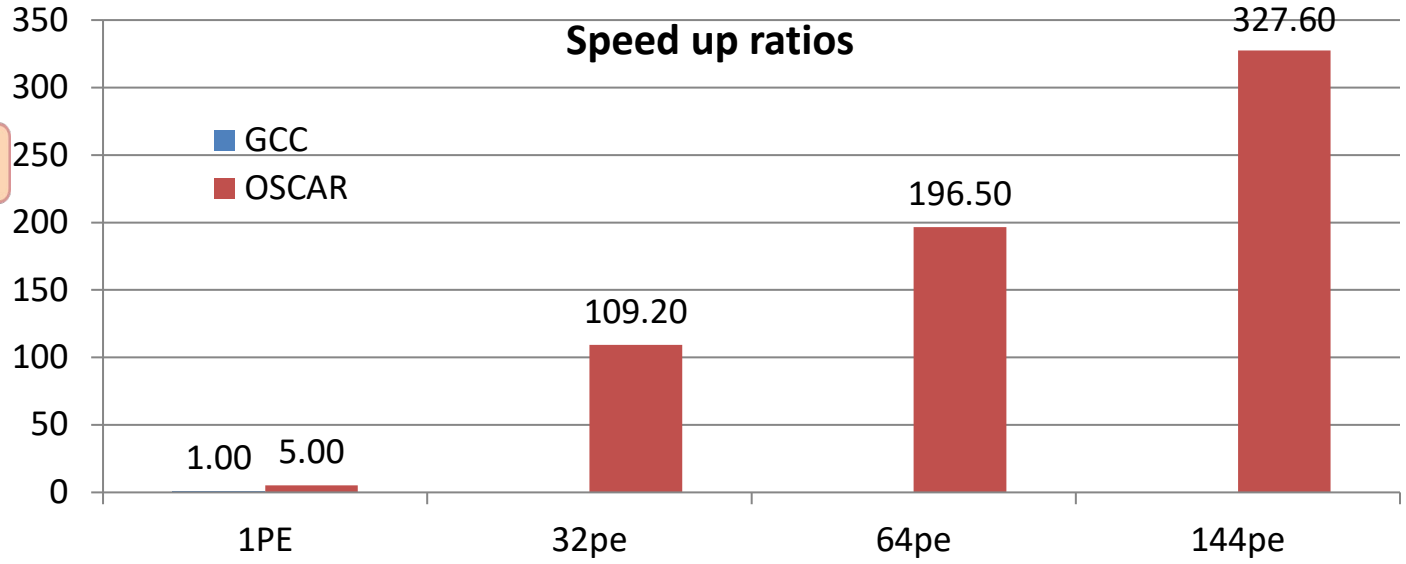


重粒子線がん治療計算の日立BS500ブレードサーバ上での並列化



放射線医学総合研究所サイトより
http://www.nirs.qst.go.jp/rd/cpt/index.html

日立 SMPブレードサーバ BS500:
Xeon E7-8890 V3(2.5GHz　18core/chip) x8 chip 計144cores



- オリジナル逐次実行時間2948秒（約50分）が、OSCARコンパイラによる144コア並列処理で、9秒に短縮され、327.6倍の速度向上

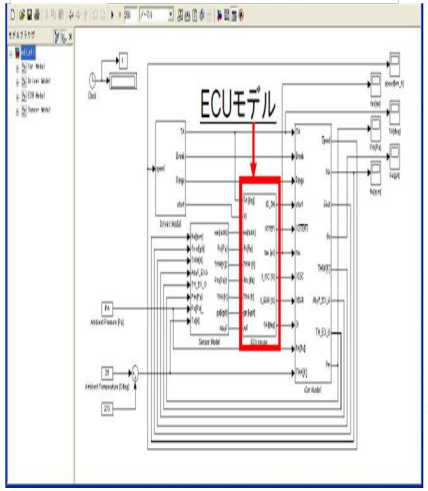
日本乗用車のエンジン制御計算をデンソー2コアECU上で、1．95倍の速度向上に成功。

欧州農耕作業車エンジン制御計算をインフィニオン2コアプロセッサ上で8.7倍の高速化に成功。

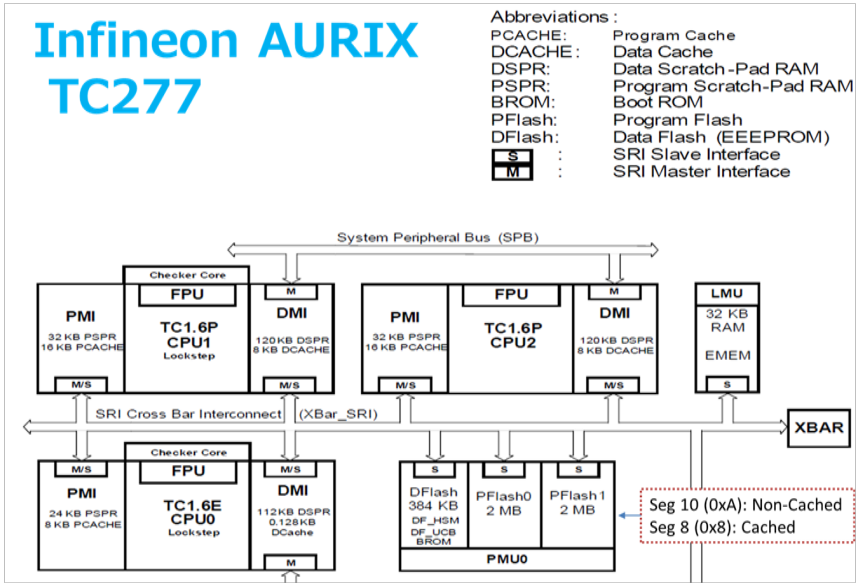
Engine Control by multicore with Denso

Though so far parallel processing of the engine control on multicore has been very difficult, Denso and Waseda succeeded 1.95 times speedup on 2core V850 multicore processor.

- Hard real-time automobile engine control by multicore using local memories
- Millions of lines C codes consisting conditional branches and basic blocks

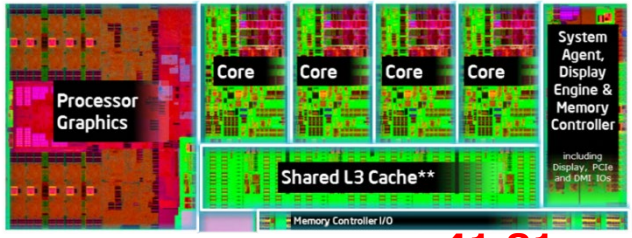


Automatic Parallelization of an Engine Control C Program with 400 thousands lines on AUTOSAR on 2 cores of Infineon AURIX TC277

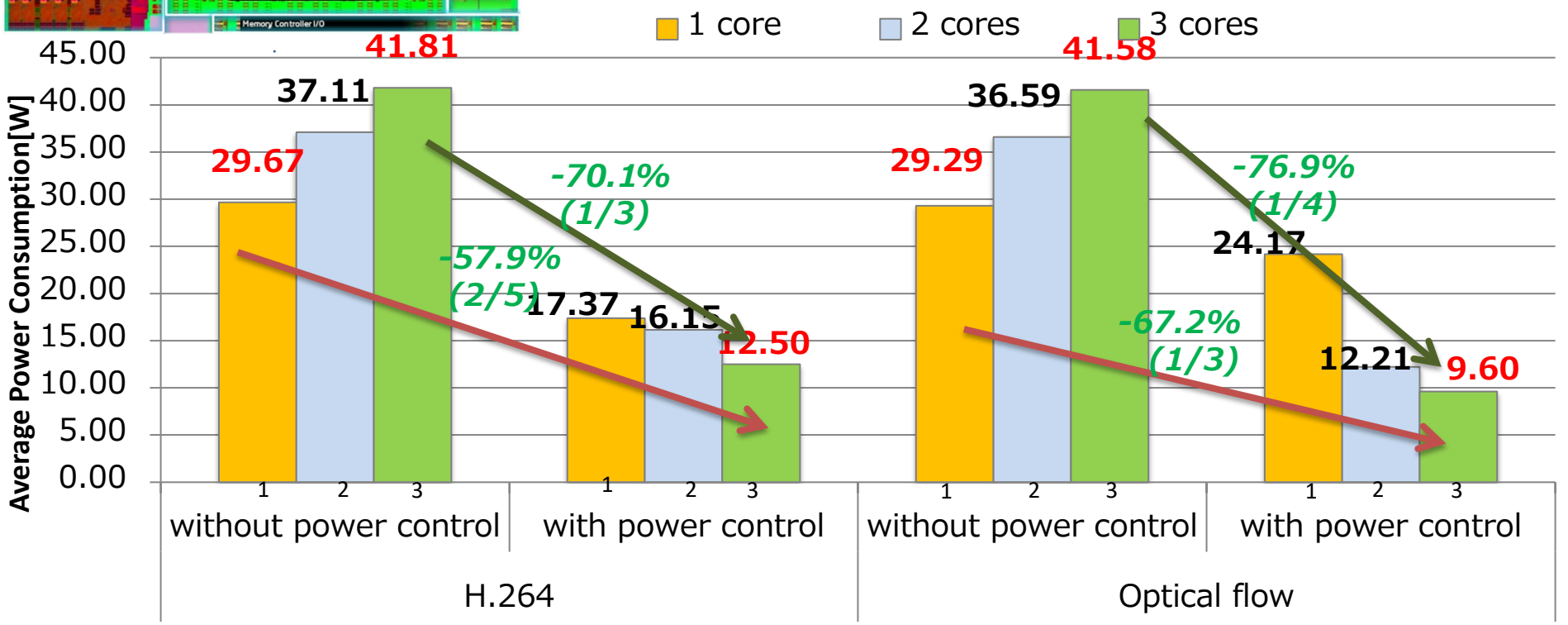


Automatic Power Reuction on Intel Haswell

H.264 decoder & Optical Flow (3cores)



H81M-A, Intel Core i7 4770k
Quad core, 3.5GHz～0.8GHz



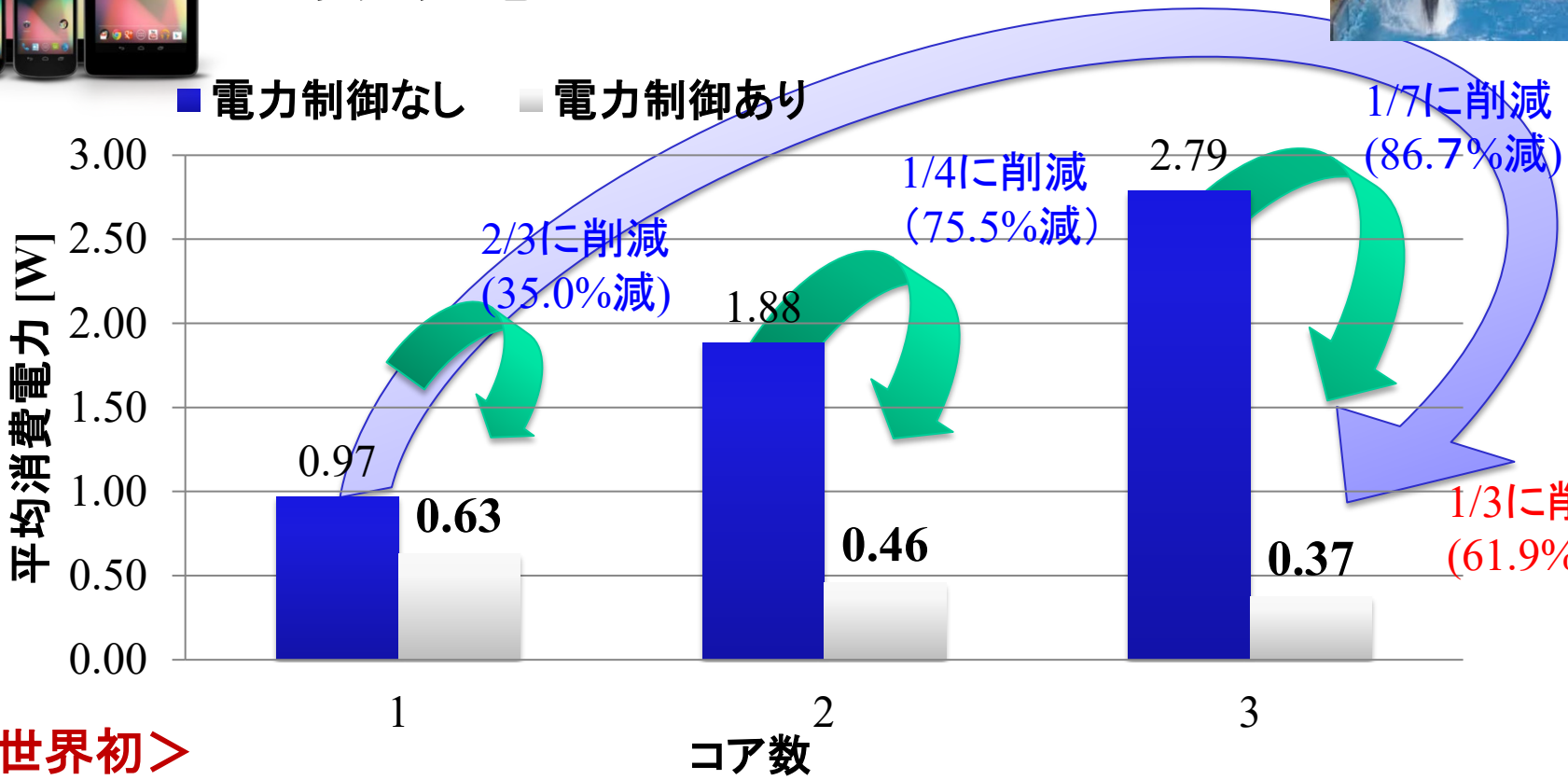
Power for 3cores was reduced to 1/3～1/4 against without software power control
Power for 3cores was reduced to 2/5～1/3 against ordinary 1core execution

46

Androidスマートフォン上での電力削減

http://www.youtube.com/channel/UCS43lNYEIkC8i_KIgFZYQBQ

週1回以下の充電,さらには
太陽光充電を目指して



＜世界初＞

- 3PE電力制御なしと3PE電力制御ありで電力を最大**1/7**に削減
- 1PE電力制御なしと3PE電力制御ありで電力を**1/3**に削減

MULTICORE VIDEO SERIES

Practical Innovation

Multicore processors have become pervasive, but most organizations struggle to use them efficiently. That's why we brought together renowned experts in the field for this video series to examine the innovative techniques they use to improve reliability and performance while reducing costs, time, and power consumption.

Hear about some of the most advanced power-reduction, parallelization, and vectorization technologies used in a range of industry applications, including automobiles, big data, cloud computing, cluster computing, medical image processing, multimedia, smartphones, and supercomputing.

World's best educational content

Learn from the World's Leading Multicore Compiler Experts


Automatic Parallelization
David Padua


Autoparallelization for GPUs
Wen-mei Hwu


Dependences and Dependence Analysis
Utpal Banerjee


Dynamic Parallelization
Rudolf Eigenmann


Instruction Level Parallelization
Alexandru Nicolau


Multigrain Parallelization and Power Reduction
Hironori Kasahara


The Polyhedral Model
Paul Feautrier


Vector Computation
David Kuck


Vectorization
P. Sadayappan


Vectorization/Parallelization in the IBM Compiler
Yaoqing Gao


Vectorization/Parallelization in the Intel Compiler
Peng Tu


Roundtable Discussion
All Presenters

Who Should Watch these Videos?

Professionals in any industry that demands real-time processing, high performance, and speed will find these videos an important tool for getting better results from their multicore processing systems and future-proofing their applications.

Educators and graduate students will also find inspiration from this window into the minds of some of the most accomplished experts in multicore.

www.computer.org/multicore-video

IEEE computer society

IEEE

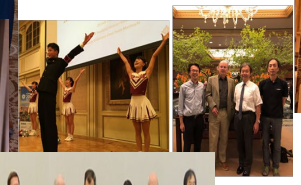
IEEE Computer Society

2018年に早大笠原がIEEE CS (1946年設立)72年の歴史の中で初めて、北米以外から会長に選出

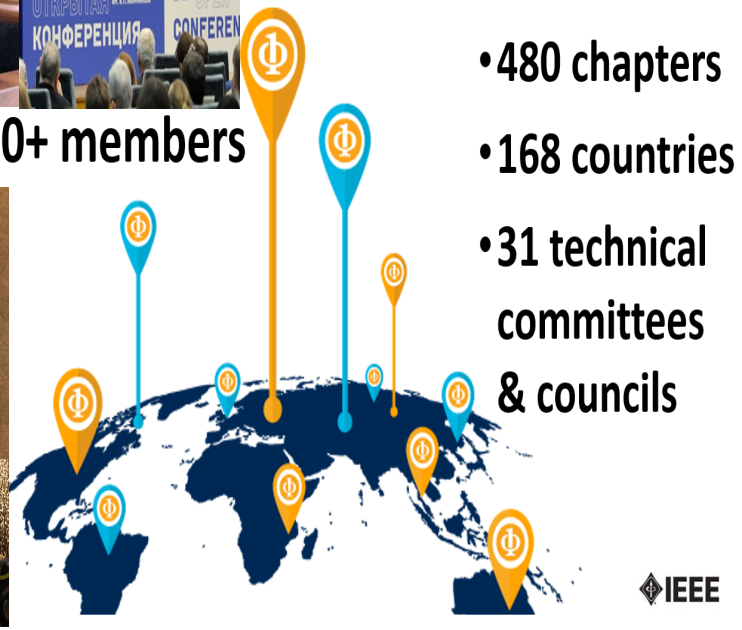
Bjarne Stroustrup: Morgan Stanley & Columbia Univ.
2018 IEEE Computer Society Computer Pioneer Award
IEEE COMPSAC2018 Keynote & Award Ceremony

July 26, 2018, Keynote, Hitotsubashi Hall

July 25, 2018 Award Ceremony
Rihga Royal Hotel Tokyo



- 84,000+ members
- 480 chapters
- 168 countries
- 31 technical committees & councils



ACM/IEEE SC (SuperComputing) 19, Denver, Nov.17-22, 2019

Cornel Univ. Prof. Steven Squyres火星探査、CalTech. Dr. Katie Boumanブラックホール可視化成功の講演等

Cooperation with International Organizations in 2018

IPSJ Leaders, March, IPSJ Convention, Tokyo

Japan (IPSJ), China(CCF), Korea(KIISE) in March, Waseda U., Tokyo

Okawa Foundation, CS Japan Chapter, Multicore STC & Japanese Government Symp.

MoU with UN ITU in AI for Good, May, Geneva

CCF China National Computer Congress, Oct. , Hangzhou

MoU with Baidu, July, Green Comp. C., Tokyo

Russian Academy of Science: Russian Computer Science 70th Anniversary, Nov., Moscow

IEEE CS China Office moderated Tencent-Waseda Univ. Joint Symposium, Nov., Waseda U., Tokyo

WASEDA University -早稲田大学-

Number of International Students

7,942* from 125* countries and territories

(Undergraduate and Graduate)

Alumni CEOs in Japan

10,606

8 Prime Ministers

Founder Shigenobu OKUMA

Graduate Employability

#1 in private university of Japan

(#2 in Japan, #27 in the world)

QS Graduate Employability Rankings 2019

ENROLLMENT [学生数]	ALUMNI [卒業生]
49,436	630,000
	FACULTY [教員]
	5,468

World Business

5 Palmes in Eduniversal Busine

Masaru IBUKA

Tadashi YANAI

PARTNER INSTITUTIONS [協定大学・機関]	NUMBER OF BOOKS [図書館蔵書]	GRADUATE STUDENTS [大学院生]	UNDERGRADUAT STUDENTS [学部生]
848 (93 countries)	5,800,000	8,385	41,051

Hiroshi YAMAUCHI

Prime Ministers	Business Leaders Founders of global companies	Business Leaders CEOs of global companies
8th Shigenobu Okuma	Sony	ANA (All Nippon Airways)
17th Shigenobu Okuma	Samsung	HONDA
55th Tanzan Ishibashi	Casio	Nintendo
74th Noboru Takeshita	LOTTE	UNIQLO
76th Toshiki Kaifu		Shiseido
84th Keizo Obuchi		Nomura Securities Co., Ltd.
85th Yoshiro Mori		Tokio Marine & Nichido Fire Insurance Co., Ltd.
91st Yasuo Fukuda		Olympus Corporation
95th Yoshihiko Noda		

Aiji TANAKA

President
International Political Science Association (IPSA) President 2016

Hironori KASAHARA

Senior Executive Vice President
IEEE Computer Society President 2018. The first president from outside USA and Canada in 72 years CS history. CS has 84,000 members from, 168 countries.

Toshio FUKUDA

The University Professor Waseda, Waseda Alumnus, Prof. Emeritus Nagoya Univ., Prof. Meijo Univ.
IEEE President 2020. The first from Asia in 135 years history.
IEEE has 420,000 members.

Haruki MURAKAMI

Hirokazu KOREEDA

Yuzuru HANYU

S. ARAKAWA

Daiya SETO

THE World Academic Summit, チューリッヒ工科大学,2019.9.10

世界リーディング大学学長・ノーベル賞受賞者パネル

Science Webinar Series

Transitioning humanoid robots from laboratory to home: From 3D printing to AI-driven computation

3 March 2021

Participating experts

Prof. Hironori Kasahara, IEEE Fellow, IPSJ Fellow
Senior Executive Vice President, Waseda University
IEEE Computer Society President 2018
URL: http://www.kasahara.cs.waseda.ac.jp/

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早稲田大学

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IEEE Computer, Oct. 2020号 (Open Access Article)
世界のHigh Qualityオンライン教育に向けた9カ国のオンライン教育事例共有

EDITOR IRENA BOJANOVA
NIST, irena.v.bojanova@gmail.com

Computer Education in the Age of COVID-19

Jean-Luc Gaudiot, University of California, Irvine
Hironori Kasahara, Waseda University

COVID-19 has been devastating across the globe, forcing profound changes in most human interactions. Through an informal survey of numerous educators worldwide, we explore some of the disease's effects on the education community and how the online delivery of educational materials can meet these challenges.

As many in the world continue to suffer from the devastating effects of the COVID-19 pandemic, solutions are continuously being sought for dealing with its consequences and the need to reduce opportunities for infection. Stores of all kinds have adapted by encouraging social distancing, requiring face masks, installing Plexiglas partitions in

Digital Object Identifier 10.1109/MC.2020.3011277
Date of current version: 5 October 2020

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In between the of higher learning lemma with which how to continue op ers experience diffi of necessary safety ularly acute for edu face-to-face interac tailor the delivery o

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We have therefore endeavored to find out how our colleague educators in computer science and engineering have approached this dramatic situation, what fruit their efforts have borne, and what support (or resistance) they have met with the student population, their own colleagues, and their administration. Indeed, most universities and schools worldwide have had to quickly retool and turn to long-distance education to continue fulfilling their educational mission when faced with the pandemic emergency and the resulting stay-at-home orders. This has caused many teething problems, from needing to educate instructors, to deciding how lab classes could be handled, all the way to designing secure environments for exams. It is thus the goal of this column to describe the reactions of educators globally. We offer a small sample of how our international colleagues have dealt with the crisis, what they regret, how they will improve; in short, they relate their experiences to the community, perhaps providing some guidance to us all for the future.

THE SURVEY

We contacted a small sample of colleagues from a number of countries around the world and presented them with the a set of 10 questions.

Question 1

What classes did you teach during the pandemic (undergraduate/graduate/lab)? How many students?

We received reports for 24 computer science and engineering-related classes for 10–400 graduate and undergraduate classes from 14 universities in nine countries, including the United States, United Kingdom, Brazil, Russia, Australia, Spain, Japan, China, Taiwan, and Iran in addition to a report for 18,000 classes for 50,000 undergraduate and graduate students from Waseda University, Japan.

Question 2

Did any one topic lend itself better/worse to remote teaching?

Most respondents (with some exceptions) are satisfied with online teaching, and there appears to be no specific topic for which online teaching presents any disadvantages. On the contrary, a number of respondents felt that it allowed the students to better concentrate. Some even cited programming courses as easier to manage online. On the negative side, some people deplored the obvious lack of teacher–student interaction. Lab classes can also take advantage of many online teaching platforms with recording or playback functions, which allow the students to review difficult steps or verify procedures beforehand.

> The problem is particularly acute for educators, who have long relied upon face-to-face interactions and interpersonal feedback to tailor the delivery of high-quality knowledge.

Question 3

What tools did you use? How much ramp-up effort was needed? What kind of support did your home institution provide? What kind would you have liked?

The following tools were reportedly used:

- learning management systems (LMSs): Moodle, Canvas, etc.
- plagiarism detection: iThenticate, Turnitin, Ejudge, etc.
- on-demand video creation and/or delivery, including
  - massive open online courses, YouTube, etc.
  - for self-on-demand video content creation in professors' homes and content delivery: Panopto, Contents Creation Studio, Open Broadcaster Software with a Vimeo platform, etc.
  - for assisted content creation on campus and content delivery, Milvi, etc. were utilized
- for real-time online lectures and meetings with recording: Zoom, Blackboard Collaborate, Microsoft Teams, Cisco Webex, Google Meet, Skype, Tencent Meeting, Rain Classroom, Jitsi, etc.; most universities provided enough licenses for faculty members and staff
- reporting and analytics for LMSs: IntelliBoard, etc.
- smartphone scanner generating PDFs for handwritten answers: Microsoft Office Lens, etc.
- exam proctors.

Universities offered the following support to prepare and operate online classes:

- "Teaching Anywhere" sites for teachers, providing information on how to prepare and operate online education with the lecturers' experiences during classes
- webinars to explain how to prepare online lectures, including on-demand video lectures and real-time online lectures (these were very helpful to educators who had not used network meeting systems or prepared on-demand video materials from their homes)
- "Learning Anywhere" sites for students, offering information on how to prepare and receive online lectures, including the prevention of server overload as a result of simultaneous log-ins in the morning and after lunch.

As an additional data point, we note that the following additional support to cope with COVID-19 was provided at Waseda University:

- free lending of Wi-Fi routers and PCs to students with financial issues stemming from the pandemic
- specially discounted ¥1 smartphones with tethering functionality and one-year free data communication for all students, faculty members, and staff who needed to reduce home network bandwidth problems
- negotiation with major smartphone companies for the purpose of discounting data communication fees for all students in Japan during the spring semester
- access to a help desk for faculty and students to prepare, operate, and/or participate in online classes from their homes. The help desks were operated by using "home-based call center systems" so that staff and teaching assistants (TAs). could answer from their own homes.

The University of California, Irvine (UCI) also proactively assisted in the transition:

- online classes for the lecturers and TAs prior to the quarter; these classes were aimed at lecturers with content creation and delivery, website design, etc.

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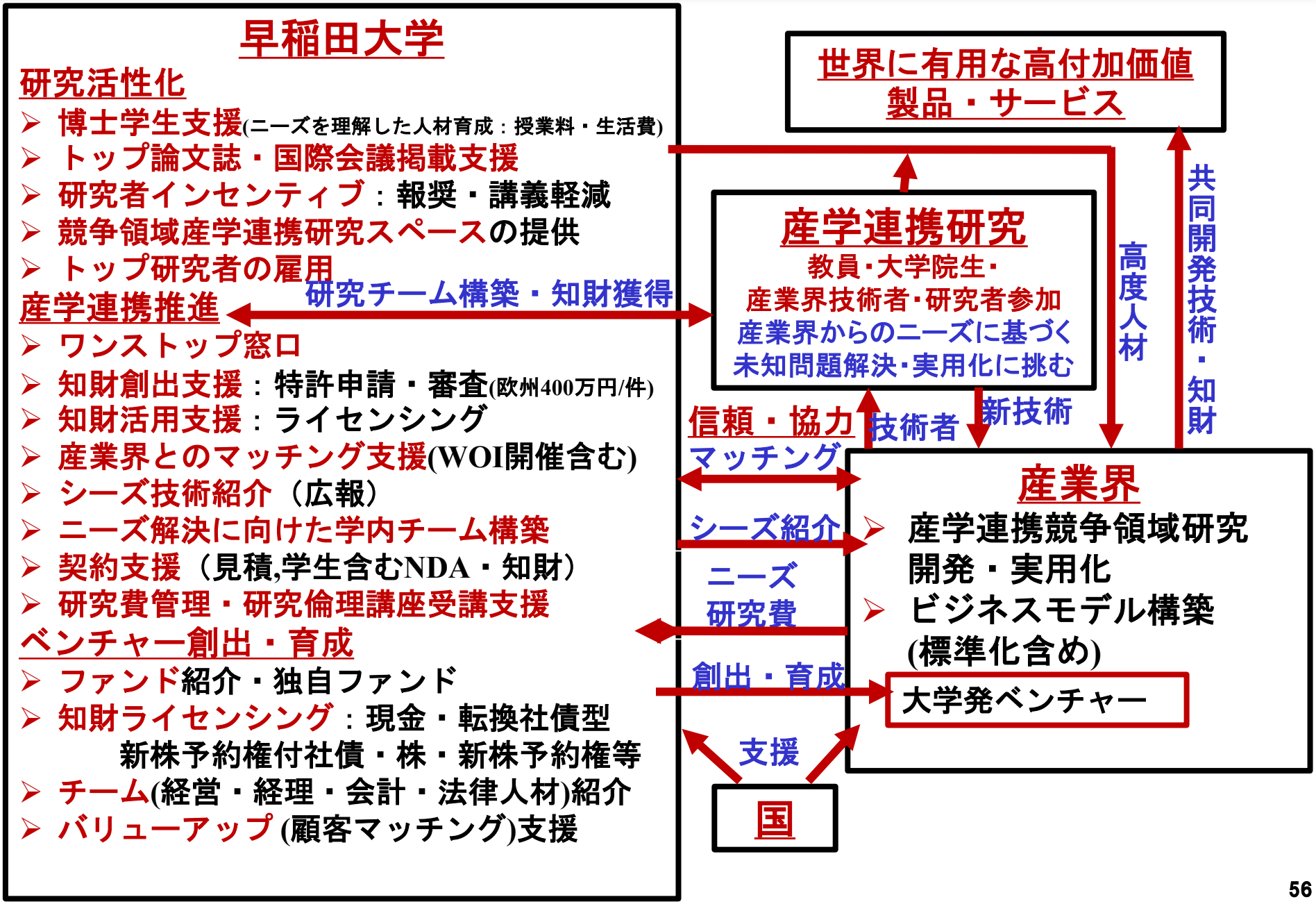
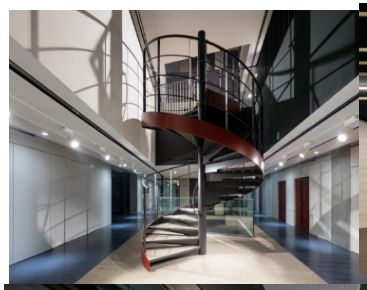
早稲田オープン・イノベーション・エコシステム

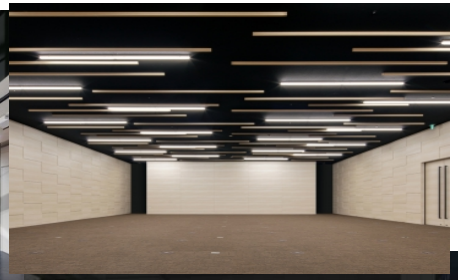


早稲田大学リサーチイノベーション統合センター

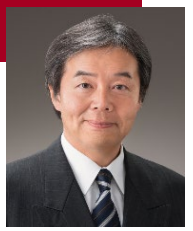
「リサーチイノベーションセンター」（2020年3月竣工）

B1　カンファレンスルーム





1階　イノベーションギャラリー



副総長(研究推進担当)が
統括センター長を兼任

リサーチイノベーション統合センター

（2021年1月より改称）

早稲田オープンイノベーションエコシステムの推進母体

研究戦略センター　URAを介した大学の研究戦略機能

オープンイノベーション戦略研究機構

- 数理エネルギー変換工学
- 持続可能エネルギー
- 先端ICT
- 建築・まちづくり
- 自動車用パワートレイン
- 生物資源利用
- 資源循環技術

企業出身ファクトリーマネージャーを活用した組織的企業連携

知財・研究連携支援センター（TLO: WTLO）　技術・法務専門家による知財獲得・技術移転戦略機能

アントレプレナーシップセンター

ベンチャー支援、アクセラレーション

- ビジネス、法務、財務面でのコンサルティングサービス
- 法人登記などオフィスサービス
- 経営チーム構築支援・ネットワーキングサービス
- 資金面での支援，上場（Exit）に向けたアクセラレーション

提携VC（2018年11月～）　WERU Investment Research & Business Development　Beyond Next Ventures

JST Score　プロジェクト

PoCファンド（2020年7月～）

早稲田オープン・イノベーション・バレー（Waseda Open Innovation Valley）構想

早稲田オープン・イノベーション・エコシステムの実現
－グローバルなオープンイノベーション環境の創造－

インキュベーションセンター
- 早稲田大学の学生・教職員を対象に起業支援を実施
- ベンチャー企業向けスペース・設備を整備

各務記念材料技術研究所
- 文部科学省「環境整合材料基盤技術共同研究拠点」

早稲田キャンパス

スマートエナジーシステム・イノベーションセンター

- JST「革新的イノベーション創出プログラム」(COIサテライト拠点)
- 蓄電池研究開発の拠点として広く学内外の研究者と連携

リサーチイノベーションセンター(仮)

- 総工費100億円(自主経費)による産学連携拠点の建設（2020年4月竣工、地上6階地下2階 総床面積18,000m²）
- 各種研究支援事業（産学連携ワンストップ窓口、研究推進・戦略、TLO、契約支援、アウトリーチ機能）を整備
- 文部科学省「オープンイノベーション機構の整備事業」を推進

早稲田アリーナ

- 多目的施設「早稲田アリーナ」が完成（2018年12月竣工）
- 健康スポーツサイエンス研究を推進

戸山キャンパス

喜久井町キャンパス

グリーン・コンピューティング・システム研究開発センター

- 経済産業省「産業技術研究開発施設整備事業」の支援を受け建設（2011年）
- 次世代マルチコア・メニーコアのハードウェア、ソフトウェア、応用技術等の研究開発を推進
- 産学共同による次世代高付加価値技術を創出する人材の育成

日本のスタートアップを
シリコンバレー、そして世界へとつなぐ。

世界最高峰のスタートアップスクール、Y Combinatorに挑む

2005年に創立されたY Combinator（通称、YC）は毎年2回、約3ヶ月間のプログラムを通して、厳選したスタートアップをシリコンバレーのオフィスにて指導し、30ヶ国以上から参加する起業家を競い合わせることで、これまで2000社以上のスタートアップを育成してきた。その結果、YCは企業価値10億ドル（約1000億円）を超える企業を25社以上輩出し、世界一のアクセラレーターとしての評価を受けることに成功している。

YCのプログラムに参加し、卒業することはスタートアップにとって大きな飛躍のチャンスであり、またグローバル市場へ挑戦する登竜門となっている。

開催日：2020年10月20日(火)-22日(木)

形　式：オンライン

費　用：無料

主　催：SVJP・Y Combinator

言　語：日本語・英語（Day1,2のみ日本語同時通訳あり）

DAY 1　10/20 TUE

09:30

Opening Speech

YCのプログラムを紹介するほか、申込みの方法や審査基準、近年の合格者の傾向を解説。さらに、起業を志す日本の参加者のためだけに「YC流スタートアップの始め方」を特別にレクチャーします。

山岸 広太郎
株式会社慶應イノベーション・イニシアティブ 代表取締役社長
プロフィールをみる

09:30-10:10

How YC Works + How to Start a Startup

シリコンバレーにあるYCのオフィスで行われるブートキャンプ。メンターとなるYCパートナーや卒業生起業家から指導を受け、選抜された約30ヶ国出身の同期の起業家たちと競い合う3ヶ月のプログラムの中身や実態を紹介。Day1で紹介される基礎的な情報に加えて、オンラインで行われた直近の2020年夏期プログラムについても振り返ります。

Kat Mañalac
Y Combinator パートナー
プロフィールをみる

10:15-10:45

Advice for Deep Tech and Biotech Founders

ディープテックやバイオテック系の起業家とその予備軍の方々（研究者・大学院生）に向けて、プロダクト化、資金調達、社会実装といった一連の流れをレクチャーします。また研究医でもあるYCパートナーのUri Lopatin氏が、B型肝炎に関するスタートアップを始めた際の経験を交えて実践的なアドバイスを送ります。

Uri Lopatin
Y Combinator パートナー
プロフィールをみる

10:50-11:50

The Role of the University in the Innovation Ecosystem

日本の大学におけるスタートアップ・インキュベーションへの取り組みを紹介した上で、シリコンバレーの事例を絡めながら、大学発イノベーションのあるべき姿について討議します。大学という環境を活かしてどのように起業できるかについて、新しいインサイトを得られるセッションです。

佐藤 輝英
BEENEXT ファウンダー & CEO
プロフィールをみる

Kat Mañalac
Y Combinator パートナー
プロフィールをみる

笠原 博徳
早稲田大学 副総長
プロフィールをみる

川原 圭博
東京大学 大学院工学系研究科 教授
プロフィールをみる

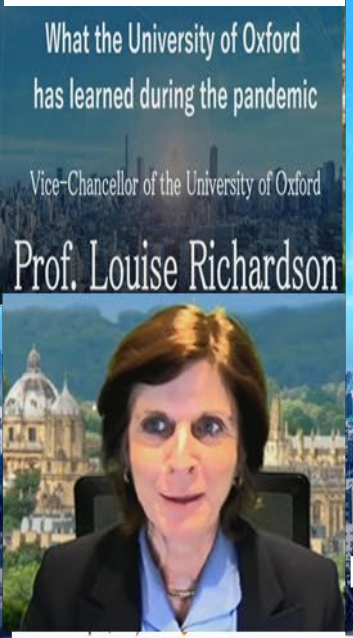
木谷 哲夫
京都大学 産官学連携センター寄付研究部門 教授
プロフィールをみる

坪田 一男
慶應義塾大学 医学部眼科学教室教授
プロフィールをみる

2021年3月9-10日 オンライン開催(参加:2300人)

WOI'21実行委員長
早稲田大学副総長(研究推進)
笠原博徳

オックスフォード
THE大学ランキング
5年連続世界No.1



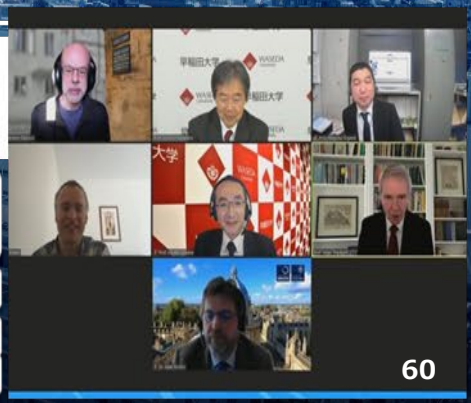
WOI'21

WASEDA OPEN INNOVATION FORUM 2021

早稲田オープン・イノベーション・フォーラム2021

IEEE
世界最大の学会

文部科学省 大臣官房審議官(科学技術・学術政策局担当) 梶原 将 氏
経済産業省 大臣官房審議官(産業技術環境局・福島復興担当) 萩原 崇弘 氏



- グリーン・コンピューティング・システム研究機構 10周年記念講演会
- Oxford-Waseda Computer Science Symposium (オックスフォード大学との大学間協定両大学トップ研究者の講演)
- 研究院・研究機構の取り組み紹介
- 早稲田知財活用ベンチャー紹介
- 研究成果展開事業 社会還元加速プログラム(SCORE) Demo Day
- 学生の発表 (EDGE-NEXT、ビジネスコンテスト優勝者、DSコンペティション優秀賞受賞者の講演)

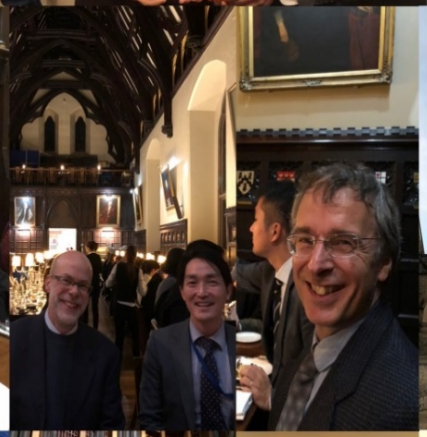
Oxford University, 11/12-13,2019（CSでの招待講演及び連携協議）

Vice Chancellor Prof. Louise Richardson
（WOI 2020で基調講演）
Head of Astrophysics：Prof. Rob Fender
Dept. of Physics: Prof. Ian Shipsey
Astrophysics: Prof. H.Falche, et. al.

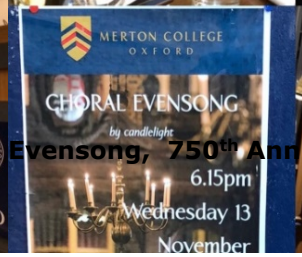
Merton College
Warden: Prof. Irene Tracy（2020年1月に来学）
Fellow: Dr. Peter Braam
Sub Warden: Prof. Judy Armitage
CS: Prof. Jeremy Gibbons













Choral Evensong，750th Anniversary Room

2020年4月オックスフォード大との大学間協定締結（CS,数学,物理）

DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF OXFORD

HOME ADMISSIONS RESEARCH NEWS & EVENTS ABOUT US ALUMNI OUR STUDENTS INNOVATION

HOME > NEWS & EVENTS > NEWS > UNIVERSITY OF OXFORD SIGNS MEMORANDUM OF UNDERSTANDING WITH WASEDA UNIVERSITY

News
- Latest News
- *Inspired* Research Newsletter
- Media Wall
- Blogs
- News Archive

Events

University of Oxford signs Memorandum of Understanding with Waseda University

Posted: 22nd April 2020

To support exchanges of graduate students and staff and to collaborate on research, a Memorandum of Understanding has been signed between the Departments of Computer Science, Mathematics, and Physics at Oxford and **Waseda University** in Tokyo. The new Memorandum of Understanding was established following the visit of **Professor Hironori Kasahara** (senior executive vice president of Waseda) in November to give a **lecture** on green computing; **Professor Jeremy Gibbons** (Computer Science) and **Professor Peter Braam** (Physics) made the return visit to Waseda in January to set up the memorandum. Waseda is one of the top private universities in Japan, with particular strengths in robotics and green computing, and this agreement will provide new opportunities for working together, particularly in machine learning and programming languages.

Photos

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Athena SWAN Bronze Award

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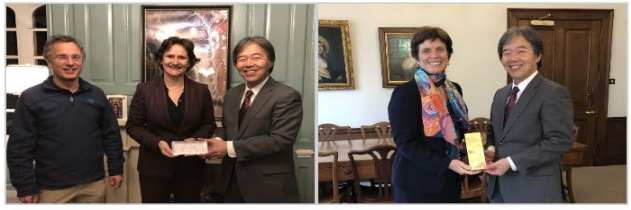
Topic
トピック

オックスフォード大学と研究交流促進

オックスフォード大学と大学間協定締結

2020年4月17日付で、早稲田大学とオックスフォード大学は大学間協定を締結しました。
この協定により、早稲田大学とオックスフォード大学の "Computer Science"、 "Mathematics"、 "Physics"分野での研究・教育面の組織的な交流の活性化が実現します。

オックスフォード大学とは、かねてより幅広い分野での研究交流が行われていましたが、個々の教員同士の交流が点在している状態でした。この度、両大学に於いて更なる組織的な研究交流の促進を模索する中、研究交流に特化した大学間協定を締結する運びとなりました。
今後は大学間協定の締結を土台にして、よりスケールの大きい研究・教育面での交流が可能となります。相互に研究者や大学院生の交換を促進し、研究プロジェクトを推進することになります。



また、この３分野にとどまらず、多方面での研究交流へと幅を広げるべく協議していくことが合意されており、今後、さらなる2大学間の交流の発展を目指していきます。

ヨーロッパにおける研究交流を加速

本学は2016年にヨーロッパにおける研究拠点として、ベルギーのブリュッセルにオフィスを開設いたしました。すでにヨーロッパの多くの大学との研究交流が進んでいますが、オックスフォード大学との大学間協定の締結によって、これまで本学が推進してきたヨーロッパにおける研究交流を、さらに加速させることが可能となります。

Tags
Vision 150, 国際課, 教務部, 教育, 研究活動, 総長室

Posted
Wed, 22 Apr 2020

ツイート Like Share メールで送信

IEEE (Institute of Electrical and Electronics Engineers)
1884年にトーマス・エジソン、グラハム・ベル等が設立

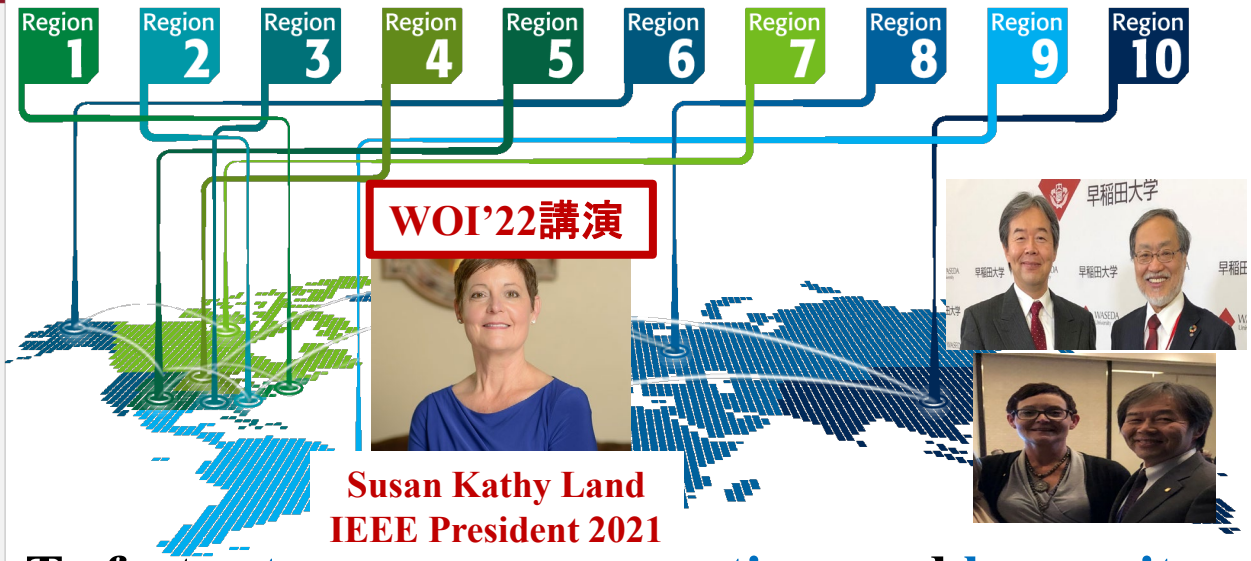
Toshio FUKUDA
IEEE 2020会長

早稲田
機械卒
特命教授

IEEE 136年の歴史の中でアジア初の会長

The University Professor Waseda,
Waseda Alumnus, Prof. Emeritus
Nagoya Univ., Prof. Meijo Univ.
IEEE President 2020. The first from Asia in 135 years history.
IEEE has 420,000 members.

World's largest technical professional organization



To foster technology, innovation, and humanity

- More than **422,000** members in over **160** countries, 50+ % from outside the United States
- **339** Sections in **10** geographic Regions worldwide
- More than **123,000** student members
- **2,200+ Student Branch Chapters** of IEEE **45 Technical Societies**
- **3,200+ Student Branches at colleges and universities in 100 countries**
- **200 transactions, journals, and magazines**
- **1,900 conferences in 103 countries each year**
- **1,800 conference proceedings via IEEE Xplore**

IEEE Women in Engineering We

IEEE

IEEE youngprofessionals

チューリング賞受賞記念講演が開催されるコンピュータ・アーキテクチャの世界最高峰国際会議　ACM/IEEE ISCAの2024あるいは2025年6月早稲田開催が決定

Co-Chairs:Jean-Luc Gaudiot (Prof. UCI, IEEE CS President 2017)
Hironori Kasahara (SEVP Waseda, IEEE CS President2018)

ACM/IEEE International Symposium on Computer Architecture にてコンピュータ分野のノーベル賞と言われるチューリング賞記念講演会を早稲田大学大隈講堂で実施予定

ソーラーパワー・パーソナル・スパコン：新アクセラレータ・グリーンマルチコア

（AI、ビッグデータ、自動運転車、交通制御、ガン治療、地震、ロボット）

世界最高性能・低電力化機能OSCARコンパイラとの協調

ベクトルアクセラレータ併置・
共有メモリ型マルチコアシステム

性能：8TFLOPS, 主メモリ：8TB

電力: 40W, 効率：200GFLOPS/W

- 命令拡張などのプロセッサにも付加できるベクトルアクセラレータ
  - 低消費電力で高速に立ち上がるベクトルで、低コスト設計
- コンパイラによる自動ベクトル・並列化及び自動電力削減
  - 周波数・電源電圧制御機能
  - バリア高速同期・ローカル分散メモリで無駄削減
  - ローカルメモリ利用で低メモリコスト
  - 誰でもチューニングなく使用でき、低コスト短期間ソフト開発可能

笠原・木村研究室：アドバンストマルチコアプロセッサ研究所

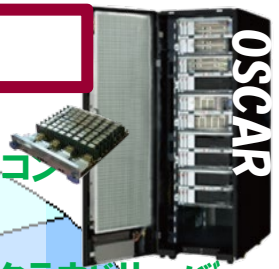
制御

車載（エンジン制御・自動運転Deep Learning・ADAS・MATLAB/Simulink自動並列化）デンソー，ルネサス,NEC

交通シミュレーション・信号制御　NTTデータ・日立

環境を守る

命を守る



グリーンスパコン

グリーンクラウドサーバ

アドバンストマルチコアプロセッサ研究所

OSCARマルチコア/メニーコア
&コンパイラ　オスカー

OSCAR
Many-core
OS
API

産業

医療

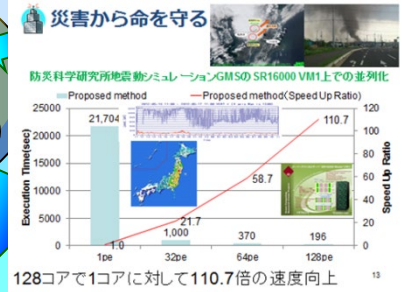
生活

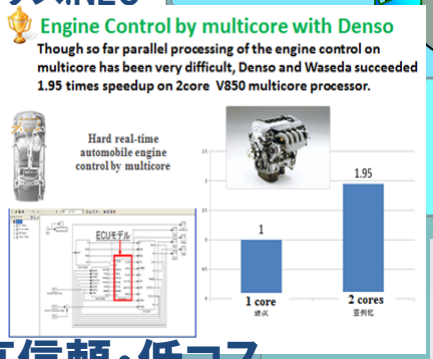
災害

ホーム・産業系メニーコア

サーバ系メニーコア

デスクトップスパコン





高信頼・低コスト・ソフト開発

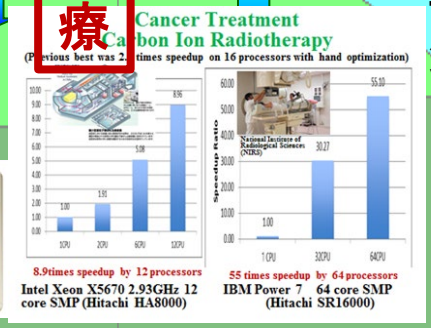
FA　三菱

カプセル内視鏡オリンパス

スマートフォン

カメラ

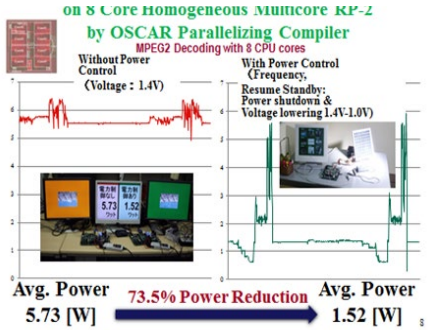
太陽電池駆動・週1以下の充電



医用画像処理等専用サーバ（医療・重粒子線照射計画）日立

首都圏直下型地震火災延焼、
住民避難指示

新幹線車体設計・ディープラーニング・日立



企業　持続的高付加価値製品の開発　大学

高速化

低消費電力化

産業競争力を守る