IEEE COMPSAC2021 IEEE-HKN Panel

Working in the IT world: a 20+ years overview in Japan

Hironori Kasahara, IEEE Fellow, Mu Tau Chapter Advisor

Senior Executive Vice President, Waseda University

IEEE Computer Society President 2018

URL: http://www.kasahara.cs.waseda.ac.jp/

1980 BS, 82 MS, 85 Ph.D. , Dept. EE, Waseda Univ.
1985 Visiting Scholar: U. of California, Berkeley,
1986 Assistant Prof., 1988 Associate Prof., 1989-90 Research Scholar: U. of Illinois, Urbana-Champaign, Center for Supercomputing R&D, 1997 Prof.,
2004 Director, Advanced Multicore Research Institute,
2017member: the Engineering Academy of Japan (2020 Board Mem) and the Science Council of Japan
2018 IEEE Computer Society President
Nov. Senior Vice President, Waseda Univ.

AWARD: 1987 IFAC World Congress Young Author Prize
1997 IPSJ Sakai Special Research Award,
2005 STARC Academia-Industry Research Award,
2008 LSI of the Year Second Prize,
2008 Intel Asia Academic Forum Best Research Award,
2010 IEEE CS Golden Core Member Award
2014 Minister of Edu., Sci. & Tech. Research Prize
2015 IPSJ Fellow, 2017 IEEE Fellow, Eta Kappa Nu
2019 Spirit of IEEE Computer Society Award,
2020 IPSJ Contribution Award,

Reviewed Papers: 223, Invited Talks: 215,
Granted Patents: 62 (Japan, US, GB, China),
Articles in News Papers, Web News, TV etc.: 660

Committees in Societies and Government 263
IEEE Computer Society: President 2018, Executive Committee(2017-2019), BoG(2009-14), Strategic Planning Committee Chair 2018, Multicore STC Chair (2012-), Japan Chair(2005-07),
IPSJ Chair: HG for Magazine. & J. Edit, Sig. on ARC.
【METI/NEDO】 Project Leaders: Multicore for Consumer Electronics, Advanced Parallelizing Compiler, Green Computing
【Cabinet Office】 CSTP Supercomputer Strategic ICT PT, Japan Prize Selection Committees, etc.
【MEXT】Info. Sci. & Tech. Committee,
Supercomputers (Earth Simulator, HPCI Promo., Next Gen. Supercomputer K) Committees
JST Moonshot Project G3 Robot & AI Vice Chair,
【COCN】Board Member in Council of Competitiveness Nippon, etc.

Some of papers in and just after Ph.D. Course in Waseda U.

IEEE TRANSACTIONS ON COMPUTERS, VOL. C-33, NO. 11, NOVEMBER 1984 1023

Practical Multiprocessor Scheduling Algorithms for Efficient Parallel Processing

HIRONORI KASAHARA, MEMBER, IEEE, AND SEINOSUKE NARITA, SENIOR MEMBER, IEEE

Courtesy of dexchao - Fotolia.com

104 IEEE JOURNAL OF ROBOTICS AND AUTOMATION, VOL. RA-1, NO. 2, JUNE 1985

Parallel Processing of Robot-Arm Control Computation on a Multimicroprocessor System

HIRONORI KASAHARA MEMBER, IEEE, AND SEINOSUKE NARITA, SENIOR MEMBER, IEEE

2nd International Conference on Superecomputing
Santa Clara, CA, USA May 3-8,1987

A PARALLEL PROCESSING SCHEME FOR THE SOLUTION OF SPARSE LINEAR EQUATIONS USING STATIC OPTIMAL-MULTIPROCESSOR-SCHEDULING ALGORITHMS

H.Kasahara*, T.Fujii*, H.Nakayama*, S.Narita*, and Leon O.Chua**

* Dept. of Electrical Eng., Waseda University, Tokyo, 160, Japan
** Dept. of Electrical Eng. and Computer Sciences, University of California, Berkeley, CA 94720, U.S.A.

PARALLEL PROCESSING OF ROBOT MOTION SIMULATION

H. Kasahara, H. Fujii and M. Iwata

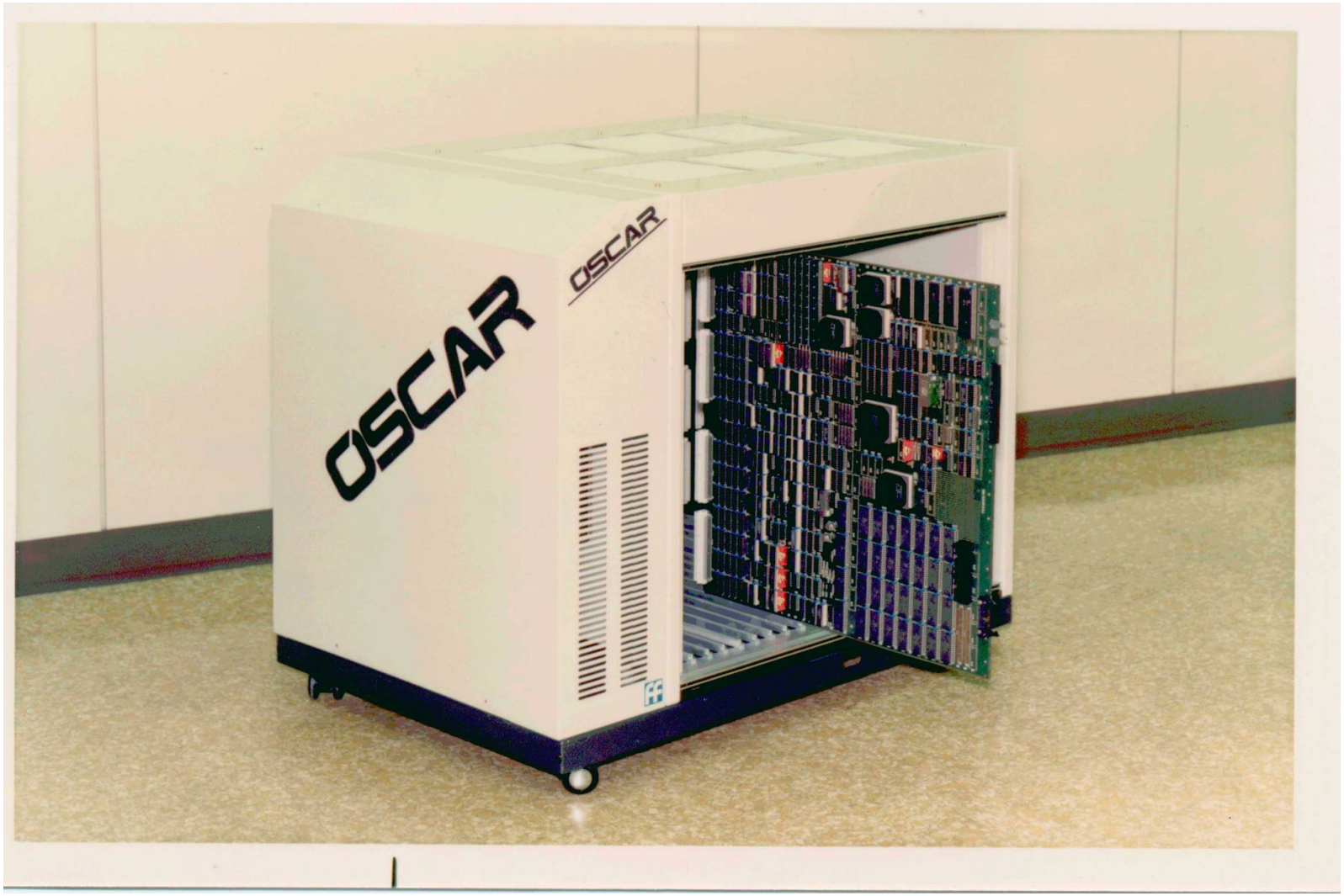
Department of Electrical Engineering, Waseda University, 3–4–1 Ohkubo Shinjuku-ku, Tokyo 160, Japan

1987 OSCAR(Optimally Scheduled Advanced Multiprocessor)

Co-design of Compiler and Architecture

Looking at various applications, design a parallelizing compiler and design a multiprocessor/multicore-processor to support compiler optimization

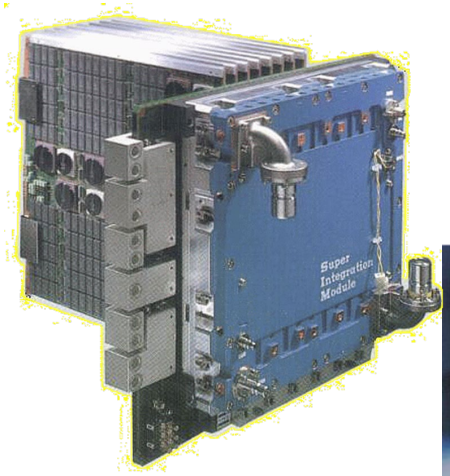
Easy to Use, Collaboration of Software and Hardware, Useful for World People

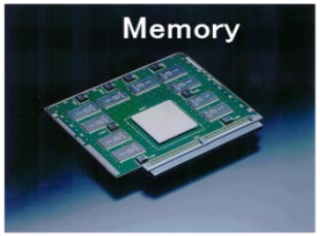


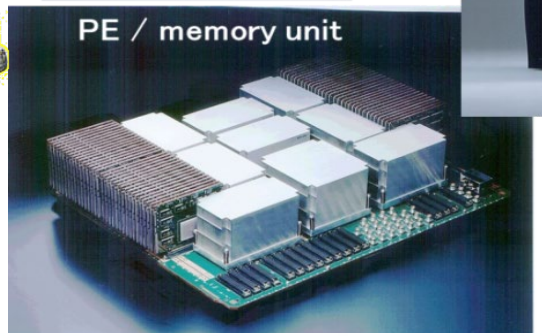
1993 World No.1 Supercomputer NWT (Numerical Window Tunnel) VPP500

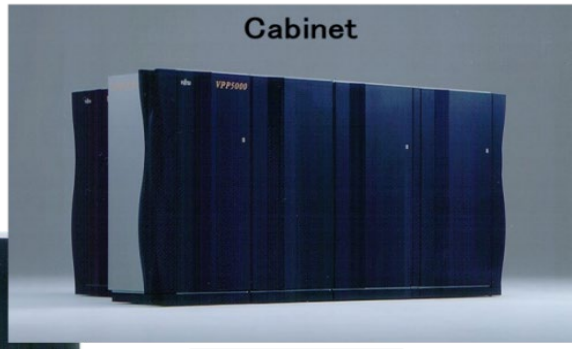
Mr. Hajime Miyoshi

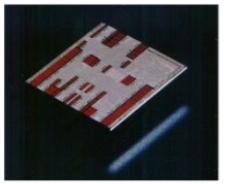
ACM/IEEE SC1994 Washington, D.C. November, 1994



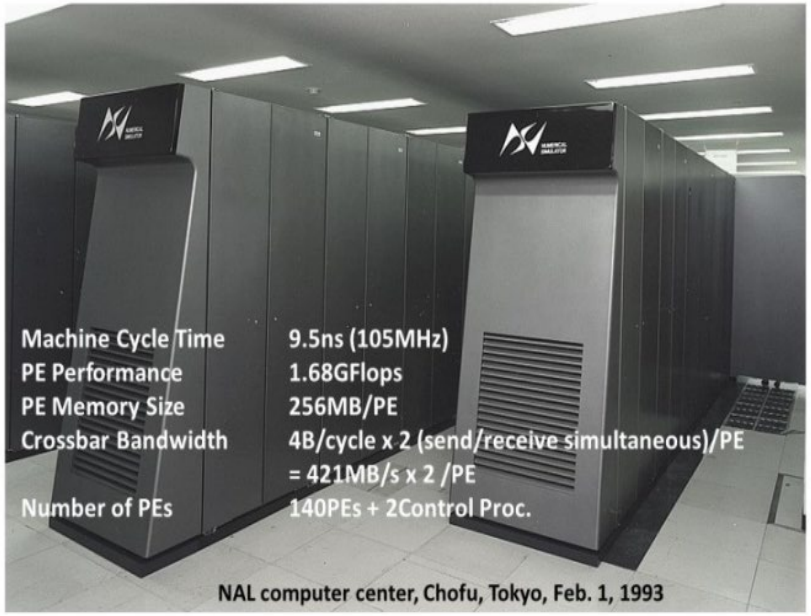


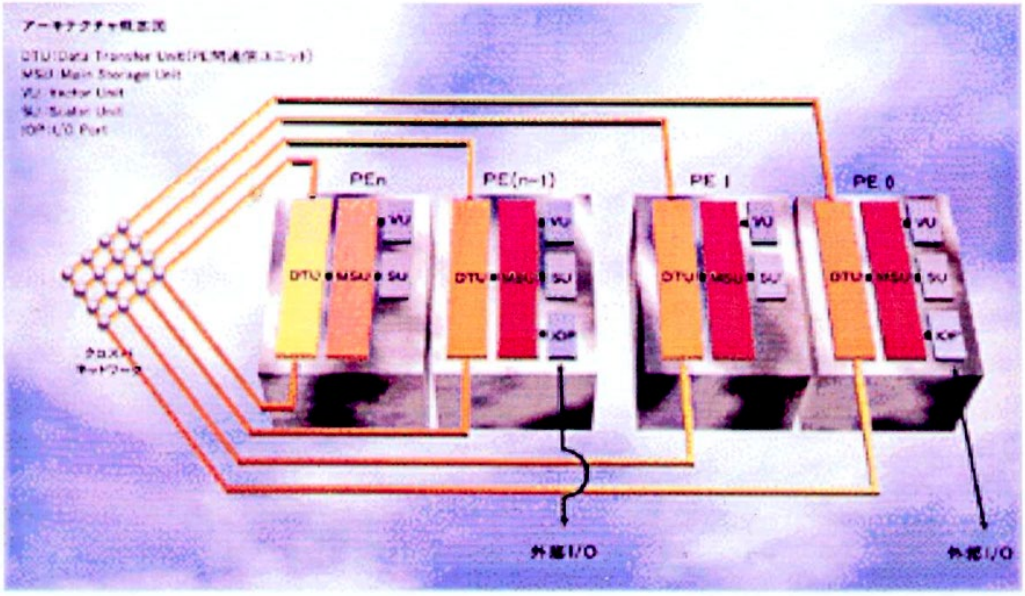






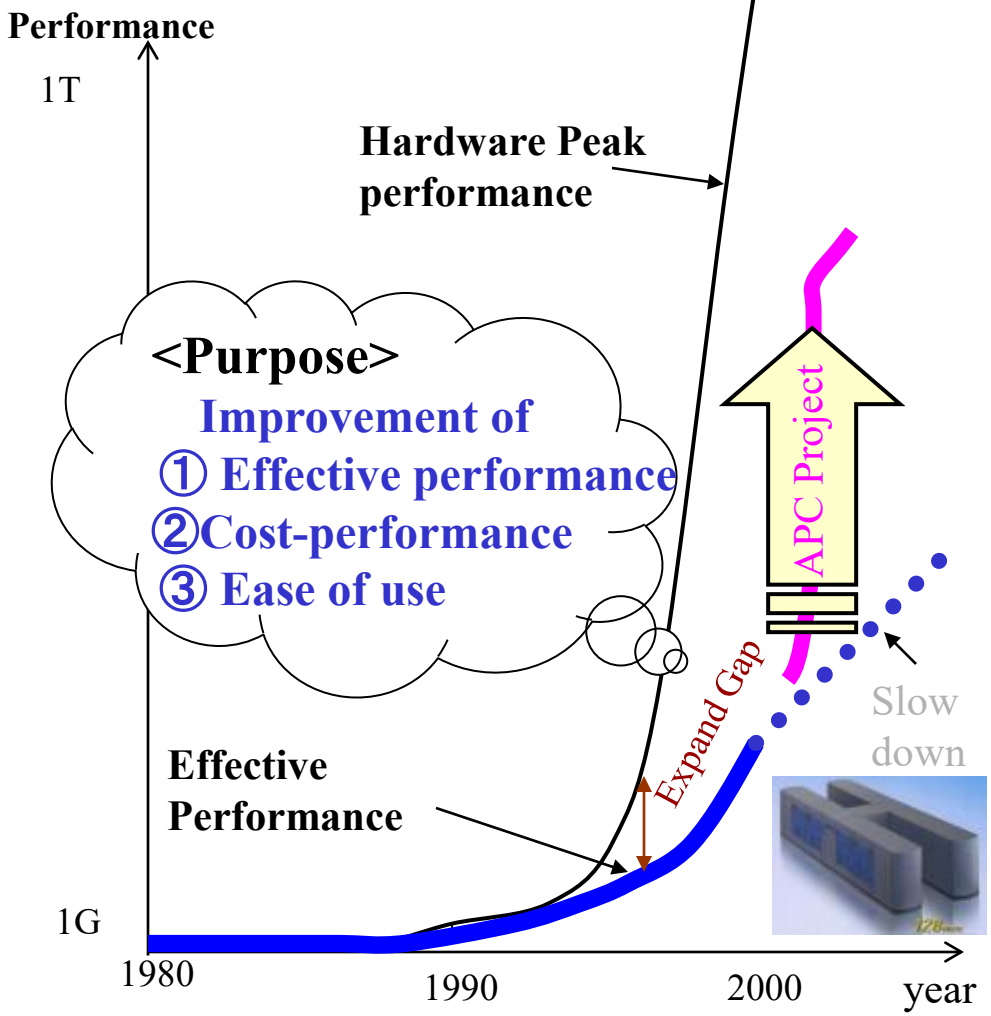
CMOS LSI





METI/NEDO Advanced Parallelizing Compiler Technology Project

Millenium Project IT21 2000.9.8 –2003.3.31
Waseda Univ., Fujitsu, Hitachi, AIST



Theoretical maximum performance vs. Effective performance of HPC

Background and Problems

①Adoption of parallel processing as a core technology on PC to HPC
② Increase of importance of software on IT
③ Need for improvement of cost-performance and usability

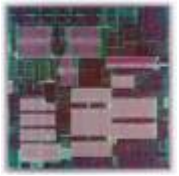
Contents of Research and Development

① R & D of advanced parallelizing compiler
Multigrain, Data localization, Overhead hiding
② R & D of Performance evaluation technology for parallelizing compilers

Goal: Double the effective performance

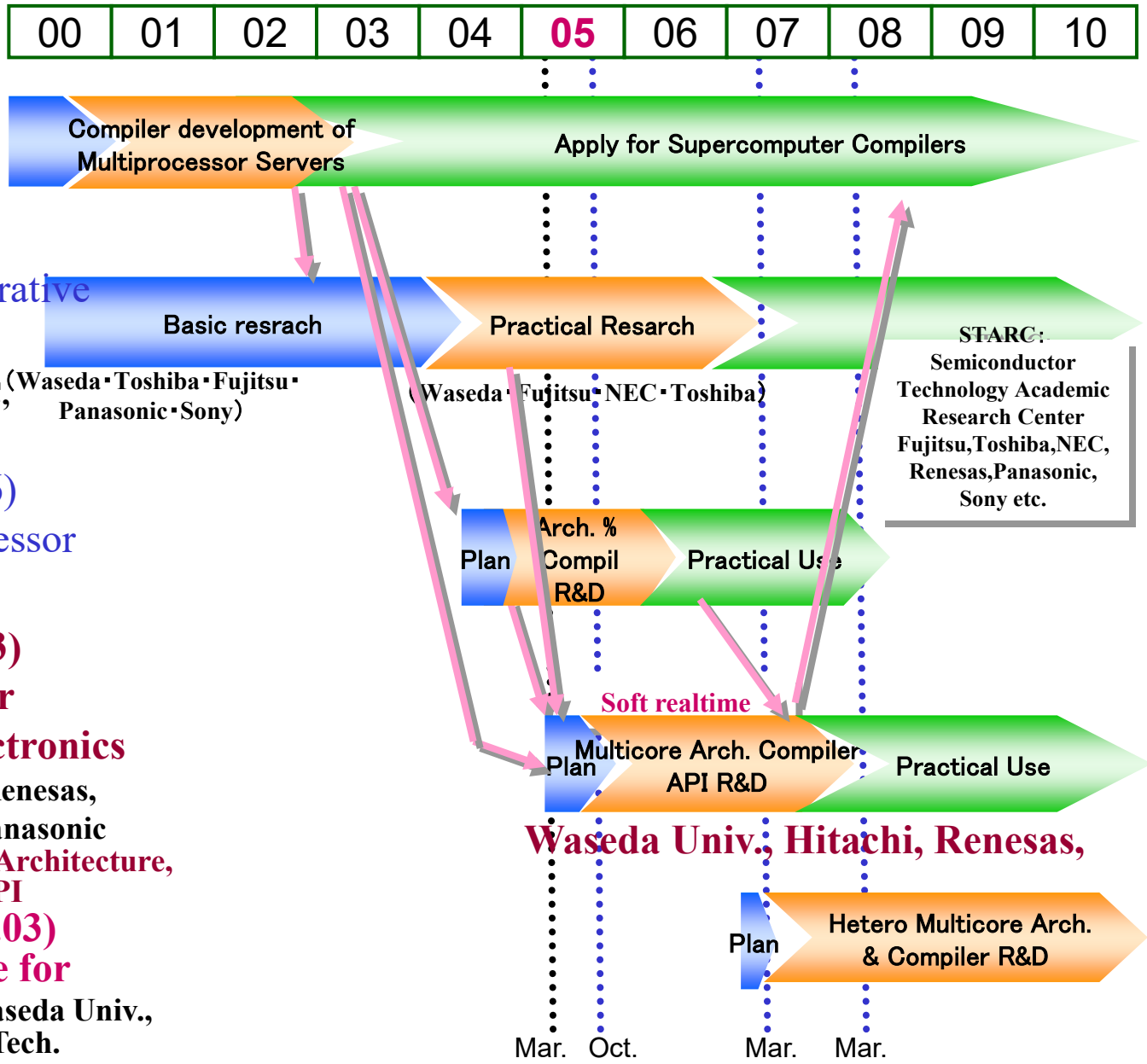
Ripple Effect

① Development of competitive next generation PC and HPC
② Putting the innovative automatic parallelizing compiler technology to practical use
③ Development and market acquisition of future single-chip multiprocessors
④ Boosting R&D in the following many fields:
IT, Bio-tech., Device, Earth environment, Next-generation VLSI design, Financial engineering, Weather forecast, New clean energy, Space development, Automobile, Electric Commerce, etc



Roadmap of compiler cooperative multicore project

- Millennium Project IT21 NEDO Advanced Parallelizing Compiler
  (Waseda Univ. Fujitsu,Hitachi, JIPDEC,AIST)
- STARC Compiler Cooperative Chip Multiprocessor
  (Waseda Univ., Fujitsu, NEC, Toshiba, Panasonic,Sony)
- NEDO (2004.07-2007.06) Heterogeneous Multiprocessor
  (Waseda Univ., Hitachi)
- **NEDO (2005.06-2008.03) Multicore Technology for Realtime Consumer Electronics**
  - Waseda Univ., Hitachi, Renesas, Fujitsu, NEC, Toshiba, Panasonic
    - ➢Power Saving Multicore Architecture, Parallelizing Compiler,API
- **NEDO (2007.02- 2010.03) Heterogeneous Multicore for Consumer Electronics** Waseda Univ., Hitachi, Renesas, Tokyo Inst, of Tech.



METI/NEDO National Project

Multi-core for Real-time Consumer Electronics

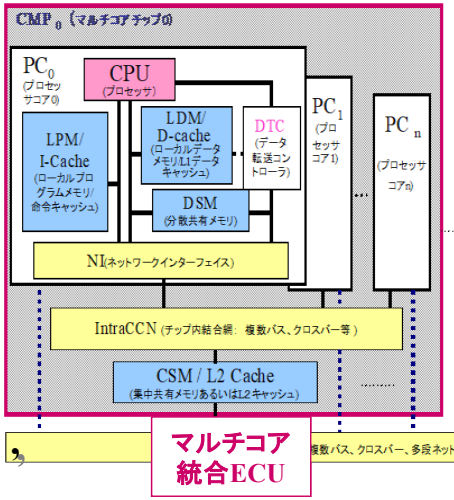
<Goal> R&D of compiler cooperative multi-core processor technology for consumer electronics like Mobile phones, Games, DVD, Digital TV, Car navigation systems.

<Period> From July 2005 to March 2008 (2005.7～2008.3)**

<Features>

- Good cost performance
- Short hardware and software development periods
- Low power consumption
- Scalable performance improvement with the advancement of semiconductor
- Use of the same parallelizing compiler for multi-cores from different vendors using newly developed API

API : Application Programming Interface



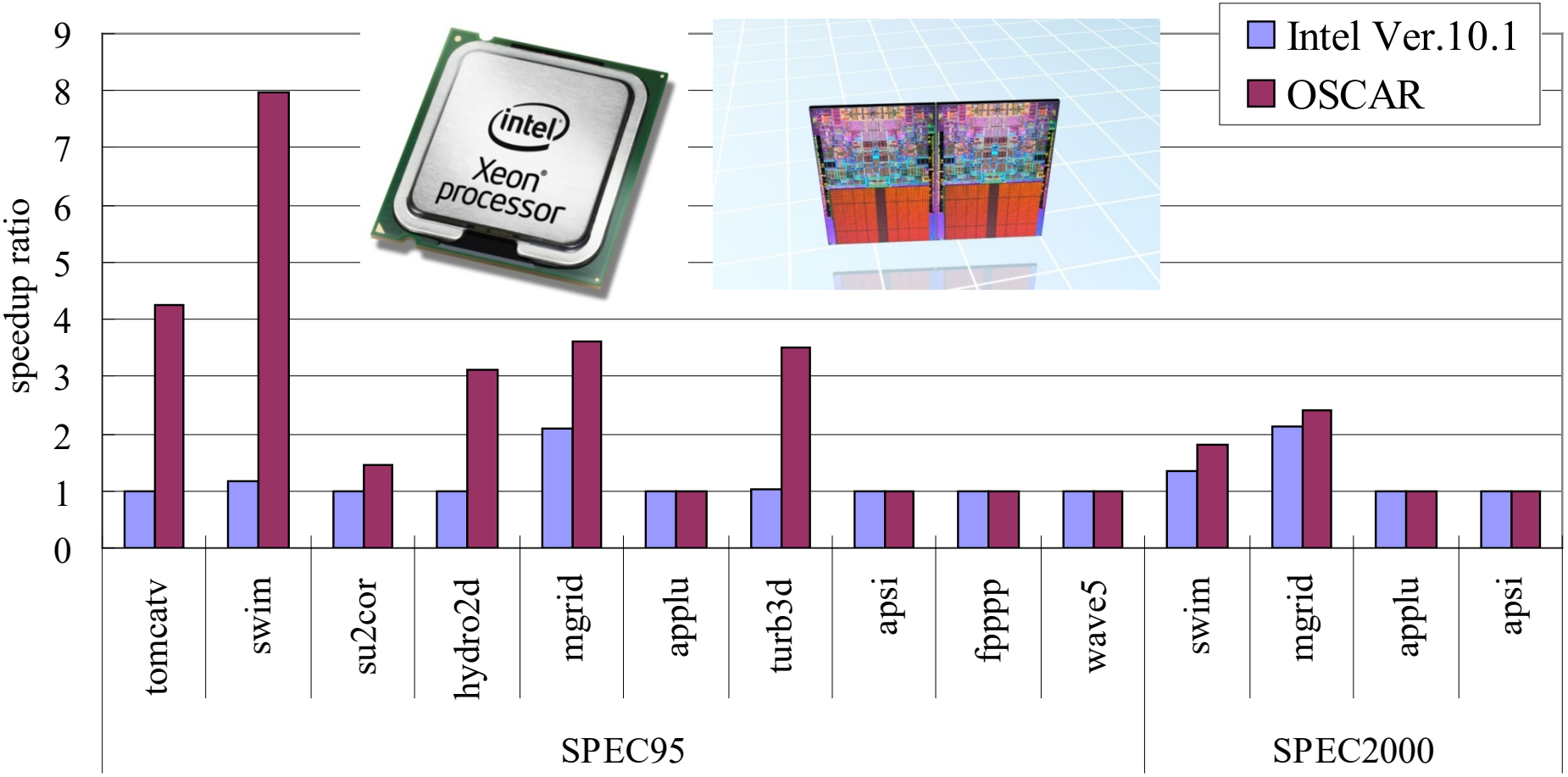
新マルチコアプロセッサ

- 高性能
- 低消費電力
- 短HW/SW開発期間
- 各チップ間でアプリケーション共用可
- 高信頼性
- 半導体集積度と共に性能向上

開発マルチコアチップは情報家電へ

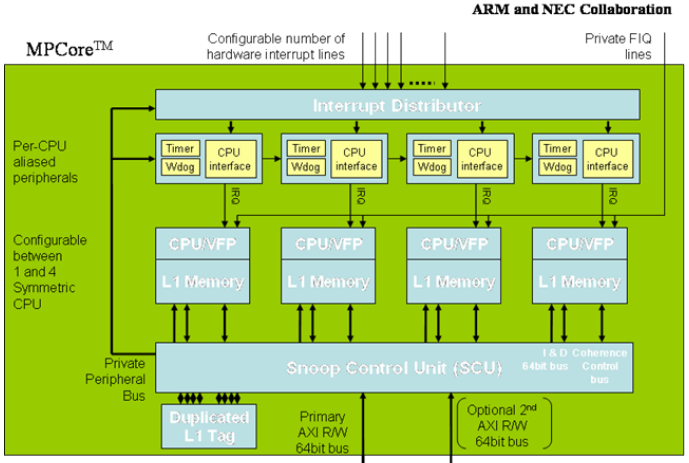
**Hitachi, Renesas, Fujitsu, Toshiba, Panasonic, NEC

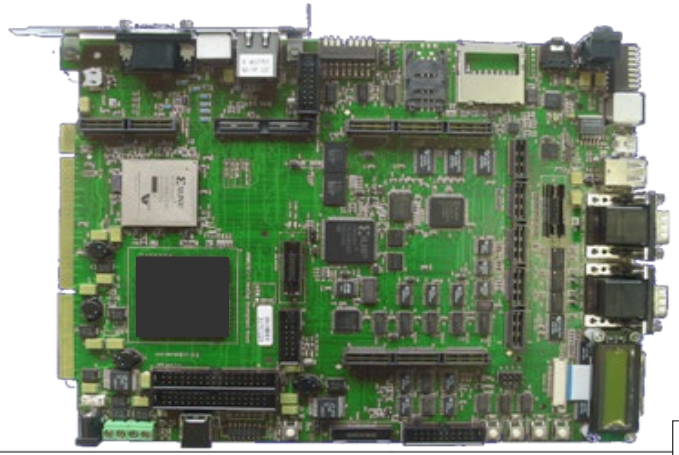
Performance of OSCAR Compiler Using the Multicore API on Intel Quad-core Xeon

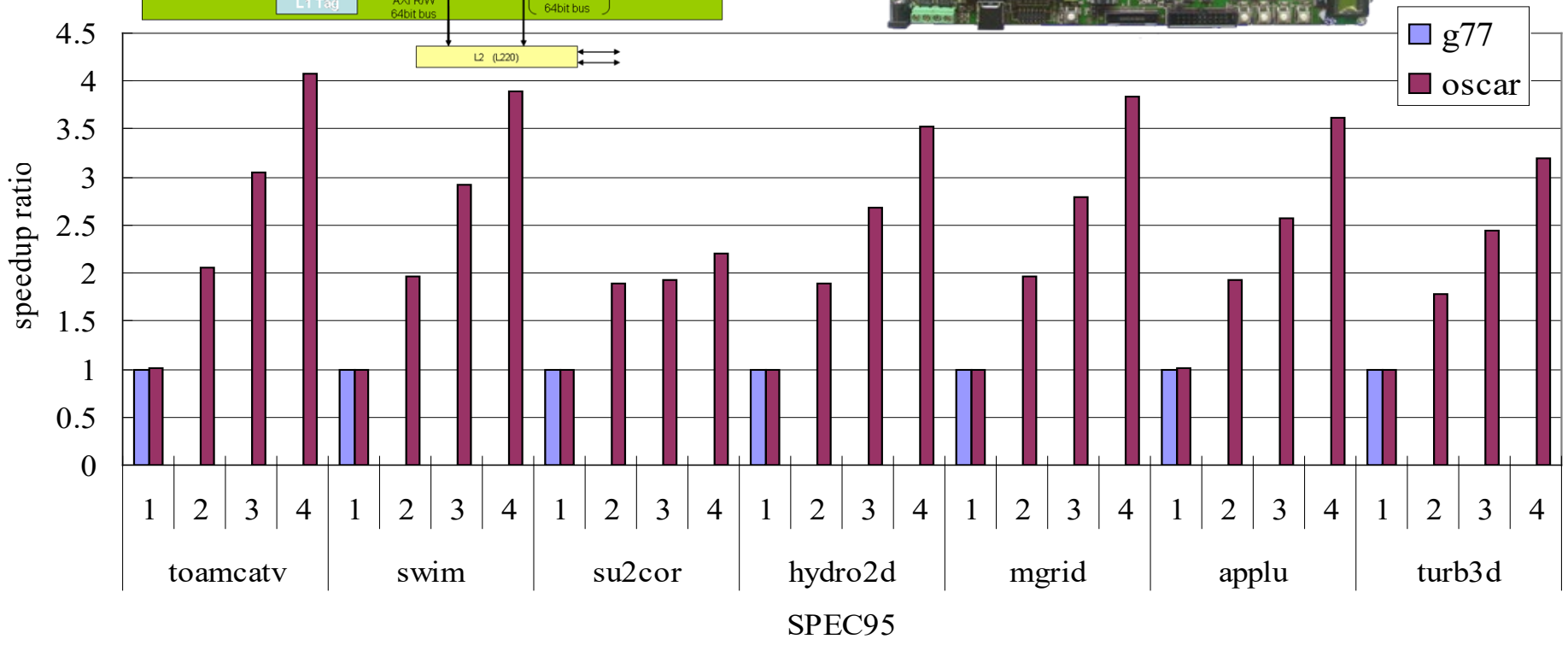


- **OSCAR Compiler gives us 2.09 times speedup on the average against Intel Compiler ver.10.1**

NEC/ARM MPCore Embedded 4 core SMP



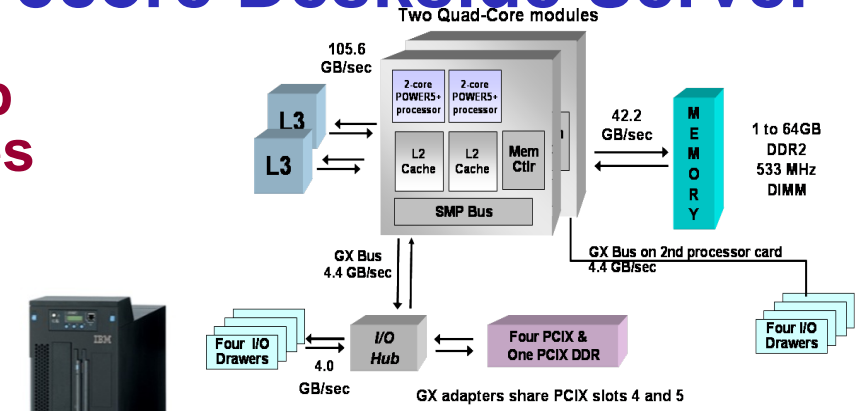




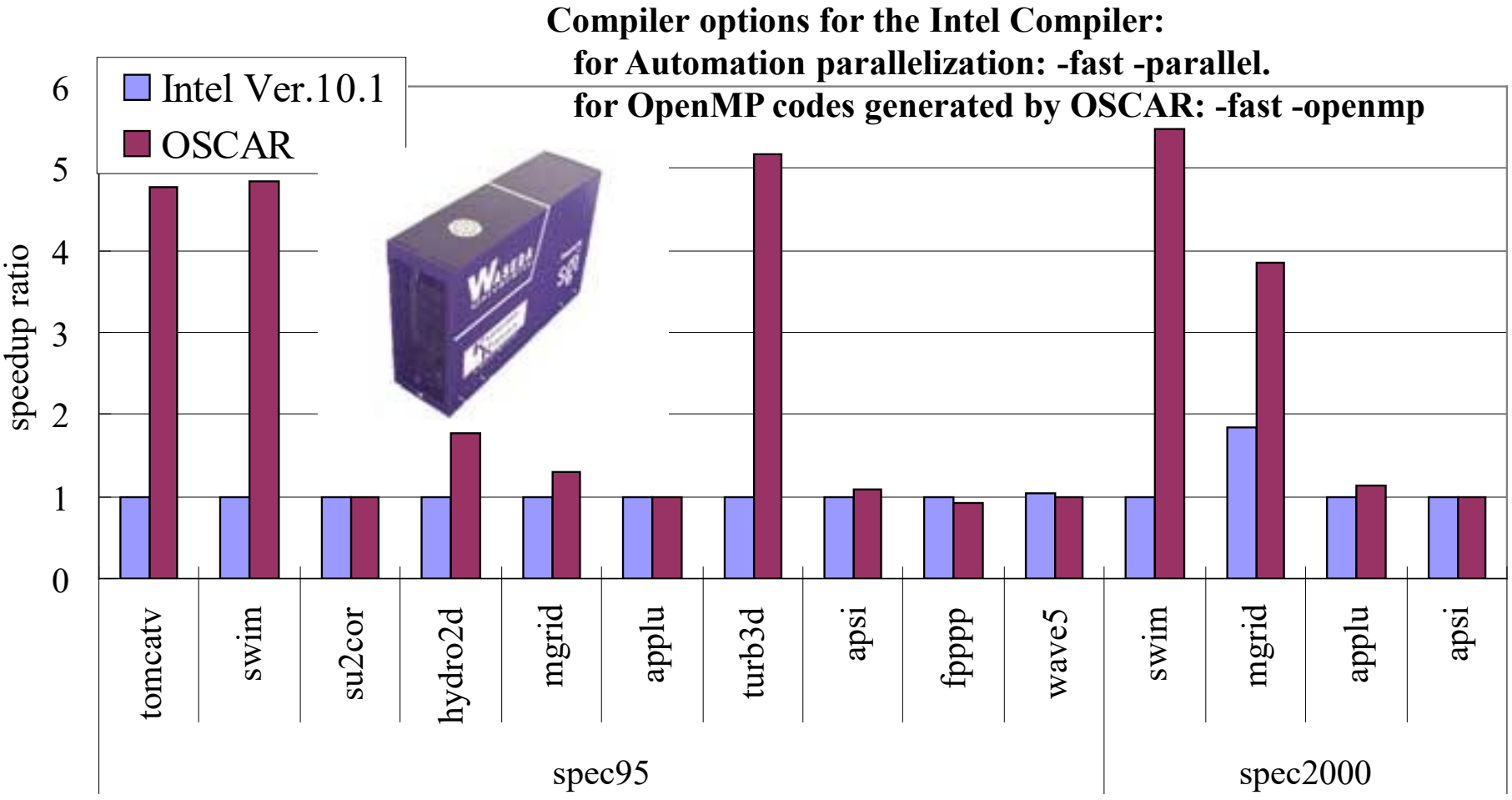
3.48 times speedup by OSCAR compiler against sequential processing

Performance OSCAR Multigrain Parallelizing Compiler on a IBM p550q 8core Deskside Server

- 2.7 times speedup against loop parallelizing compiler on 8 cores



Performance of OSCAR compiler on 16 cores SGI Altix 450 Montvale server



- **OSCAR compiler gave us 2.32 times speedup against Intel Fortran Itanium Compiler revision 10.1**

Demo of NEDO Green Multicore Processor for Real Time Consumer Electronics at Council of Science and Engineering Policy on April 10, 2008

http://www8.cao.go.jp/cstp/gaiyo/honkaigi/74index.html

第74回総合科学技術会議【平成20年4月10日】


第74回総合科学技術会議の様子(1)

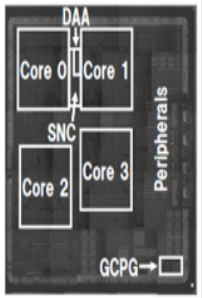
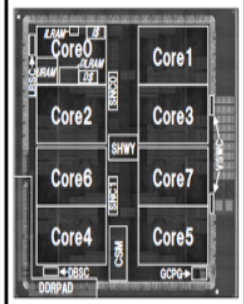
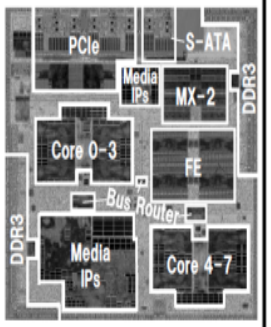
第74回総合科学技術会議の様子(2)


第74回総合科学技術会議の様子(3)


第74回総合科学技術会議の様子(4)

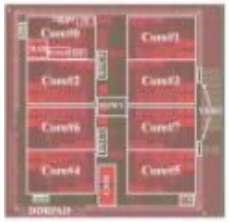
Codesign of Compiler and Multiprocessor Architecture since 1985

4 core multicore RP1 (2007), 8 core multicore RP2 (2008) and 15 core Heterogeneous multicore RPX (2010) developed in NEDO Projects with Hitachi and Renesas

RP-1 (ISSCC2007 #5.3)	*RP-2* (ISSCC2008 #4.5)	*RP-X* (ISSCC2010 #5.3)
		
90nm, 8-layer, triple-Vth, CMOS	90nm, 8-layer, triple-Vth, CMOS	45nm, 8-layer, triple-Vth, CMOS
97.6 mm^2 (9.88 x 9.88 mm)	104.8 mm^2 (10.61 x 9.88 mm)	153.8 mm^2 (12.4 x 12.4 mm)
1.0V (internal), 1.8/3.3V (I/O)	1.0-1.4V (internal), 1.8/3.3V (I/O)	1.0-1.2V (internal), 1.2-3.3V (I/O)
600MHz ,4.32 GIPS,16.8 GFLOPS	600MHz , 8.64 GIPS, 33.6 GFLOPS	648MHz, 13.7GIPS, 115GOPS, 36.2GFLOPS
11.4 GOPS/W (32b換算)	18.3 GOPS/W (32b換算)	37.3 GOPS/W (32b換算)

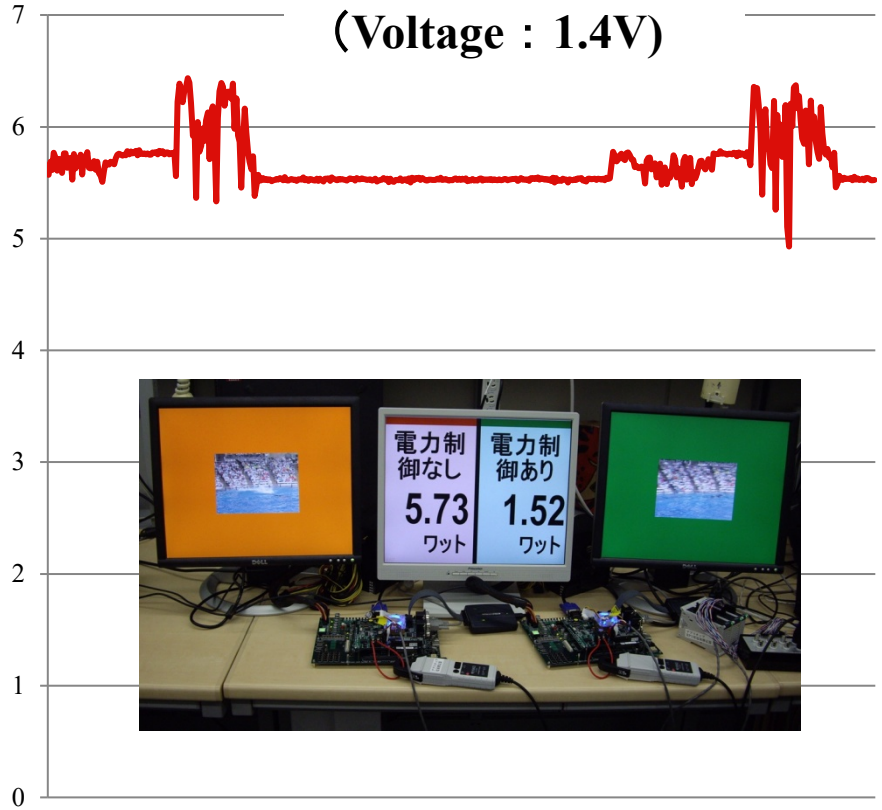
Prime Minister FUKUDA is touching our multicore chip during execution.

Power Reduction of MPEG2 Decoding to 1/4 on 8 Core Homogeneous Multicore RP-2 by OSCAR Parallelizing Compiler

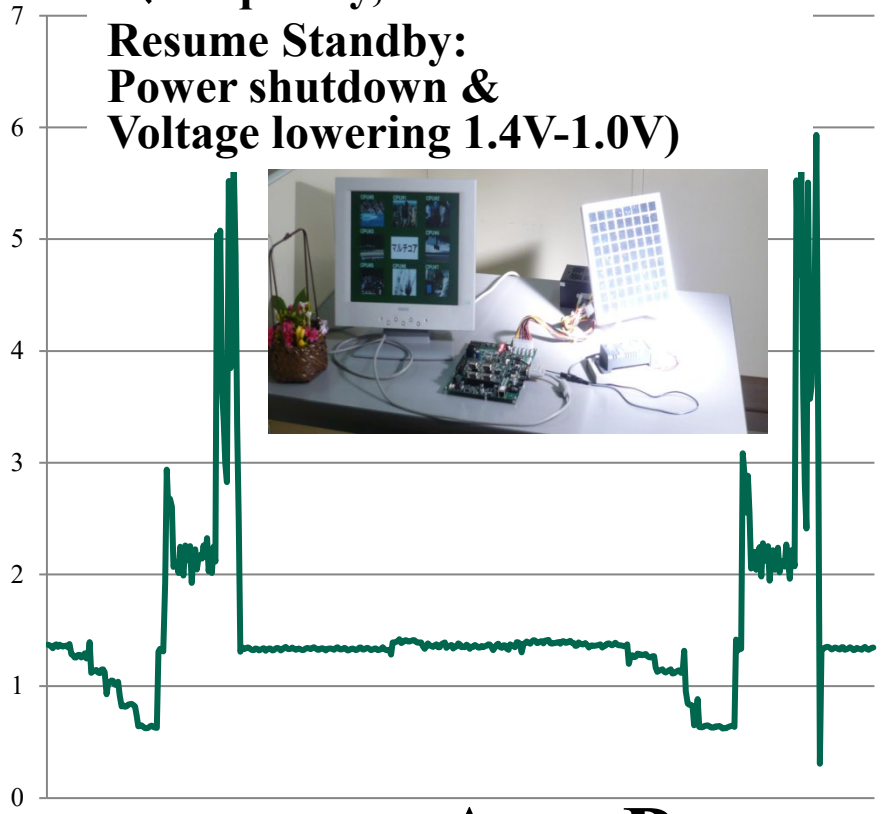


MPEG2 Decoding with 8 CPU cores

Without Power Control (Voltage : 1.4V)



With Power Control (Frequency, Resume Standby: Power shutdown & Voltage lowering 1.4V-1.0V)



Avg. Power 5.73 [W]

73.5% Power Reduction

Avg. Power 1.52 [W]

Green Computing Systems R&D Center

Waseda University

Established by Prof. Kasahara supported by METI (Mar. 2011)

＜R & D Target＞

Hardware, Software, Application for Super Low-Power Manycore

- **More than 64 cores**
- **Natural air cooling (No fan)**
  Cool, Compact, Clear, Quiet
- **Operational by Solar Panel**

<Industry, Government, Academia>

Hitachi, Fujitsu, NEC, Renesas, Olympus, Toyota, Denso, Mitsubishi, Toshiba, NTT, NTT Data, OSCAR Technology, etc

＜Ripple Effect＞

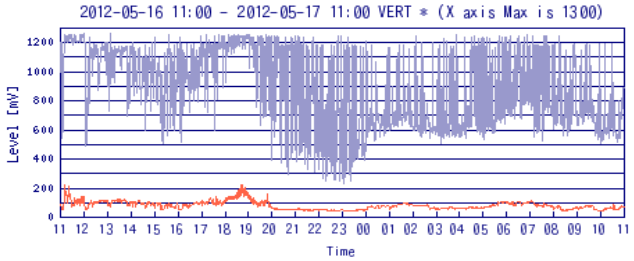
- **Low CO_2 (Carbon Dioxide) Emissions**
- **Creation Value Added Products**
- **Automobiles, Medical, IoT, Servers**

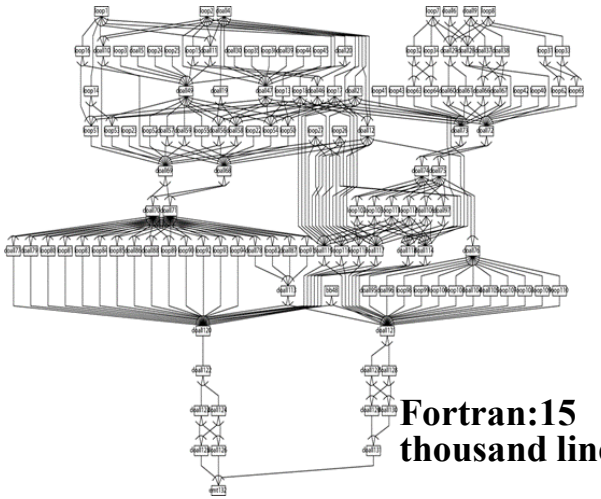
Hitachi SR16000:
Power7 128coreSMP
Fujitsu M9000
SPARC VII 256 core SMP

Beside Subway Waseda Station, Near Waseda Univ. Main Campus

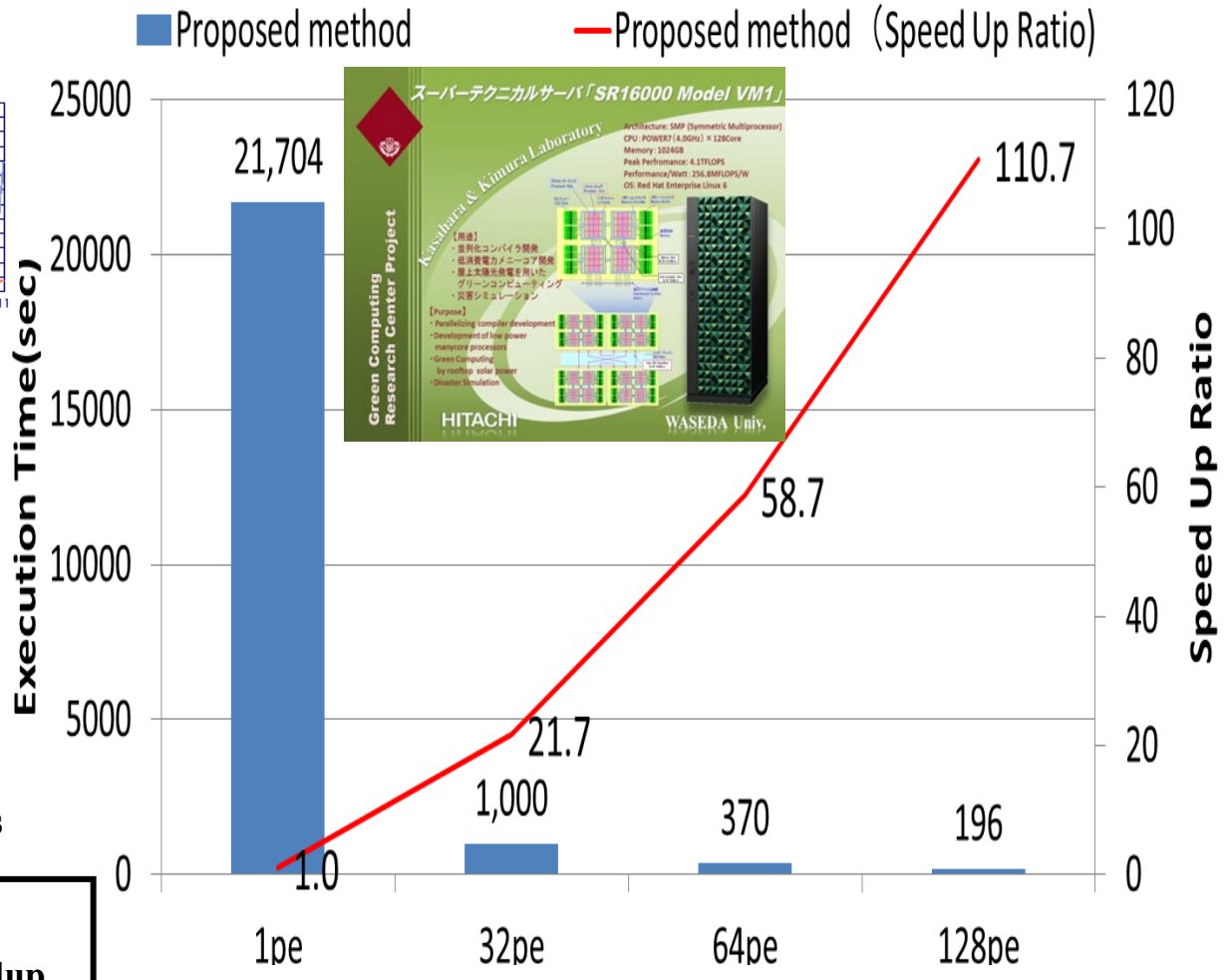
110 Times Speedup against the Sequential Processing for GMS Earthquake Wave Propagation Simulation on Hitachi SR16000

（Power7 Based 128 Core Linux SMP） (LCPC2015)





Fortran:15 thousand lines

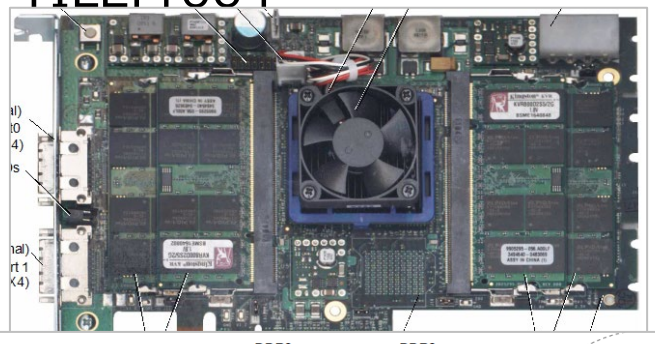


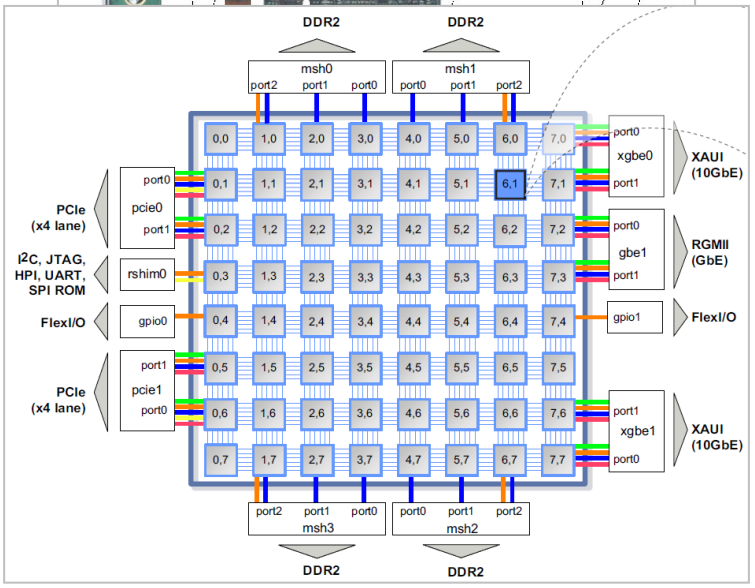
First touch for distributed shared memory and cache optimization over loops are important for scalable speedup

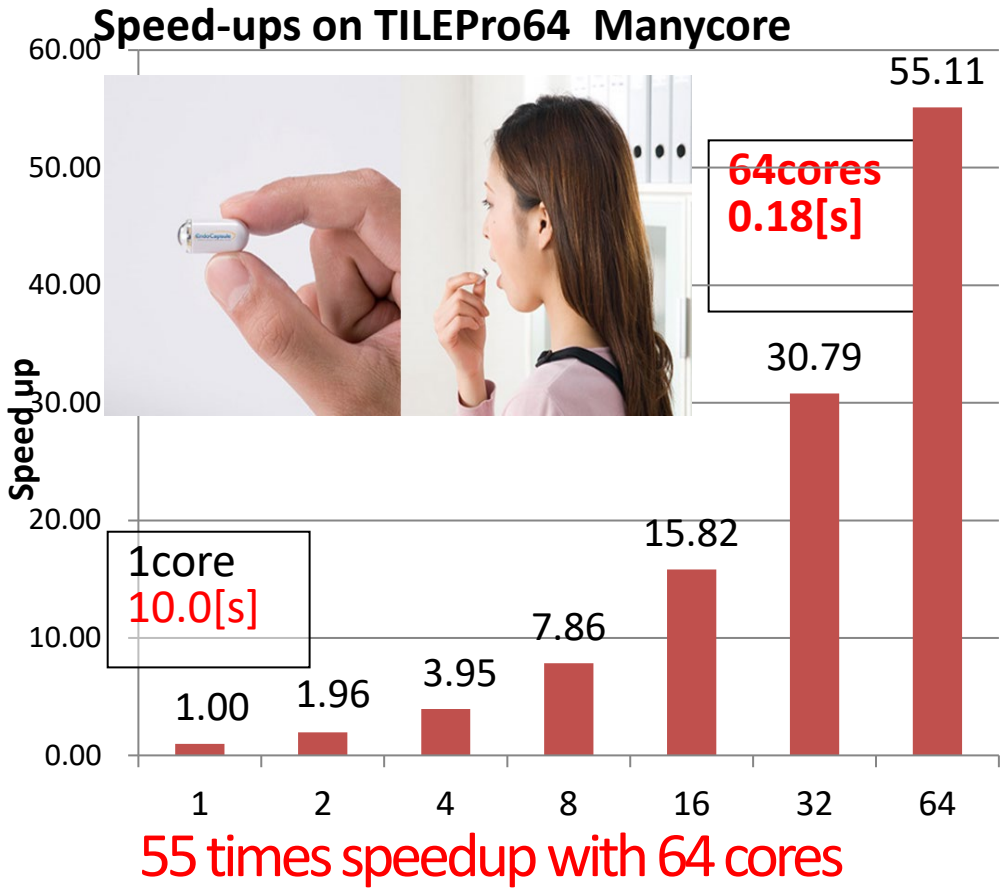
Automatic Parallelization of JPEG-XR for Drinkable Inner Camera (Endo Capsule)

10 times more speedup needed after parallelization for 128 cores of Power 7. Less than 35mW power consumption is required.

- TILEPro64



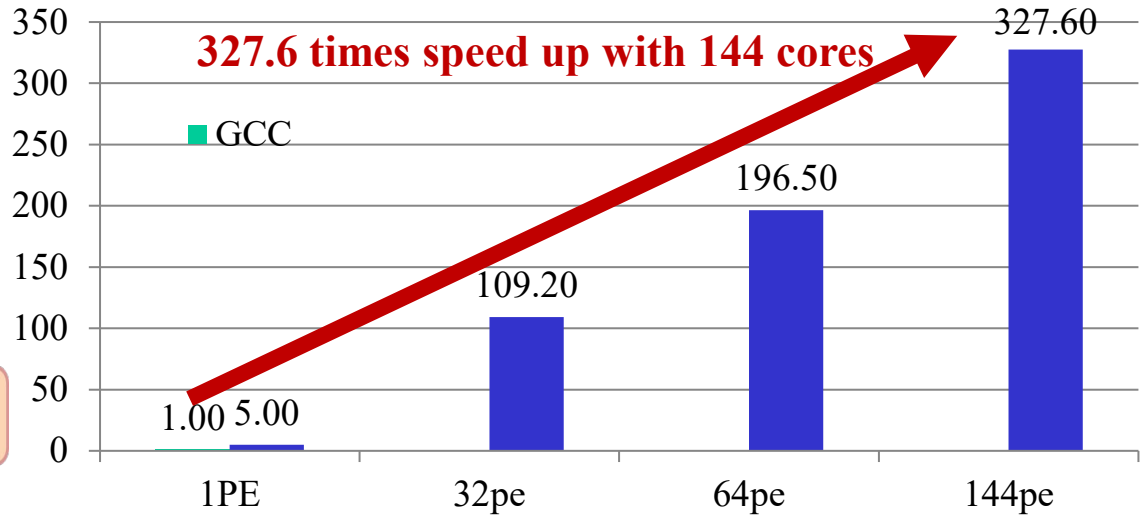




Performance on Multicore Server for Latest Cancer Treatment Using Heavy Particle (Proton, Carbon Ion)

327 times speedup on 144 cores

Hitachi 144cores SMP Blade Server BS500:
Xeon E7-8890 V3(2.5GHz　18core/chip) x8 chip



- Original sequential execution time 2948 sec（50 minutes）using GCC was reduced to 9 sec with 144 cores（327.6 times speedup）
  - Reduction of treatment cost and reservation waiting period is expected

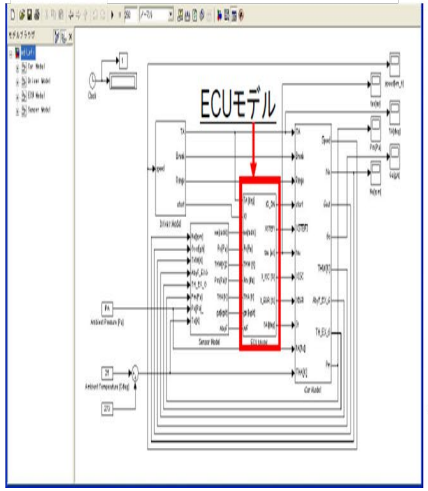
1.95 times speedup of Japanese automobile engine control on Renesas Electronics two processor core ECU with Denso

8.7 times speedup of European Tractor Engine Control on Infineon 2 core multicore by memory usage optimization and parallelization.

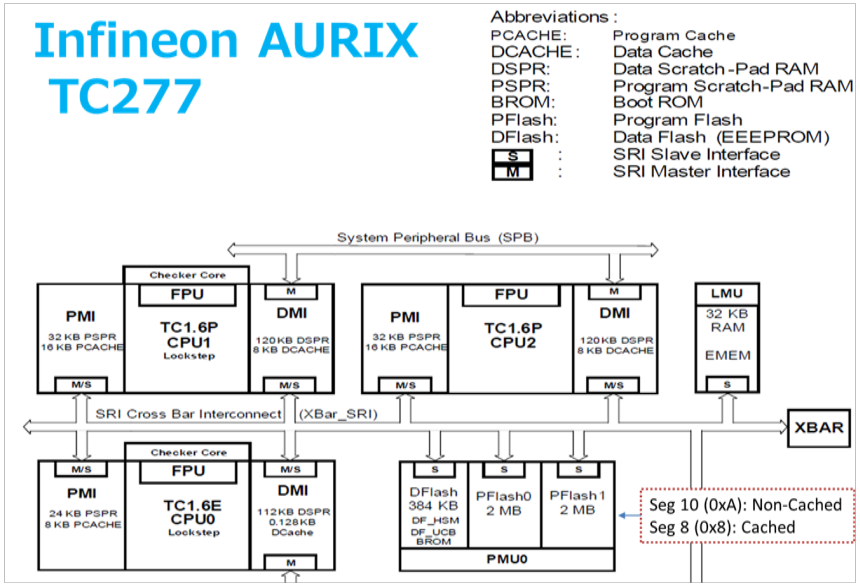
Engine Control by multicore with Denso

Though so far parallel processing of the engine control on multicore has been very difficult, Denso and Waseda succeeded 1.95 times speedup on 2core V850 multicore processor.

- Hard real-time automobile engine control by multicore using local memories
- Millions of lines C codes consisting conditional branches and basic blocks

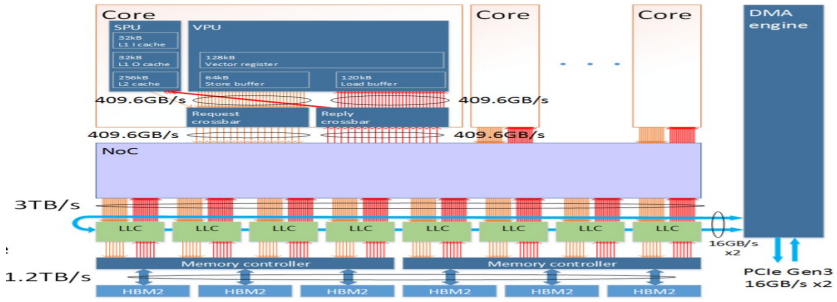


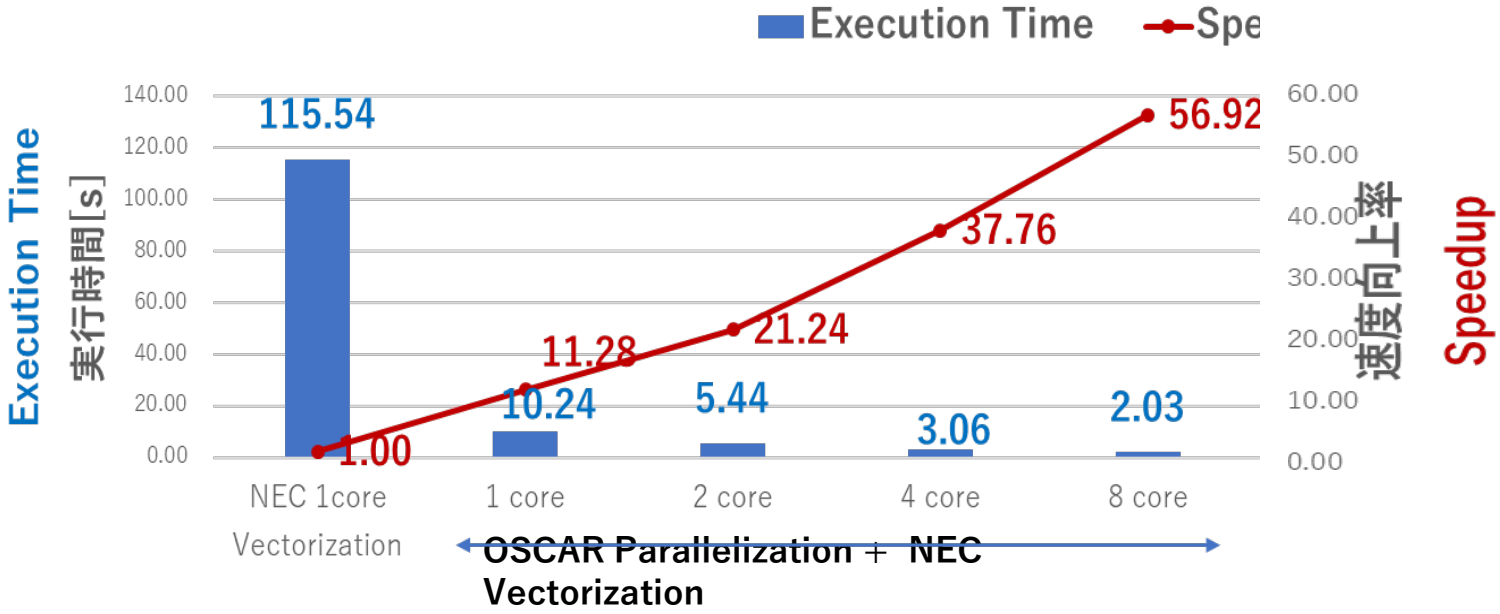
Automatic Parallelization of an Engine Control C Program with 400 thousands lines on AUTOSAR on 2 cores of Infineon AURIX TC277



Speedup of NPB/CG by OSCAR Compiler on NEC SX-Aurora TSUBASA A100-1 8 cores 10C VE

57 times speed up for 8 core Parallelization by OSCAR Compiler & NEC Vectorization against NEC 1 core Vectorization





https://www.oscartech.jp/product

"OSCAR Multicore Suite" is a new product from OSCAR Technology based on the OSCAR Parallelizing Compiler developed by Prof. Hironori Kasahara & Prof. Keiji Kimura Group at Waseda University.

The research OSCAR Compiler has functions, such as Multigrain Parallelization using coarse grain task parallelism, loop parallelism and statement-level fine-grain parallelism, memory access optimization over tasks for coherent cache, no-coherent cache and distributed shared memory, power reduction using DVFS, Clock & Power Gating. It can generate parallel machine codes for various multicores from Intel, AMD, IBM, arm, RISC-V and so on. https://www.linkedin.com/in/hironori-kasahara-b6712855/detail/recent-activity/shares/

OSCAR Multicore Suite is a software suite for assist parallelizing applications. A sequential C code is accepted as input.

- OSCAR Multicore Estimator : Analyze C code statically and estimate execution time. Data dependency and loop parallelization is reported.
- OSCAR Multicore Profiler : Assist software profiling. Automatically insert the code for time measurement to minimize its overhead.
- OSCAR Parallel Compiler : Automatically generates parallel C code from a sequential C code. This tool utilize both loop parallelism and task parallelism.

IEEE Computer Society

The first President from outside North America in 72 years history of IEEE CS

Bjarne Stroustrup: Morgan Stanley & Columbia Univ.
2018 IEEE Computer Society Computer Pioneer Award

2018年に早大笠原がIEEE CS (1946年設立)72年の歴史の中で初めて、北米以外から会長に選出

July 26, 2018, Keynote, Hitotsubashi Hall

July 25, 2018 Award Ceremony
Rihga Royal Hotel Tokyo

- 84,000+ members
- 480 chapters
- 168 countries
- 31 technical committees & councils

ACM/IEEE SC (SuperComputing) 19, Denver, Nov.17-22, 2019

Cornel Univ. Prof. Steven Squyres: Mars Exploration, Caltech. Dr. Katie Bouman:Visualization of Blackhole

WASEDA University -早稲田大学-

Number of International Students

7,942* from 125* countries and territories

(Undergraduate and Graduate)

Alumni CEOs in Japan

10,606

8 Prime Ministers

Founder Shigenobu OKUMA

Graduate Employability

#1 in private university of Japan

(#2 in Japan, #27 in the world)

QS Graduate Employability Rankings 2019

ENROLLMENT [学生数]	ALUMNI [卒業生]
49,436	630,000
	FACULTY [教員]
	5,468

World Business

5 Palmes in Eduniversal Busine

Masaru IBUKA

Tadashi YANAI

PARTNER INSTITUTIONS [協定大学・機関]	NUMBER OF BOOKS [図書館蔵書]	GRADUATE STUDENTS [大学院生]	UNDERGRADUAT STUDENTS [学部生]
848 (93 countries)	5,800,000	8,385	41,051

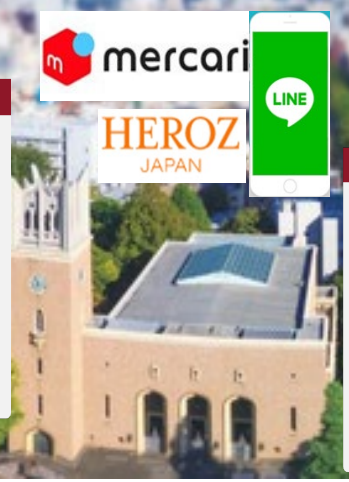
Hiroshi YAMAUCHI

Prime Ministers	Business Leaders Founders of global companies	Business Leaders CEOs of global companies
8th Shigenobu Okuma	Sony	ANA (All Nippon Airways)
17th Shigenobu Okuma	Samsung	HONDA
55th Tanzan Ishibashi	Casio	Nintendo
74th Noboru Takeshita	LOTTE	UNIQLO
76th Toshiki Kaifu		Shiseido
84th Keizo Obuchi		Nomura Securities Co., Ltd.
85th Yoshiro Mori		Tokio Marine & Nichido Fire Insurance Co., Ltd.
91st Yasuo Fukuda		Olympus Corporation
95th Yoshihiko Noda		

mercari

HEROZ JAPAN

LINE



Aiji TANAKA	Hironori KASAHARA
	
President International Political Science Association (IPSA) President 2016	Senior Executive Vice President IEEE Computer Society President 2018. The first president from outside USA and Canada in 72 years CS history. CS has 84,000 members from, 168 countries.

Toshio FUKUDA

The University Professor Waseda, Waseda Alumnus, Prof. Emeritus Nagoya Univ., Prof. Meijo Univ.
IEEE President 2020. The first from Asia in 135 years history.
IEEE has 420,000 members.

Haruki MURAKAMI

Hirokazu KOREEDA

Yuzuru HANYU

S. ARAKAWA

Daiya SETO

THE World Academic Summit, チューリッヒ工科大学,2019.9.10

世界リーディング大学学長・ノーベル賞受賞者パネル

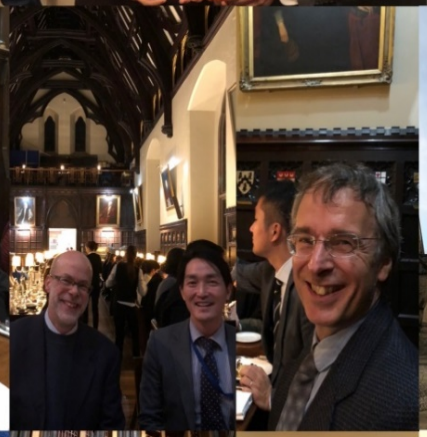
Oxford University, 11/12-13,2019（CSでの招待講演及び連携協議）

Vice Chancellor Prof. Louise Richardson
（WOI 2020で基調講演）
Head of Astrophysics：Prof. Rob Fender
Dept. of Physics: Prof. Ian Shipsey
Astrophysics: Prof. H.Falche, et. al.

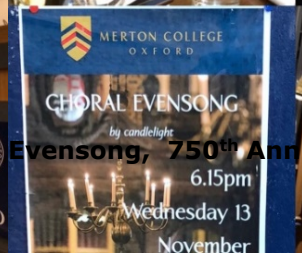
Merton College
Warden: Prof. Irene Tracy（2020年1月に来学）
Fellow: Dr. Peter Braam
Sub Warden: Prof. Judy Armitage
CS: Prof. Jeremy Gibbons













Choral Evensong, 750th Anniversary Room

SISA II: Integrating HPC, Big Data, AI, Quantum Computing and Beyond, Waseda University, Feb. or March, 2022

A Strategic Initiative of Computing: Systems and Applications (SISA)- Integrating HPC, Big Data, AI and Beyond, Jan.18-19, 2017

A Strategic Initiative of Computing:Systems and Applications (SISA) --Integrating HPC, Big Data, AI and Beyond-- Jan. 18-19, 2017

Opening: Prof. Gao, Prof. Kasahara

Waseda VP Shuji Hashimoto

I. Architecture and Applications

Keynote: William J. Dally,
NVIDIA and Stanford University, USA

- Kimihiko Hirao, RIKEN, Japan
- G. W. Yang, Tsinghua Univ. China
- J. Sexton, IBM, USA

II . System Software and Applications

Keynote : Rick. Stevens ANL. USA

- S. Mikhail Smelyanskiy Intel USA
- Fred. Streitz, LLNL USA
- R. Govind, IIS, India
- H. Hironori Kasahara, Waseda Univ,

III. Extreme Scale and Beyond

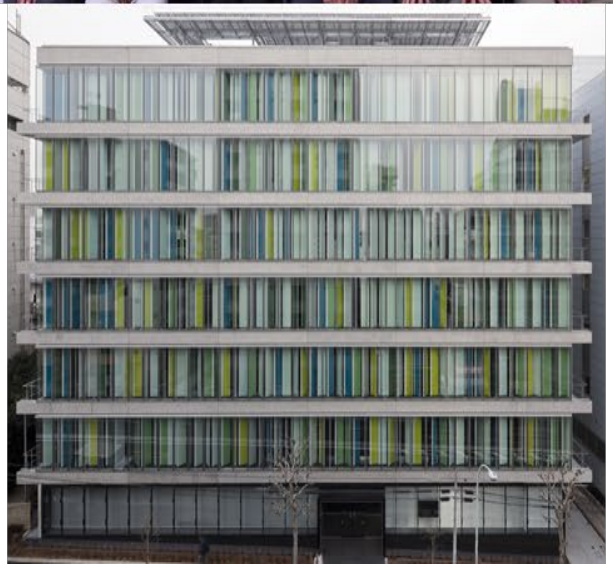
Keynote: Paul Messina ANL, USA

- Motoaki Saito, PEZY, Japan
- Eiji Ishida, MEXT, Japan
- Depei Qian, BUAA, China
- Toshiyuki Shimizu, Fujitsu, Japan

IV. Integration of HPC, Big Data, and AI

Keynote: Thomas Sterling, Indiana Univ., USA

- Masaru Kitsuregawa, NII and Univ. of Tokyo, Japan
- Thomas Schulthess, ETH, Swiss
- Moriyuki Takamura/Toshiaki Kitamura, Oscar Tech, Japan



2021 No.1 Candidate USA AURORA Leader ANL Dr. Stevens(SISA2022 Co-Chair)

ACM/IEEE ISCA in 2024 or 2025

in Waseda University, Tokyo, Japan

Co-Chairs:Jean-Luc Gaudiot (Prof. UCI, IEEE CS President 2017)
Hironori Kasahara (SEVP Waseda, IEEE CS President2018)

ACM/IEEE International Symposium on Computer Architecture にてコンピュータ分野のノーベル賞と言われるチューリング賞記念講演会を早稲田大学大隈講堂で実施予定

Future Multicore Products with Automatic Parallelizing Compiler

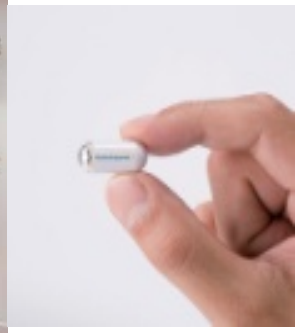
Next Generation Automobiles

- Safer, more comfortable, energy efficient, environment friendly
- Cameras, radar, car2car communication, internet information integrated brake, steering, engine, moter control

Smart phones

-From everyday recharging to less than once a week
- Solar powered operation in emergency condition
- Keep health

Advanced medical systems



Cancer treatment,
Drinkable inner camera

- Emergency solar powered
- No cooling fun, No dust , clean usable inside OP room

Personal / Regional Supercomputers

Solar powered with more than 100 times power efficient : FLOPS/W

- Regional Disaster Simulators saving lives from tornadoes, localized heavy rain, fires with earth quakes