High Performance Green Multicore Computing

Hironori Kasahara, Ph.D., IEEE Fellow

IEEE Computer Society President 2018

Professor, Dept. of Computer Science & Engineering
Director, Advanced Multicore Processor Research Institute

Waseda University, Tokyo, Japan

URL: http://www.kasahara.cs.waseda.ac.jp/

1980 BS, 82 MS, 85 Ph.D. , Dept. EE, Waseda Univ.
1985 Visiting Scholar: U. of California, Berkeley
1986 Assistant Prof., 1988 Associate Prof., 1997,
Waseda Univ., Now Dept. of Computer Sci. & Eng.
1989-90 Research Scholar: U. of Illinois, Urbana-Champaign, Center for Supercomputing R&D
2004 Director, Advanced Multicore Research
Institute, 2017 member: the Engineering Academy
of Japan and the Science Council of Japan

2005 STARC Academia-Industry Research Award
2008 LSI of the Year Second Prize
2008 Intel AsiaAcademic Forum Best Research Award
2010 IEEE CS Golden Core Member Award
2014 Minister of Edu., Sci. & Tech. Research Prize
2015 IPSJ Fellow
2017 IEEE Fellow, IEEE Eta Kappa Nu

Reviewed Papers: 214, Invited Talks: 145, Published
Unexamined Patent Application:59 (Japan, US, GB,
China Granted Patents: 30), Articles in News Papers,
Web News, Medias incl. TV etc.: 572

Committees in Societies and Government   245
IEEE Computer Society President 2018, BoG(2009-14), Multicore STC Chair (2012-), Japan Chair (2005-07), IPSJ Chair: HG for Mag. & J. Edit, Sig. on ARC.
【METI/NEDO】 Project Leaders: Multicore for
Consumer Electronics, Advanced Parallelizing
Compiler, Chair: Computer Strategy Committee
【Cabinet Office】 CSTP Supercomputer Strategic
ICT PT, Japan Prize Selection Committees, etc.
【MEXT】Info. Sci. & Tech. Committee,
Supercomputers (Earth Simulator, HPCI Promo.,
Next Gen. Supercomputer K) Committees, etc.

Hironori Kasahara Voted 2017 IEEE Computer Society President-Elect

LOS ALAMITOS, Calif., 30 September 2016 — Hironori Kasahara, a Professor of Computer Science at Waseda University in Tokyo, and Director of the Advanced Multicore Research Institute, has been voted **IEEE Computer Society 2017 President-Elect.**

Kasahara is a former member of the IEEE-CS Board of Governors, has served as chair of the IEEE-CS Multicore STC and CS Japan Chapter, and board member of the IEEE Tokyo Section. Kasahara will serve as the 2018 IEEE CS President for a one-year term beginning 1 January 2018. Kasahara garnered 3,278 votes, compared with 2,804 votes cast for Hausi A. Müller, a Professor of Computer Science and Associate Dean of Research, Faculty of Engineering at University of Victoria, Canada, and a member of IEEE-CS Board of Governors.

The President oversees IEEE-CS programs and operations and is a nonvoting member of most IEEE-CS program boards and committees. The 2016 election had a 12.69% turnout, with 6,357 ballots cast. The turnout was higher than the 2015 election with and 12.68% turnout (6,239 ballots cast) and the 2014 election with a 12.66% turnout (6,728 ballots cast).

2016 IEEE Computer Society Election Results

Press Release | Ballot counts

Posted 29 September 2016

Hironori Kasahara selected 2017 President-Elect (2018 President)

Hironori Kasahara has served as a chair or member of 225 society and government committees, including a member of the CS Board of Governors; chair of CS Multicore STC and CS Japan chapter; associate editor of IEEE Transactions on Computers; vice PC chair of the 1996 ENIAC 50th Anniversary International Conference on Supercomputing; general chair of LCPC; PC member of SC, PACT, PPoPP, and ASPLOS; board member of IEEE Tokyo section; and member of the Earth Simulator committee.

He received a PhD in 1985 from Waseda University, Tokyo, joined its faculty in 1986, and has been a professor of computer science since 1997 and a director of the Advanced Multicore Research Institute since 2004. He was a visiting scholar at University of California, Berkeley, and the University of Illinois at Urbana–Champaign's Center for Supercomputing R&D.

Kasahara received the CS Golden Core Member Award, IFAC World Congress Young Author Prize, IPSJ Fellow and Sakai Special Research Award, and the Japanese Minister's Science and Technology Prize. He led Japanese national projects on parallelizing compilers and embedded multicores, and has presented 210 papers, 132 invited talks, and 27 patents. His research has appeared in 520 newspaper and Web articles.

IEEE Computer Society BoG (Board of Governors) Feb.1, 2017

https://www.computer.org/web/cshistory/officers-2017

Past IEEE Computer Society Presidents

**Chairs of the IRE Professional Group
on Electronic Computers**
1951-53 Morton M. Astrahan
1953-54 John H. Howard
1954-55 Harry Larson
1955-56 Jean H. Felker
1956-57 Jerre D. Noe
1957-58 Werner Buchholz
1958-59 Willis H. Ware
1959-60 Richard O. Endres
1960-62 Arnold A. Cohen
1962-64 Walter L. Anderson

**Chairs of the AIEE Committee
on Large-Scale Computing Devices**
1946-49 Charles Concordia
1949-51 John Grist Brainerd
1951-53 Walter H. MacWilliams
1953-55 Frank J. Maginniss
1955-57 Edwin L. Harder
1957-59 Morris Rubinoff
1959-61 Ruben A. Imm
1961-63 Claude A. Kagan
1963-64 Gerhard L. Hollander

**Chairs & Presidents of the IEEE
Computer Society**
1964-65 Keith Uncapher
1965-66 Richard I. Tanaka
1966-67 Samuel Levine
1968-69 Charles L. Hobbs
1970-71 Edward J. McCluskey
1972-73 Albert S. Hoagland
1974-75 Stephen S. Yau
1976   Dick B. Simmons
1977-78 Merlin G. Smith
1979-80 Tse-Yun Feng
1981   Richard E. Merwin
1982-83 Oscar N. Garcia
1984-85 Martha Sloan
1986-87 Roy L. Russo
1988   Edward A. Parrish
1989   Kenneth A. Anderson
1990   Helen M. Wood
1991   Duncan H. Lawrie
1992   Bruce D. Shriver
1993   James H. Aylor
1994   Laurel V. Kaleda
1995   Ronald G. Hoelzeman

1996   Mario R. Barbacci
1997   Barry W. Johnson
1998   Doris L. Carver
1999   Leonard L. Tripp
2000   Guylaine M. Pollock
2001   Benjamin W. Wah
2002   Willis K. King
2003   Stephen Diamond
2004   Carl K. Chang
2005   Gerald L. Engel
2006   Deborah M. Cooper
2007   Michael R. Williams
2008   Rangachar Kasturi
2009   Susan K. (Kathy) Land,
2010   James D. Isaak
2011   Sorel Reisman
2012   John W. Walz
2013   David Alan Grier
2014   Dejan S. Milojicic
2015   Thomas M. Conte
2016   Roger U. Fujii
2017 Jean-Luc Gaudiot
2018 Hironori Kasahara

IEEE Computer Society

60,000+ members,   volunteer-led organization,
200 technical conferences, industry-oriented "**Rock Stars**" ,
17 scholarly journals and **13 magazines,   awards program,**
Digital Library with more than 550,000 articles and papers ,
400 local and regional chapters,   40 technical committees,

▮ Region 1 (Northeastern US)	▮ Region 6 (Western US)
▮ Region 2 (Eastern US)	▮ Region 7 (Canada)
▮ Region 3 (Southern US)	▮ Region 8 (Africa, Europe, Middle East)
▮ Region 4 (Central US)	▮ Region 9 (Latin America)
▮ Region 5 (Southwestern US)	▮ Region 10 (Asia and Pacific)

> IEEE-USA (Regions 1-6)

Toward 2018

1. Refining <u>content and services</u> to further improve the <u>satisfaction of CS members</u>;
2. Considering an <u>incentive for volunteers</u> to further accelerate CS activities and promptly provide technical benefits for people around the globe;
   <u>To express appreciation to volunteers:</u>
   <u>CS Point (Mileage) System: Annual & Life Time Honor,</u>
   <u>Premier Seating, Premier Registration, Distinguished Reviewer,</u> etc
3. Offering more <u>attractive services</u> for practitioners in <u>industry</u>;
4. Providing the <u>world's best educational content</u> and historical treasures for future generations, which only the CS can create with our pioneering researchers (for example, the Multicore Compiler Video Series found at www.computer.org/web/education/multicore-video-series);
5. Thinking about <u>sustainable membership fees</u> while considering the diversity of economic situations within the 10 regions;
6. <u>Cooperating</u> with <u>other IEEE societies and sister societies</u> in a timely and efficient manner;
7. Intelligibly introducing the latest computer-related technologies to <u>younger generations, including children</u>, so that they can realize their technological dreams.

IEEE
Φcomputer
society

IEEE
Advancing Technology
for Humanity

Multicores for Performance and Low Power

Power consumption is one of the biggest problems for performance scaling from smartphones to cloud servers and supercomputers ("K" more than 10MW) .
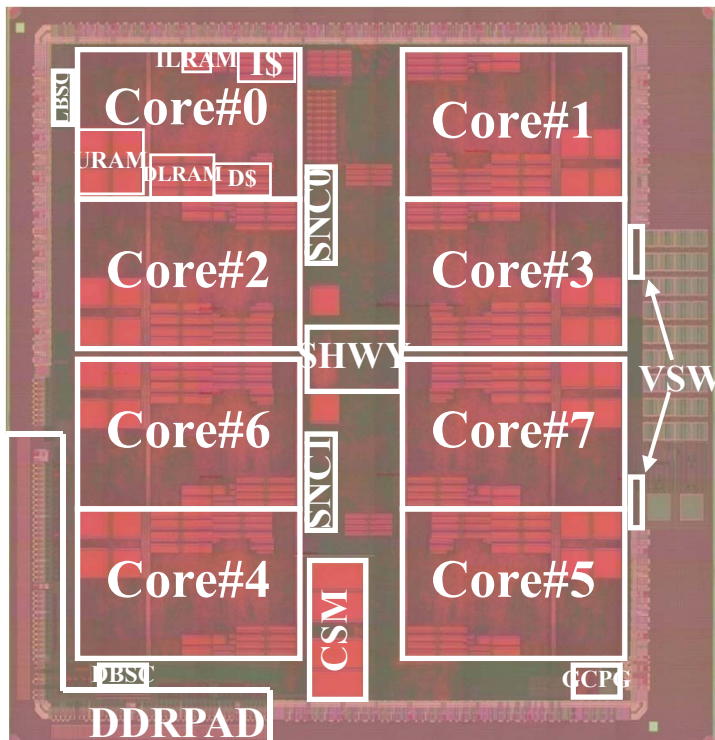
IEEE ISSCC08: Paper No. 4.5, M.ITO, … and H. Kasahara, "An 8640 MIPS SoC with Independent Power-off Control of 8 CPUs and 8 RAMs by an Automatic Parallelizing Compiler"

Power $\propto$ Frequency * Voltage^2
(Voltage $\propto$ Frequency)
⇒ **Power $\propto$ Frequency^3**

If Frequency is reduced to 1/4
(Ex. 4GHz→1GHz),
Power is reduced to 1/64 and
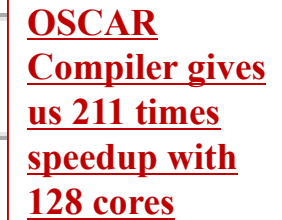**Performance falls down to 1/4 .**
<Multicores>
If 8cores are integrated on a chip,
Power is still 1/8 and
Performance becomes 2 times.

Parallel Soft is important for scalable performance of multicore (LCPC2015)

➢ **Just more cores don't give us speedup**
➢ **Development cost and period of parallel software are getting a bottleneck of development of embedded systems, eg. IoT, Automobile**

Earthquake wave propagation simulation GMS developed by National Research Institute for Earth Science and Disaster Resilience (NIED)

Fjitsu M9000 SPARC Multicore Server

■ original (sun studio)   ■ proposed method

OSCAR Compiler gives us 211 times speedup with 128 cores

Commercial compiler gives us 0.9 times speedup with 128 cores (slow-downed against 1 core)

➢ **Automatic parallelizing compiler available on the market gave us no speedup against execution time on 1 core on 64 cores**
  ➢ Execution time with 128 cores was slower than 1 core (0.9 times speedup)
➢ **Advanced OSCAR parallelizing compiler gave us 211 times speedup with 128cores against execution time with 1 core using commercial compiler**
  ➢ OSCAR compiler gave us 2.1 times speedup on 1 core against commercial compiler by global cache optimization
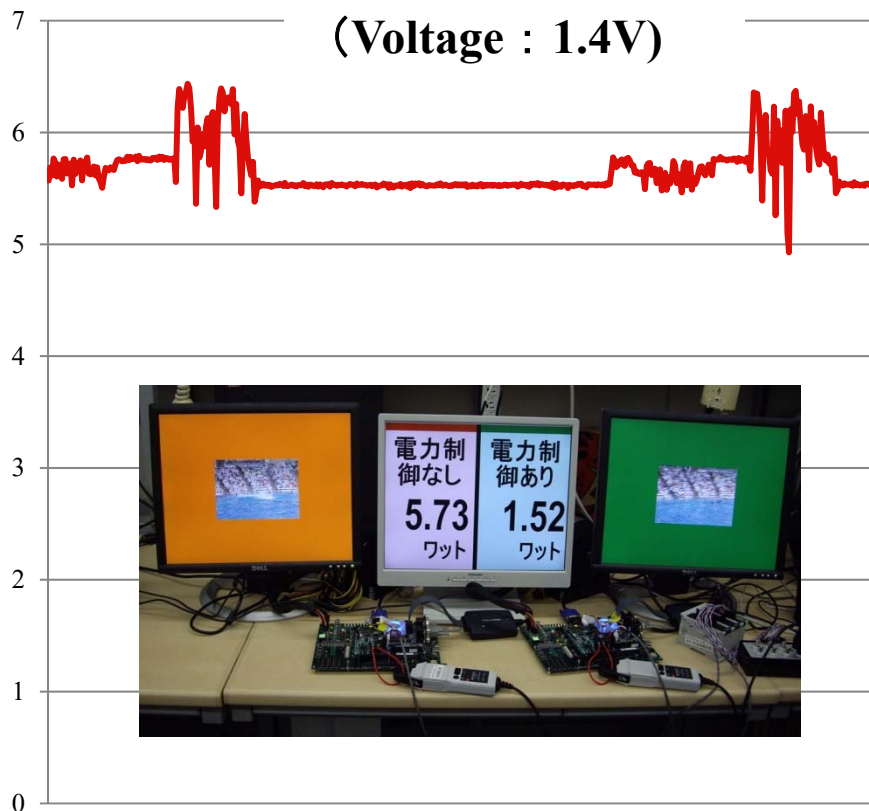
8

Power Reduction of MPEG2 Decoding to 1/4 on 8 Core Homogeneous Multicore RP-2 by OSCAR Parallelizing Compiler
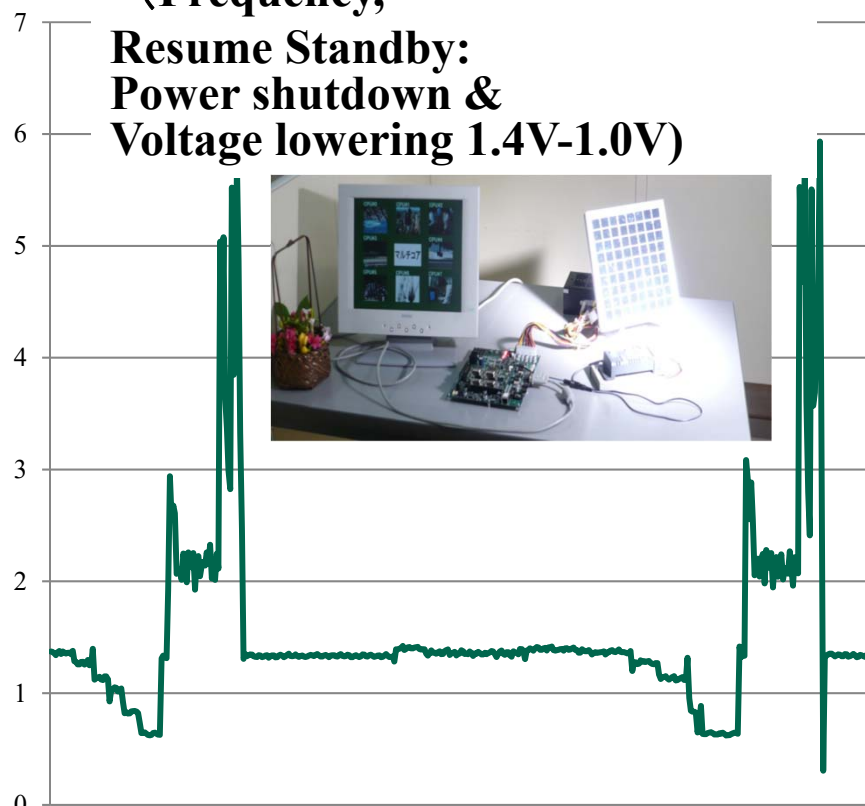
MPEG2 Decoding with 8 CPU cores
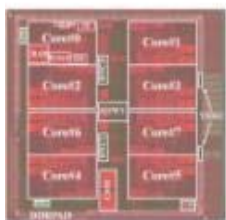
Without Power Control（Voltage：1.4V)

With Power Control（Frequency, Resume Standby: Power shutdown & Voltage lowering 1.4V-1.0V)

Avg. Power 5.73 [W]

73.5% Power Reduction

Avg. Power 1.52 [W]

Demo of NEDO Multicore for Real Time Consumer Electronics at the Council of Science and Engineering Policy on April 10, 2008

第74回総合科学技術会議 【平成20年4月10日】

第74回総合科学技術会議の様子(1)

第74回総合科学技術会議の様子(2)

第74回総合科学技術会議の様子(3)

第74回総合科学技術会議の様子(4)

CSTP Members

Prime Minister:
Mr. Y. FUKUDA

Minister of State for Science, Technology and Innovation Policy:
Mr. F. KISHIDA

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Minister of Education, Culture, Sports, Science and Technology:
Mr. K. TOKAI

Minister of Economy,Trade and Industry:
Mr. A. AMARI

Green Computing Systems R&D Center
Waseda University
Supported by METI (Mar. 2011 Completion)

〈R & D Target〉

Hardware, Software, Application for Super Low-Power Manycore

➢ **More than 64 cores**

➢ **Natural air cooling (No fan)** Cool, Compact, Clear, Quiet

➢ **Operational by Solar Panel**

〈Industry, Government, Academia〉

Hitachi, Fujitsu, NEC, Renesas, Olympus, Toyota, Denso, Mitsubishi, Toshiba, OSCAR Technology, etc

〈Ripple Effect〉

➢ **Low CO_2 (Carbon Dioxide) Emissions**

➢ **Creation Value Added Products**

➢ **Automobiles, Medical, IoT, Servers**
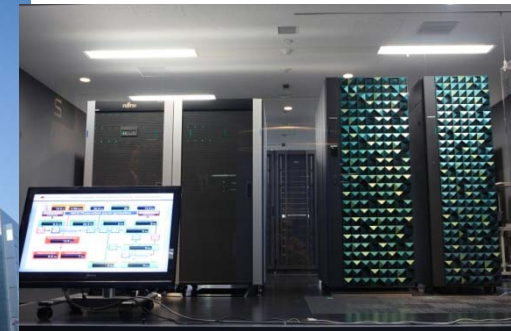
Hitachi SR16000: Power7 128coreSMP
Fujitsu M9000 SPARC VII 256 core SMP

Beside Subway Waseda Station, Near Waseda Univ. Main Campus

OSCAR Parallelizing Compiler

To improve effective performance, cost-performance and software productivity and reduce power

Multigrain Parallelization(LCPC1991,2001,04)

coarse-grain parallelism among loops and subroutines (2000 on SMP), near fine grain parallelism among statements (1992) in addition to loop parallelism

Data Localization

Automatic data management for distributed shared memory, cache and local memory (Local Memory 1995, 2016 on RP2,Cache2001,03) Software Coherent Control (2017)
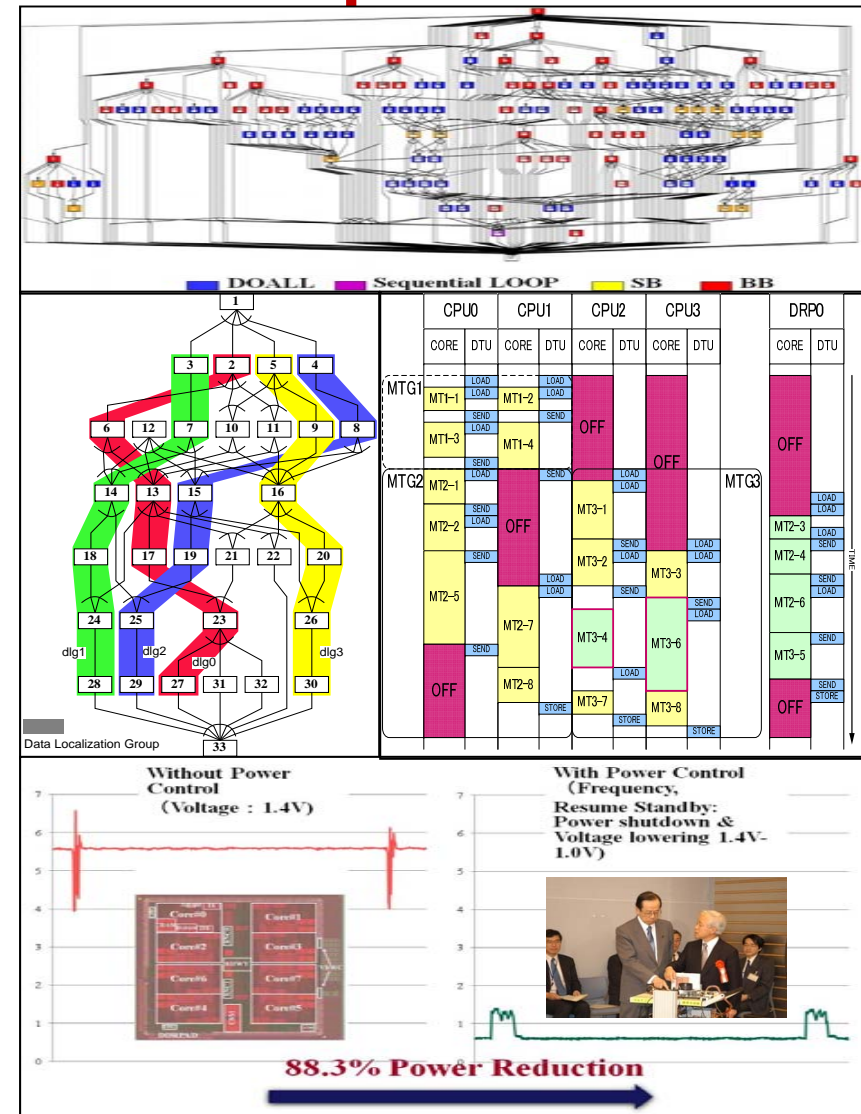
Data Transfer Overlapping(2016 partially)

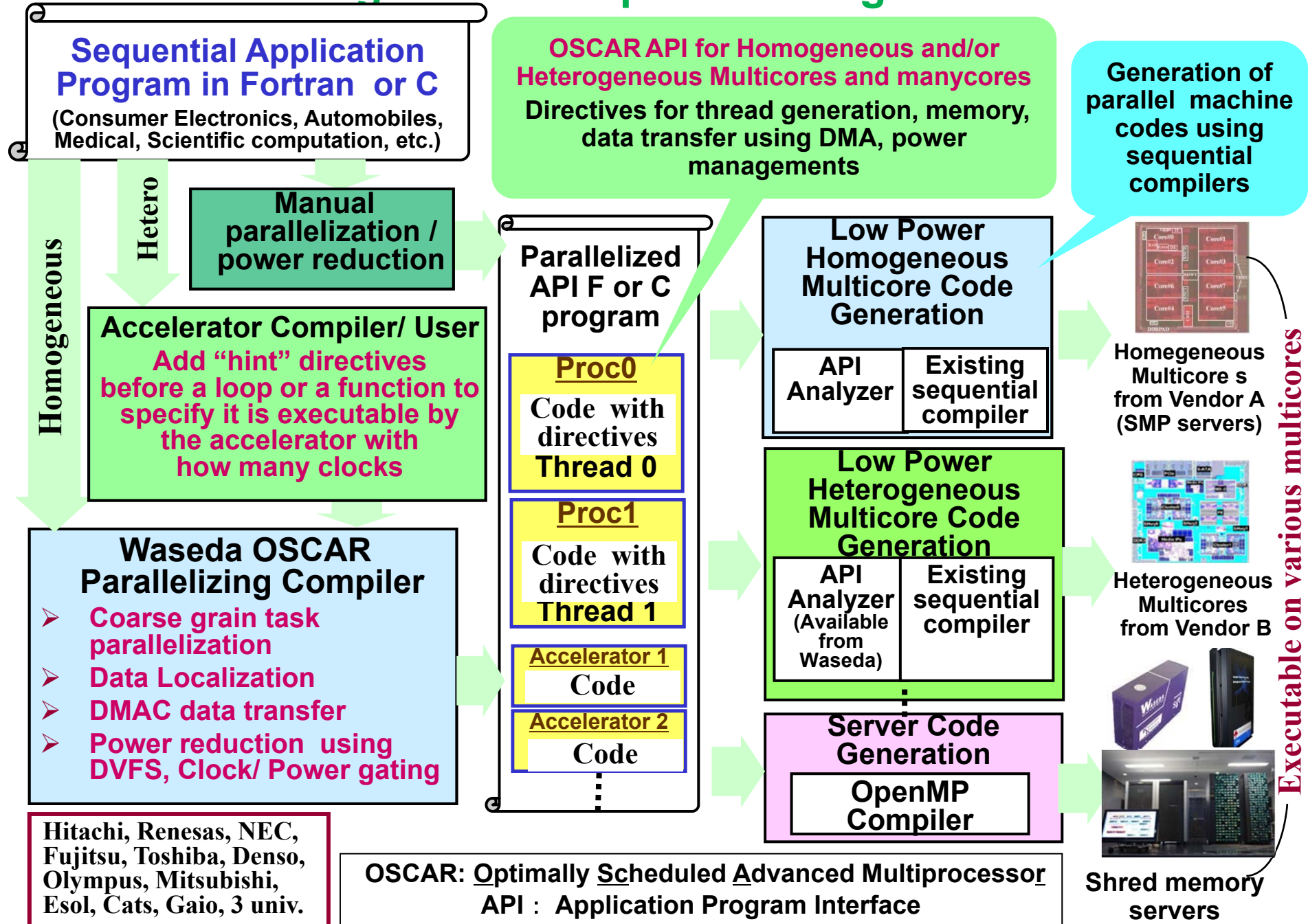Data transfer overlapping using Data Transfer Controllers (DMAs)

Power Reduction

(2005 for Multicore, 2011 Multi-processes, 2013 on ARM)

Reduction of consumed power by compiler control DVFS and Power gating with hardware supports.

DOALL Sequential LOOP SB BB

Data Localization Group

Without Power Control (Voltage : 1.4V)

With Power Control (Frequency, Resume Standby: Power shutdown & Voltage lowering 1.4V-1.0V)

88.3% Power Reduction

Multicore Program Development Using OSCAR API V2.0

Sequential Application Program in Fortran or C

(Consumer Electronics, Automobiles, Medical, Scientific computation, etc.)

OSCAR API for Homogeneous and/or Heterogeneous Multicores and manycores

Directives for thread generation, memory, data transfer using DMA, power managements

Generation of parallel machine codes using sequential compilers

Hetero

Homogeneous

Manual parallelization / power reduction

Accelerator Compiler/ User

Add "hint" directives before a loop or a function to specify it is executable by the accelerator with how many clocks

Waseda OSCAR Parallelizing Compiler

➢ **Coarse grain task parallelization**
➢ **Data Localization**
➢ **DMAC data transfer**
➢ **Power reduction using DVFS, Clock/ Power gating**

Hitachi, Renesas, NEC, Fujitsu, Toshiba, Denso, Olympus, Mitsubishi, Esol, Cats, Gaio, 3 univ.

Parallelized API F or C program

Proc0
Code with directives
Thread 0

Proc1
Code with directives
Thread 1

Accelerator 1
Code

Accelerator 2
Code

Low Power Homogeneous Multicore Code Generation

API Analyzer	Existing sequential compiler

Low Power Heterogeneous Multicore Code Generation

API Analyzer (Available from Waseda)	Existing sequential compiler

Server Code Generation

OpenMP Compiler

Homegeneous Multicore s from Vendor A (SMP servers)

Heterogeneous Multicores from Vendor B

Shred memory servers

Executable on various multicores

OSCAR: **O**ptimally **S**cheduled **A**dvanced Multiprocessor
API : Application Program Interface

Speedup ratio for H.264 and Optical Flow on ARM Cortex-A9 Android 3 cores by OSCAR Automatic Parallelization
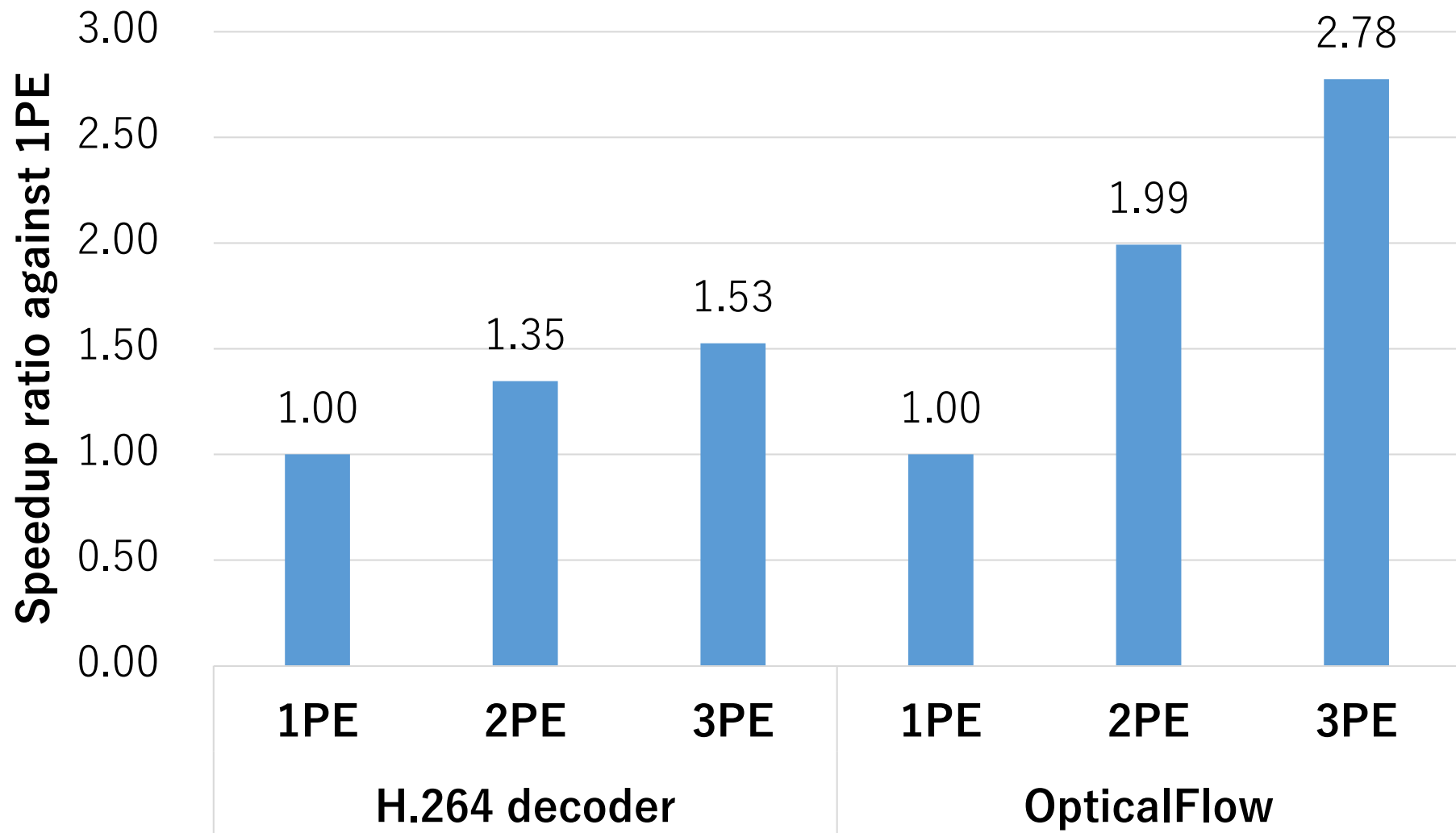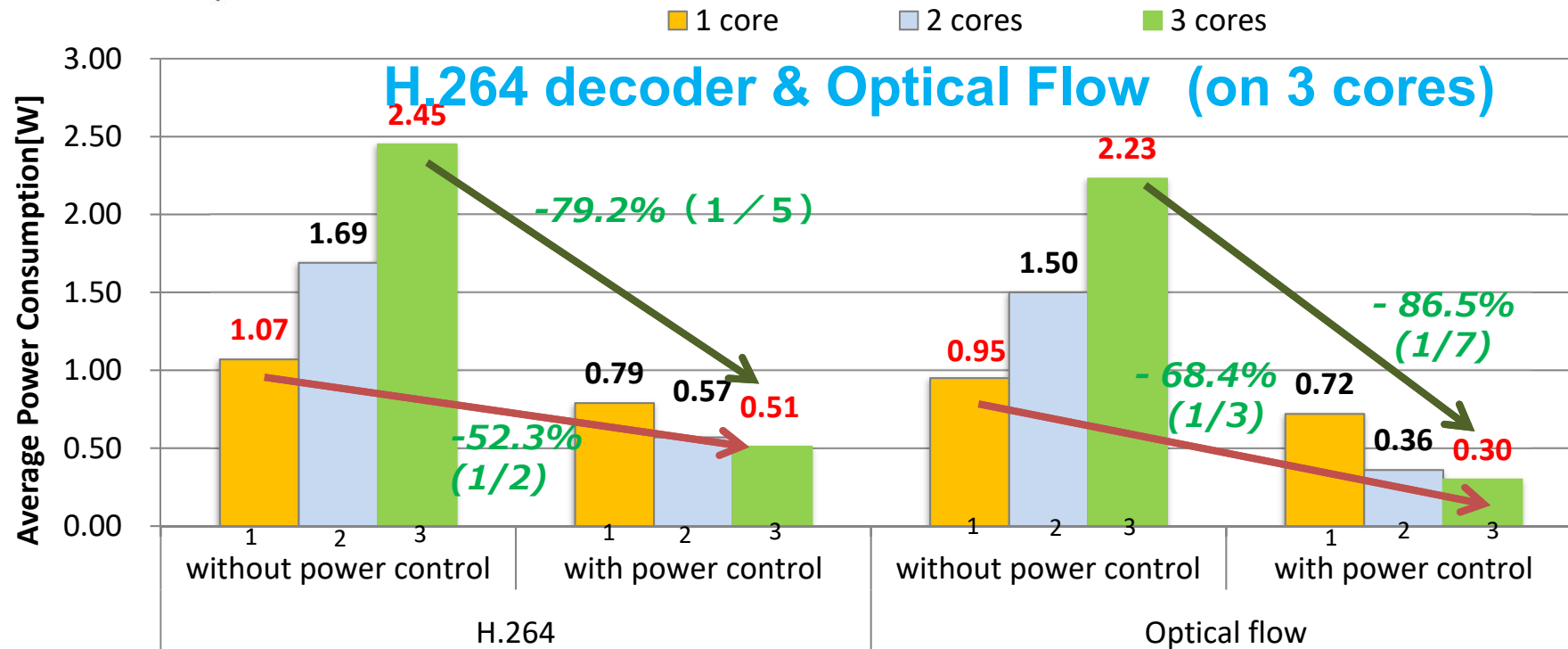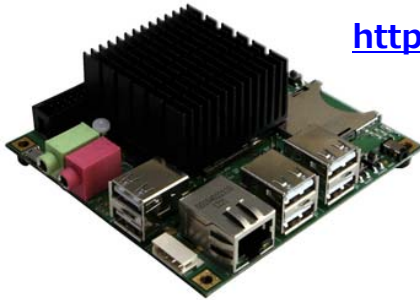
Automatic Power Reduction on ARM CortexA9 with Android

http://www.youtube.com/channel/UCS43lNYEIkC8i_KIgFZYQBQ

ODROID X2

Samsung Exynos4412 Prime, ARM Cortex-A9 Quad core
1.7GHz～0.2GHz, used by Samsung's Galaxy S3

Legend: ■ 1 core ■ 2 cores ■ 3 cores

H.264 decoder & Optical Flow (on 3 cores)

Chart — Average Power Consumption[W]

H.264:
- without power control: 1 core = 1.07, 2 cores = 1.69, 3 cores = 2.45
- with power control: 1 core = 0.79, 2 cores = 0.57, 3 cores = 0.51
- −79.2% (1／5)
- −52.3% (1/2)

Optical flow:
- without power control: 1 core = 0.95, 2 cores = 1.50, 3 cores = 2.23
- with power control: 1 core = 0.72, 2 cores = 0.36, 3 cores = 0.30
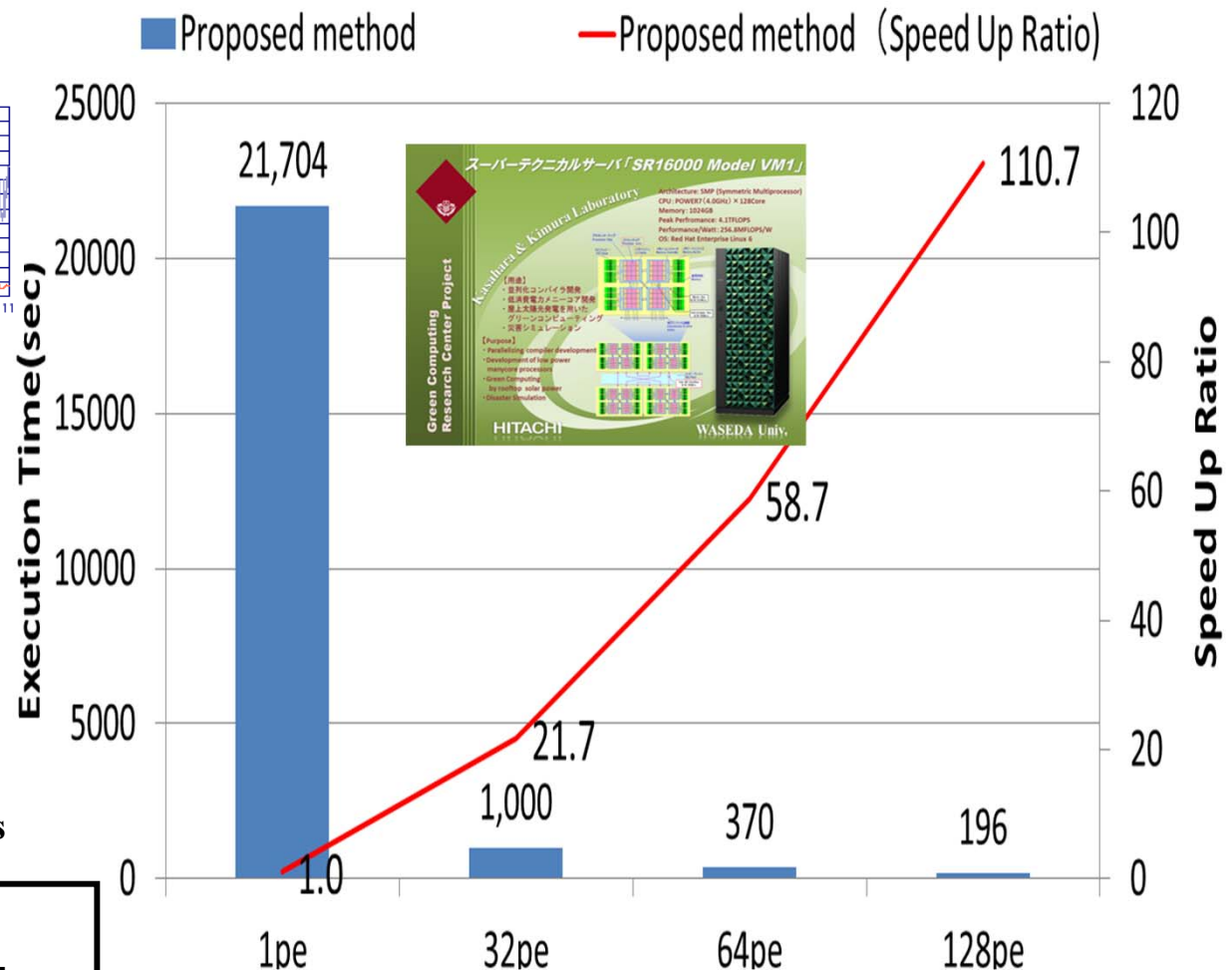- − 86.5% (1/7)
- − 68.4% (1/3)

Power for 3cores was reduced to 1/5～1/7 against without software power control
Power for 3cores was reduced to 1/2～1/3 against ordinary 1core execution

15

Automatic Power Reduction of OpenCV Face Detection on big.LITTLE ARM Processor

Power Consumption [W]

4.9w

-67% (1/3)

1.6w

3PE — W/O Power Control

3PE — W/ Power Control

- ## ODROID-XU3
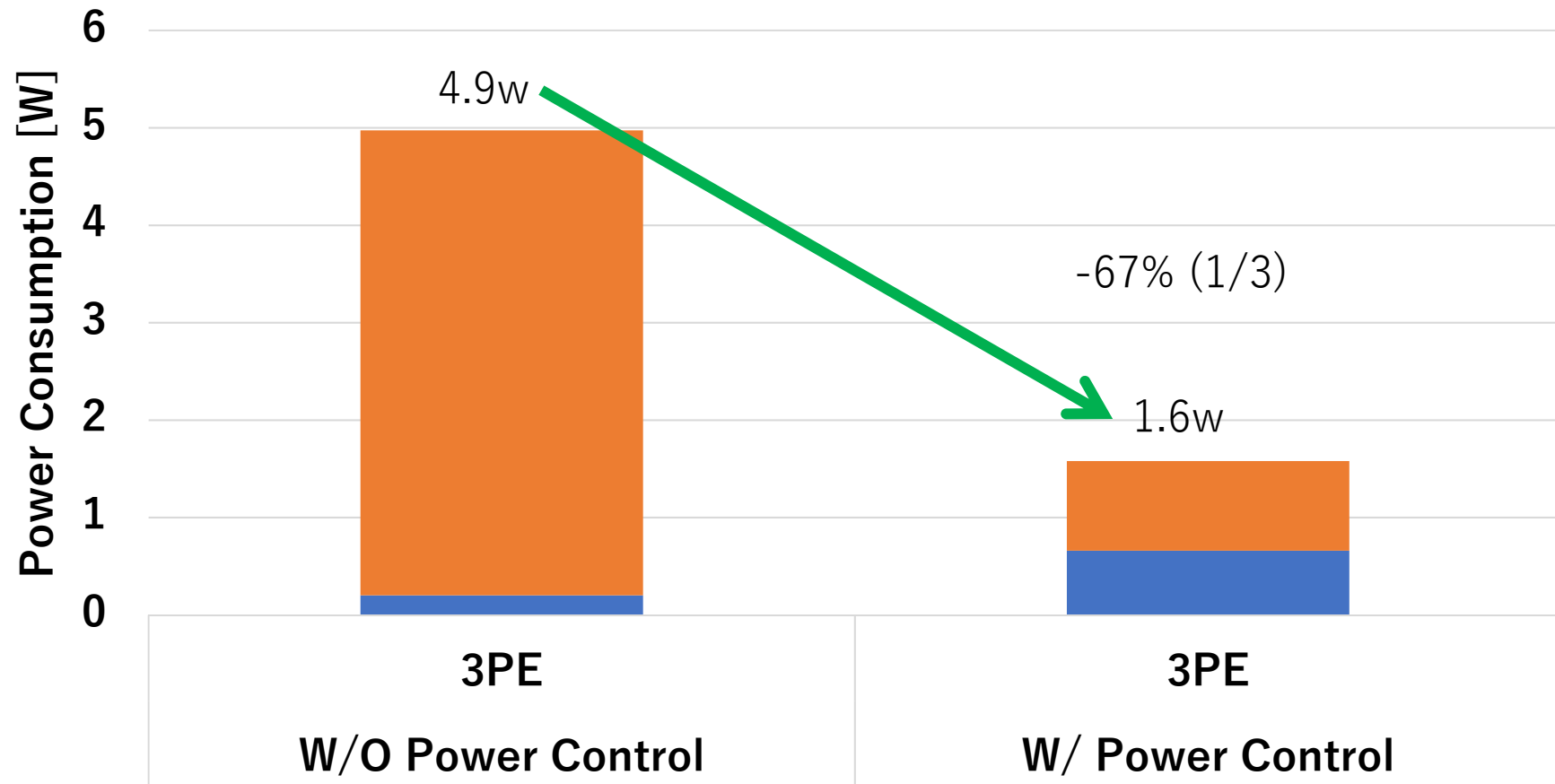
Cortex-A7   Cortex-A15

  - ## Samsung Exynos 5422 Processor

    - 4x Cortex-A15 2.0GHz, 4x Cortex-A7 1.4GHz big.LITTLE Architecture

    - 2GB LPDDR3 RAM   Frequency can be changed by

Automatic Power Reuction on Intel Haswell
H.264 decoder & Optical Flow (3cores)

H81M-A, Intel Core i7 4770k

Quad core, 3.5GHz～0.8GHz
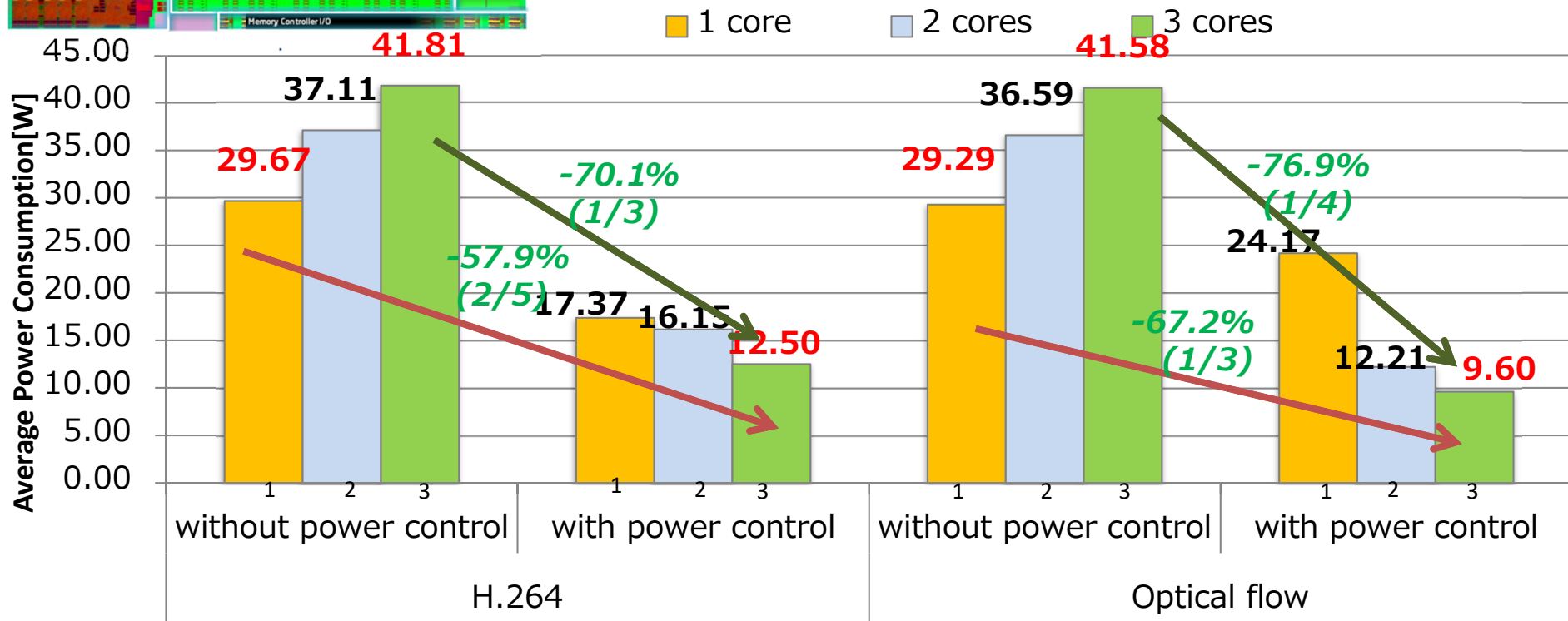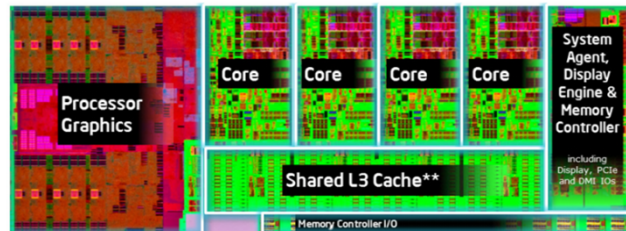
Power for 3cores was reduced to 1/3～1/4 against without software power control

Power for 3cores was reduced to 2/5～1/3 against ordinary 1core execution

110 Times Speedup against the Sequential Processing for GMS Earthquake Wave Propagation Simulation on Hitachi SR16000
（Power7 Based 128 Core Linux SMP） (LCPC2015)

Fortran:15 thousand lines
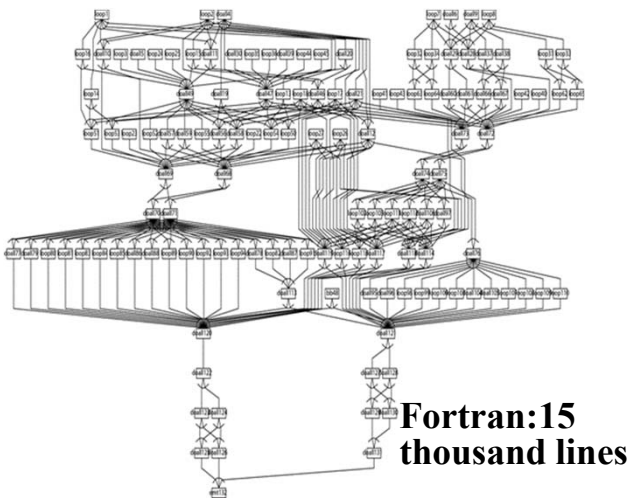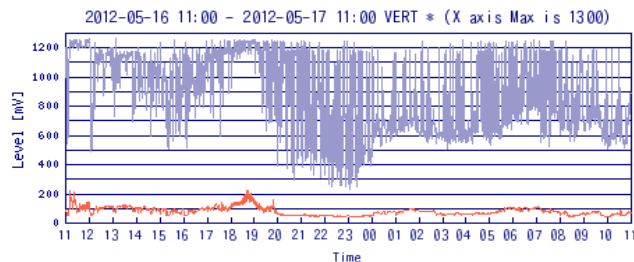
First touch for distributed shared memory and cache optimization over loops are important for scalable speedup

Proposed method — **Proposed method（Speed Up Ratio)**

21,704

1,000

370

196

110.7

58.7

21.7

1.0

Execution Time(sec)

Speed Up Ratio

25000

20000

15000

10000

5000

0

120

100

80

60

40

20

0

1pe   32pe   64pe   128pe

2012-05-16 11:00 - 2012-05-17 11:00 VERT ※ (X axis Max is 1300)

Performance on Multicore Server for Latest Cancer Treatment Using Heavy Particle (Proton, Carbon Ion)

327 times speedup on 144 cores

Hitachi 144cores SMP Blade Server BS500:
Xeon E7-8890 V3(2.5GHz　18core/chip) x8 chip

327.6 times speed up with 144 cores

- GCC

1PE	32pe	64pe	144pe
1.00 5.00	109.20	196.50	327.60
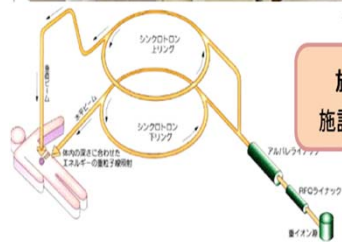
放射線医学研究所
施設の費用：120億円
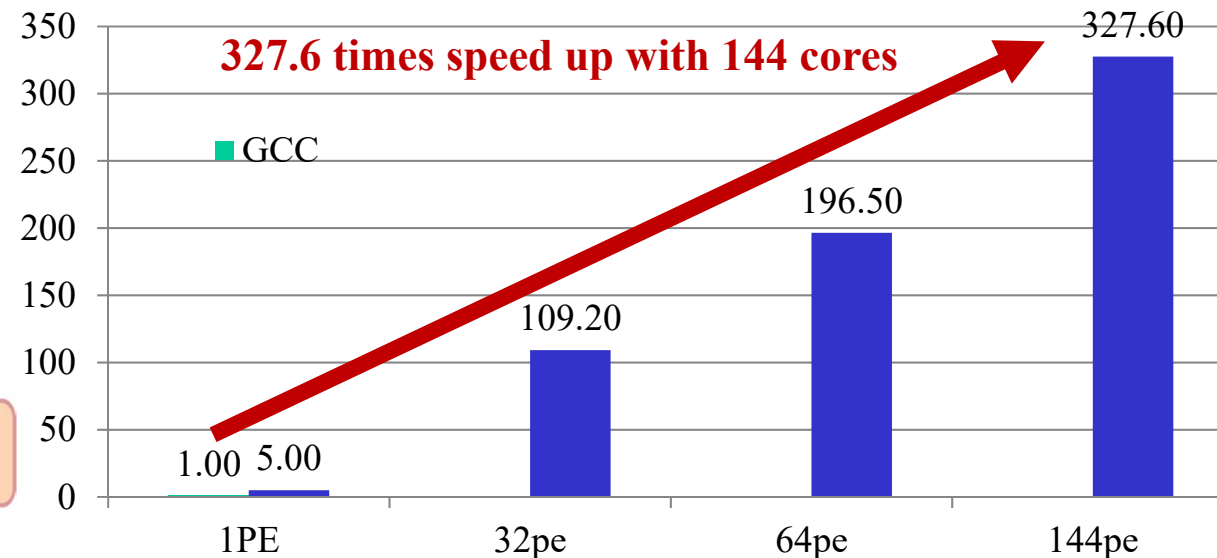
➤ **Original sequential execution time 2948 sec（50 minutes）using GCC was reduced to 9 sec with 144 cores（327.6 times speedup）**
  ➤ **Reduction of treatment cost and reservation waiting period is expected**

19

Cancer Treatment
Carbon Ion Radiotherapy

(Previous best was 2.5 times speedup on 16 processors with hand optimization)
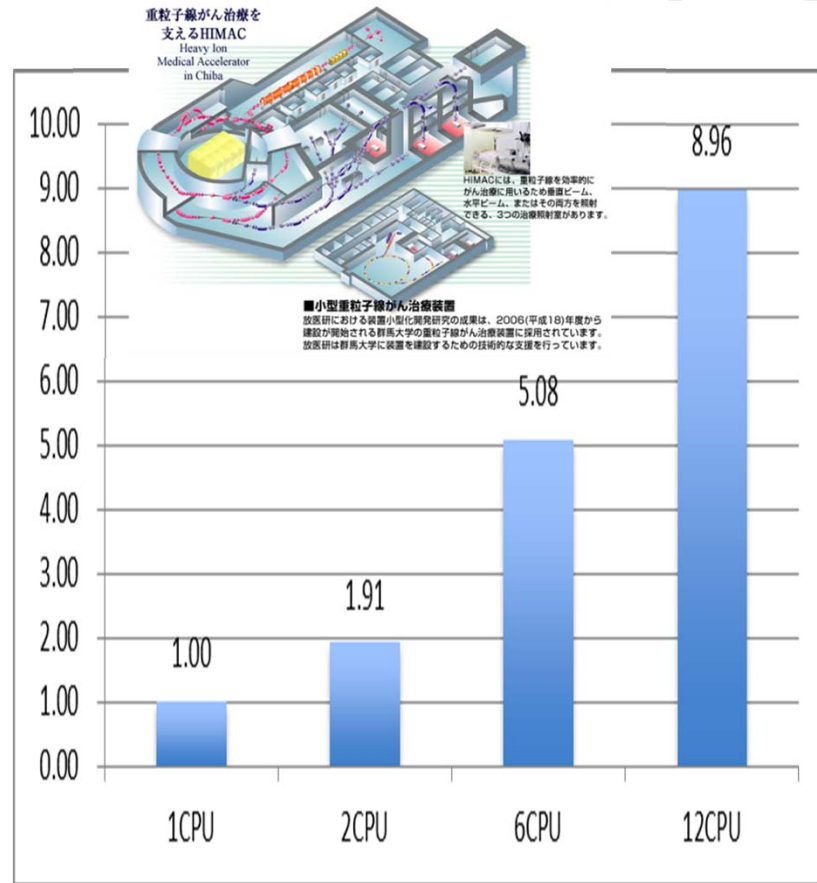
8.9times speedup by 12 processors

Intel Xeon X5670 2.93GHz 12 core SMP (Hitachi HA8000)
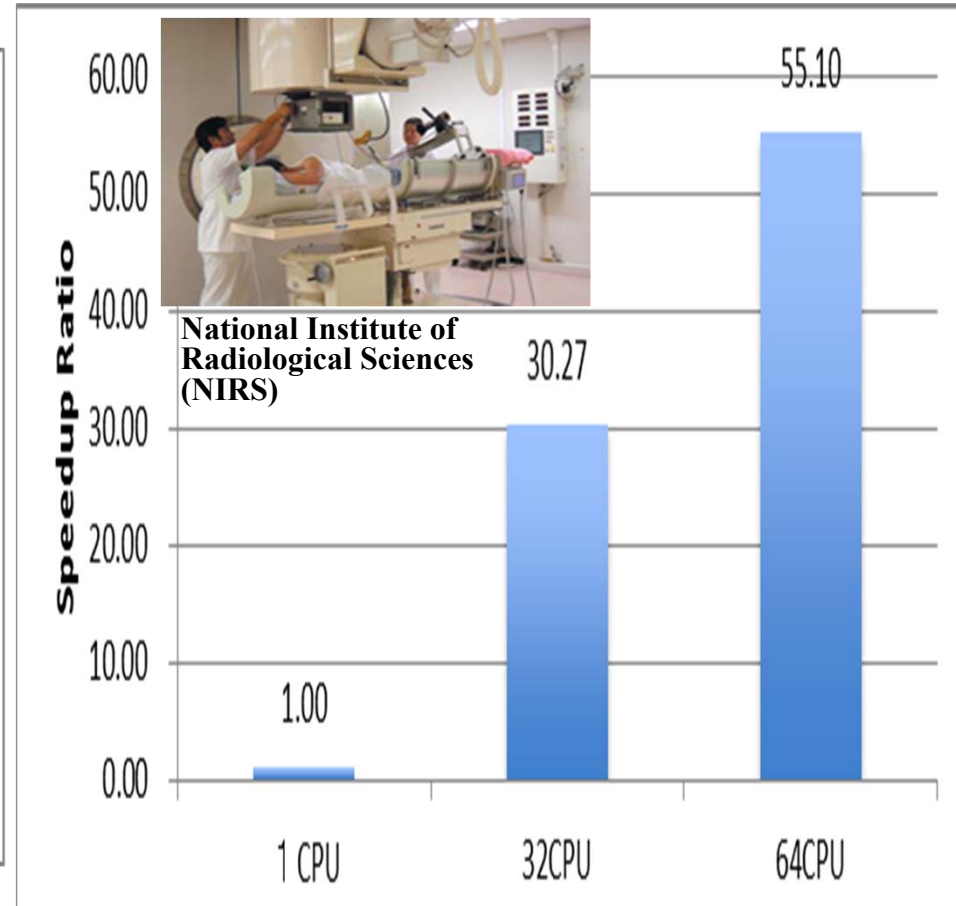
55 times speedup by 64 processors

IBM Power 7   64 core SMP (Hitachi SR16000)
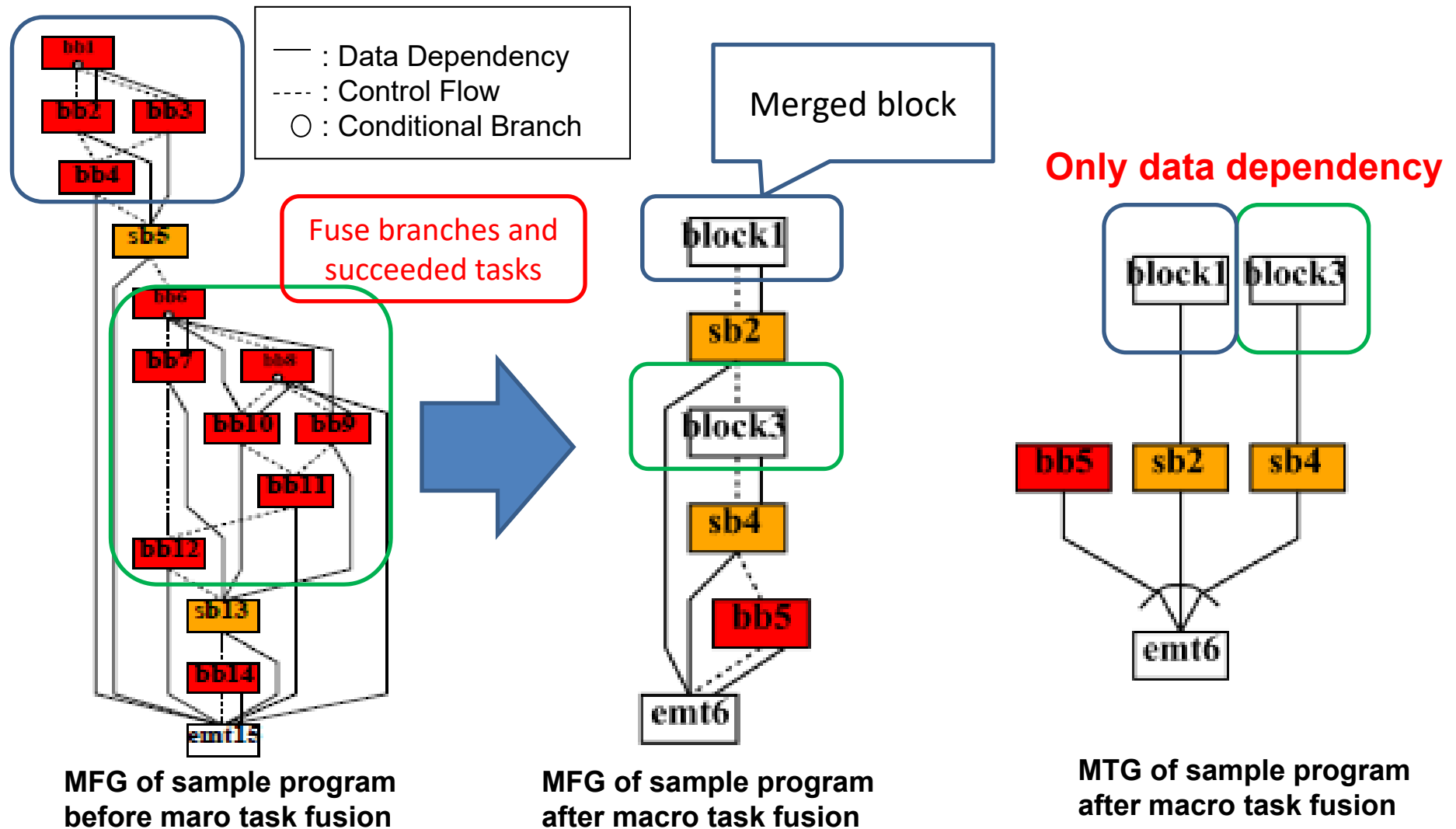
Engine Control by multicore with Denso

Though so far parallel processing of the engine control on multicore has been very difficult, Denso and Waseda succeeded 1.95 times speedup on 2core V850 multicore processor.

➢ **Hard real-time automobile engine control by multicore using local memories**

➢ **Millions of lines C codes consisting conditional branches and basic blocks**

1 core
逐次

2 cores
並列化
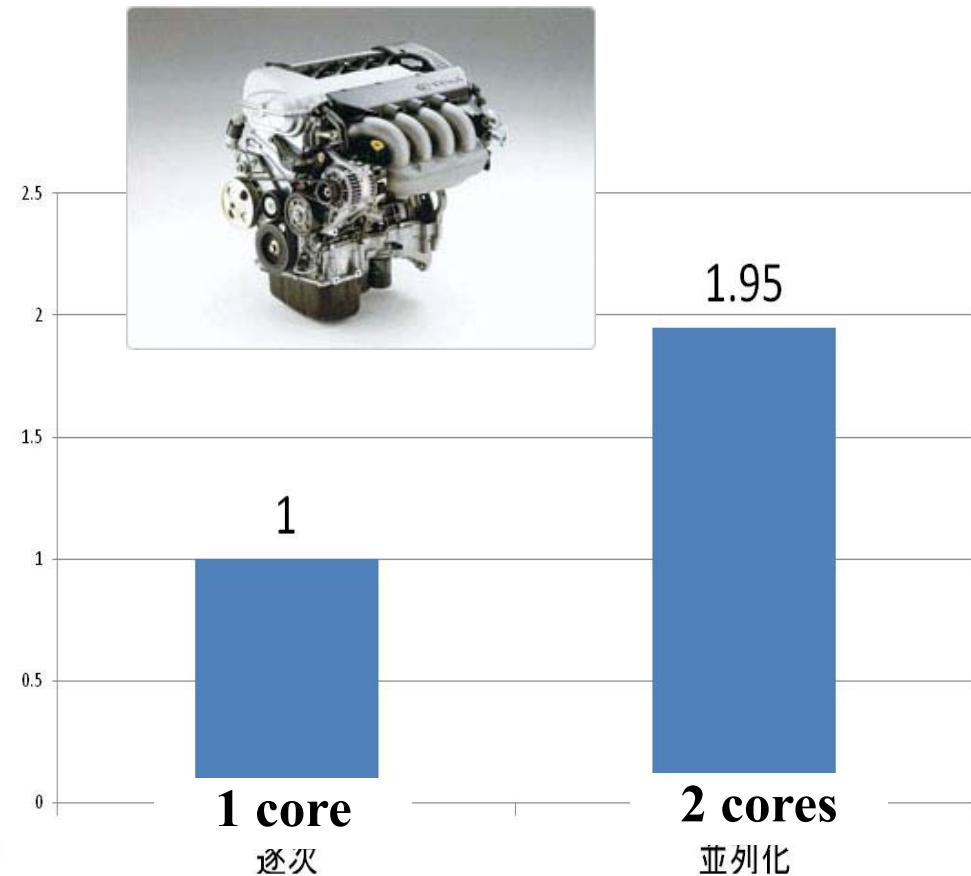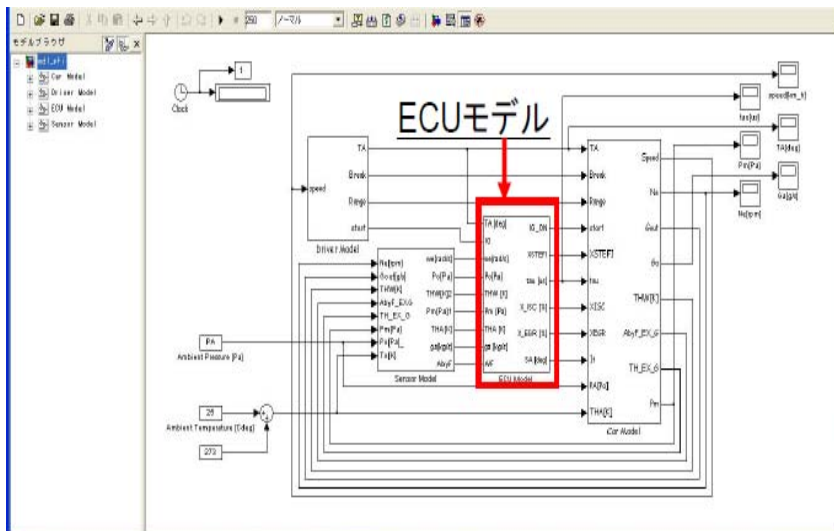
Macro Task Fusion for Static Task Scheduling

: Data Dependency
---- : Control Flow
○ : Conditional Branch

Fuse branches and succeeded tasks

Merged block

Only data dependency

MFG of sample program before maro task fusion

MFG of sample program after macro task fusion

MTG of sample program after macro task fusion

3.1 Restructuring : Inline Expansion

□ Inline expansion is effective

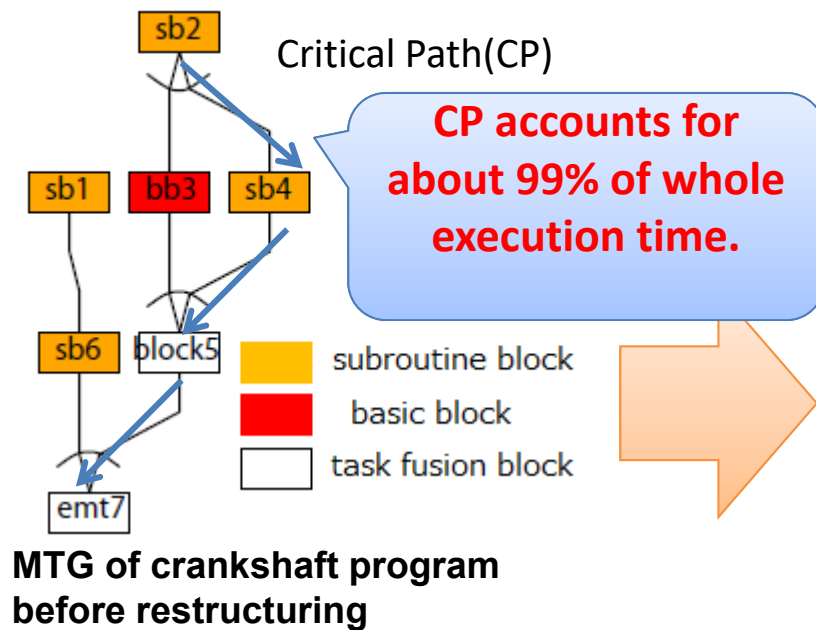   □ To increase coarse grain parallelism

□ Expands functions having inner parallelism

Improves coarse grain parallelism
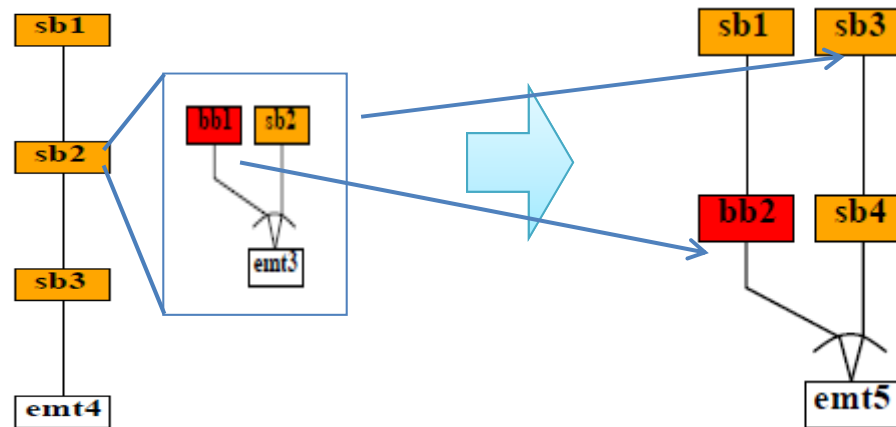
MTG before inline expansion

MTG after inline expansion

MTG of Crankshaft Program Using Inline Expansion

Critical Path(CP)

CP accounts for about 99% of whole execution time.

subroutine block

basic block

task fusion block

MTG of crankshaft program before restructuring

subroutine block

basic block

task fusion block

Critical Path(CP)

CP accounts for about 90% of whole execution time.

70%
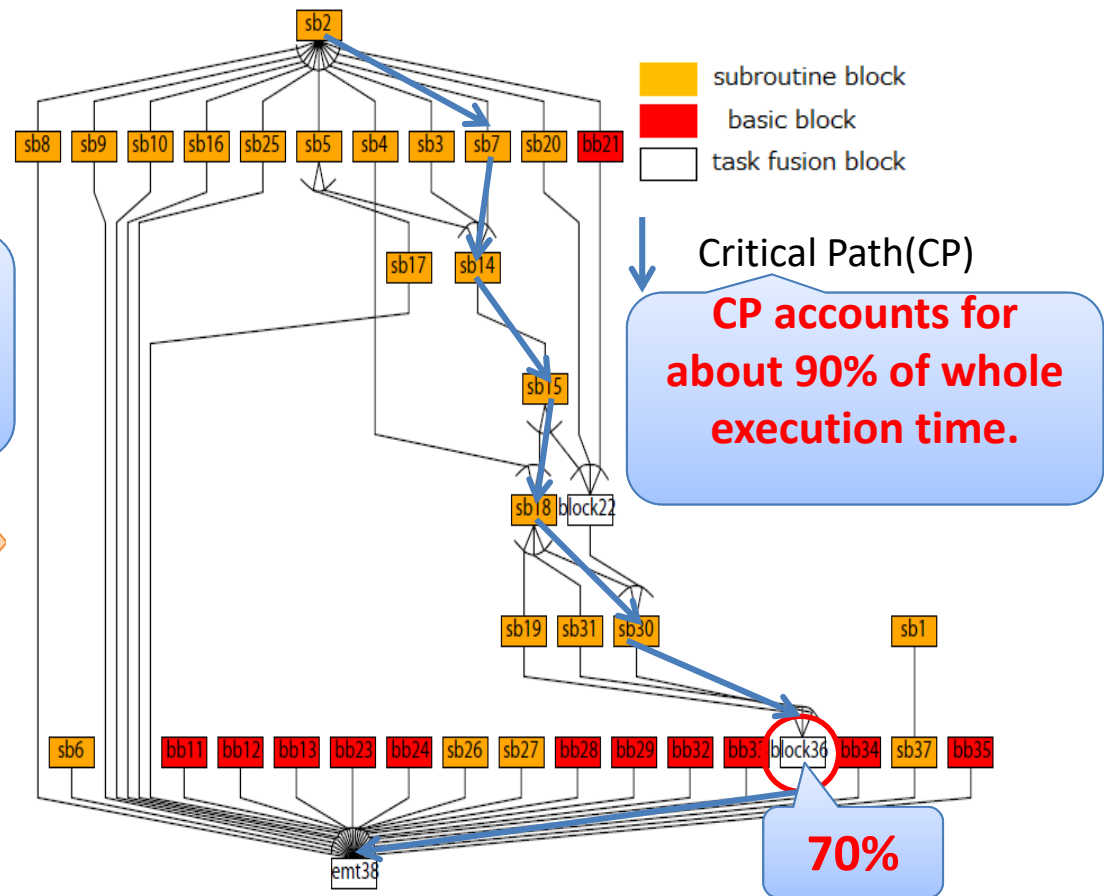
Not enough coarse grain parallelism yet!

3.2 Restructuring: Duplicating If-statements

- ☐ Duplicating if-statements is effective
  - ☐ To increase coarse grain parallelism
- ☐ Duplicates fused tasks having inner parallelism

Improves coarse grain parallelism

Func1 depends on func3
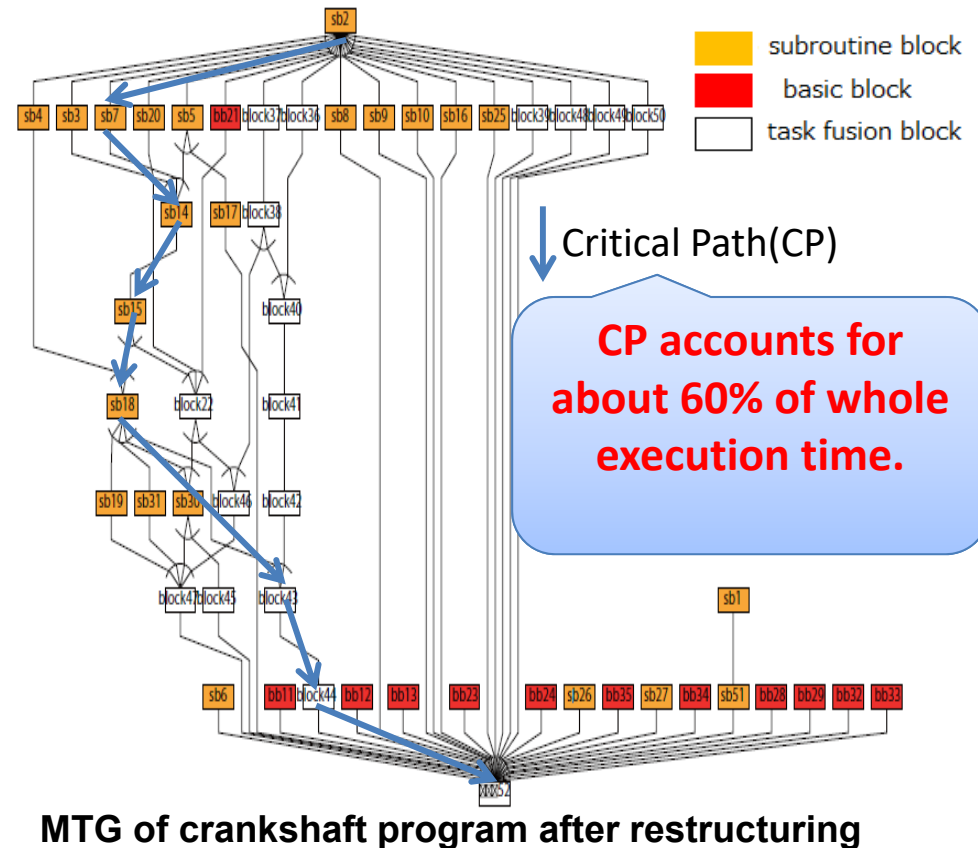
func1();

```
if (condition) {
    func2();
    func3();          No
    func4();          dependemce
}
```
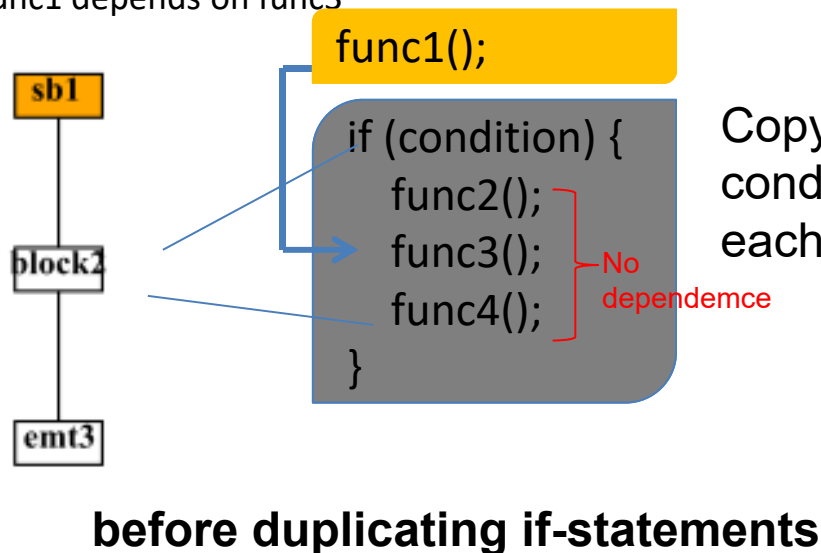
Copying if-condition for each function

func1();

```
if (condition) {
    func2();
}
```

```
if (condition) {
    func3();
}
```

```
if (condition) {
    func4();
}
```

before duplicating if-statements

after duplicating if-statements

sb1

block2

emt3

sb1

block2 block4 block3

emt5
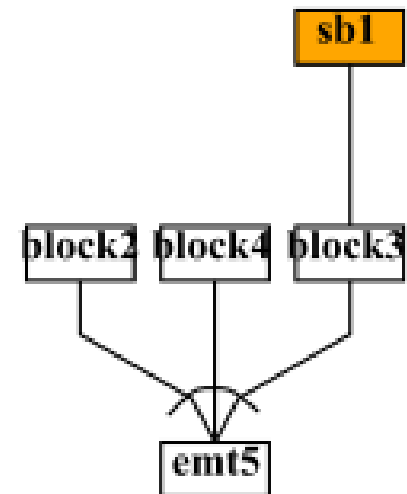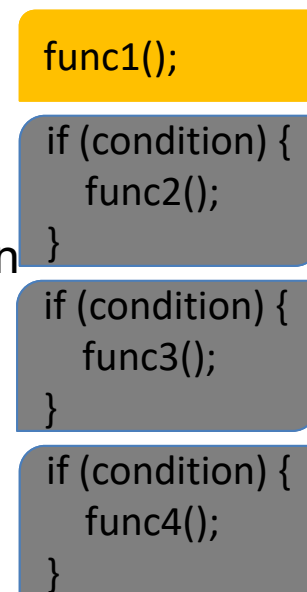
MTG of Crankshaft Program Using Inline Expansion and Duplicating If-statements

CP accounts for over 99% of whole execution time.

Critical Path(CP)

CP accounts for about 60% of whole execution time.

subroutine block
basic block
task fusion block

MTG of crankshaft program before restructuring

MTG of crankshaft program after restructuring
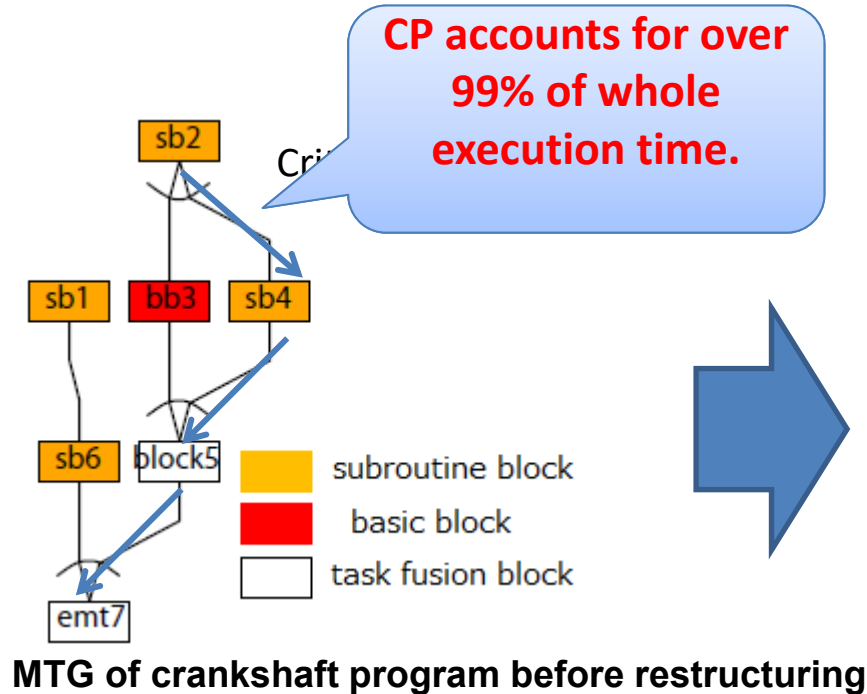
□ Succeed to reduce CP
  □ 99% -> 60%

Successfully increased coarse grain parallelism

Evaluation of Crankshaft Program with Multi-core Processors

speedup ratio

execution time(us)

0.57

1.54

1.00

0.37

1 core

2 core
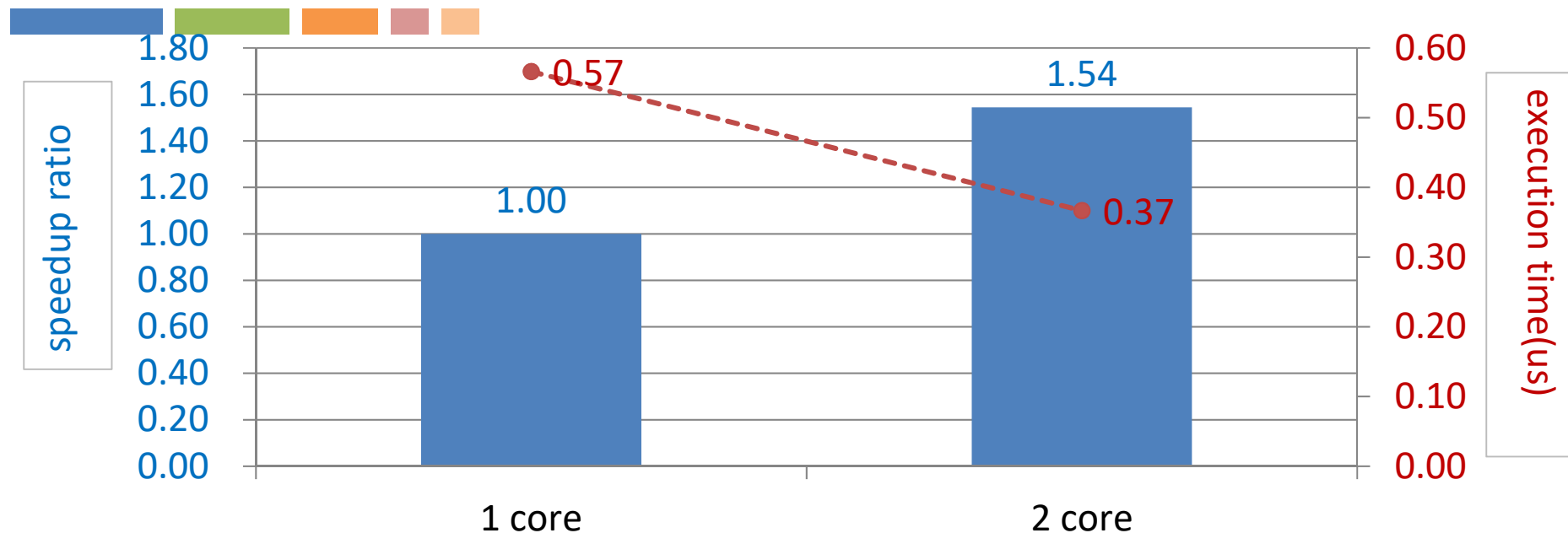
- ☐ Attain 1.54 times speedup on RPX
  - ■ There are no loops, but only many conditional branches and small basic blocks and difficult to parallelize this program
- ☐ This result shows possibility of multi-core processor for engine control programs

OSCAR Compile Flow for Simulink Applications
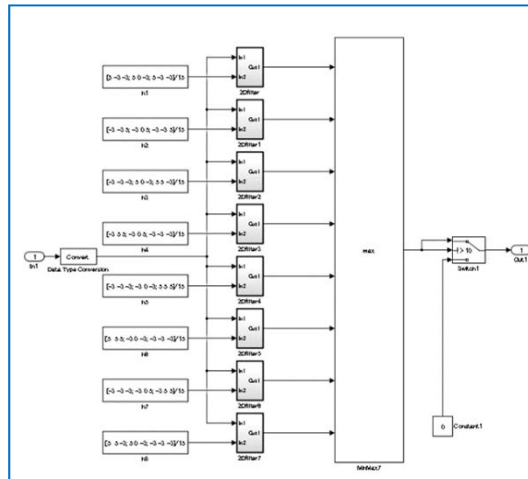
Simulink model

**Generate C code
using Embedded Coder**
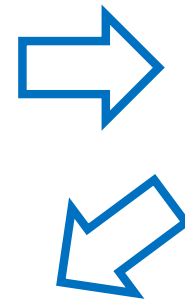
```
/* Model step function */
void VesselExtraction_step(void)
{
  int32_T i;
  real_T u0;

  /* DataTypeConversion: '<S1>/Data Type Conversion' incorporates:
   *  Inport: '<Root>/In1'
   */
  for (i = 0; i < 16384; i++) {
    VesselExtraction_B.DataTypeConversion[i] = VesselExtraction_U.In1[i];
  }

  /* End of DataTypeConversion: '<S1>/Data Type Conversion' */

  /* Outputs for Atomic SubSystem: '<S1>/2Dfilter' */

  /* Constant: '<S1>/h1' */
  VesselExtraction_Dfilter(VesselExtraction_B.DataTypeConversion,
    VesselExtraction_P.h1_Value, &VesselExtraction_B.Dfilter,
    (P_Dfilter_VesselExtraction_T *)&VesselExtraction_P.Dfilter);

  /* End of Outputs for SubSystem: '<S1>/2Dfilter' */

  /* Outputs for Atomic SubSystem: '<S1>/2Dfilter1' */

  /* Constant: '<S1>/h2' */
  VesselExtraction_Dfilter(VesselExtraction_B.DataTypeConversion,
    VesselExtraction_P.h2_Value, &VesselExtraction_B.Dfilter1,
    (P_Dfilter_VesselExtraction_T *)&VesselExtraction_P.Dfilter1);
```
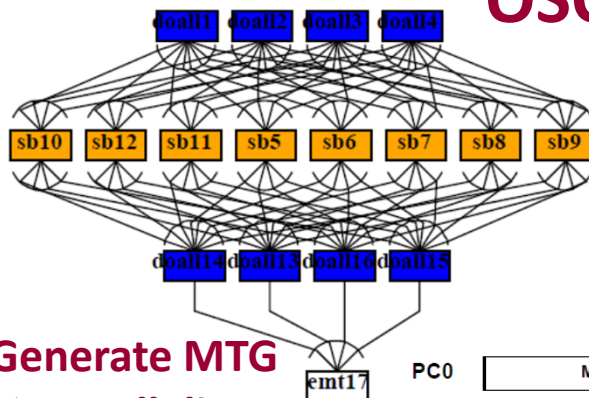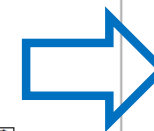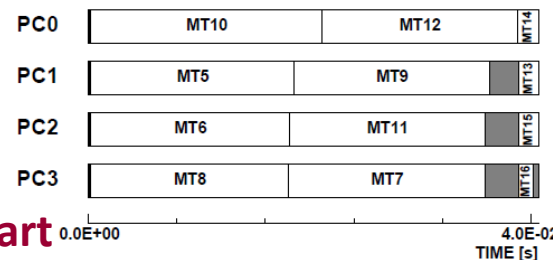
C code

OSCAR Compiler


```
void VesselExtraction_step ( )
{
  int thr1 ;
  int thr2 ;
  int thr3 ;
  {
    oscar_thread_create ( & thr1 ,
      thread_function_001 , (void*)1 ) ;
    oscar_thread_create ( & thr2 ,
      thread_function_002 , (void*)2 ) ;
    oscar_thread_create ( & thr3 ,
      thread_function_003 , (void*)3 ) ;

    VesselExtraction_step_PE0 ( ) ;

    oscar_thread_join ( thr1 ) ;
    oscar_thread_join ( thr2 ) ;
    oscar_thread_join ( thr3 ) ;
  }
}
```
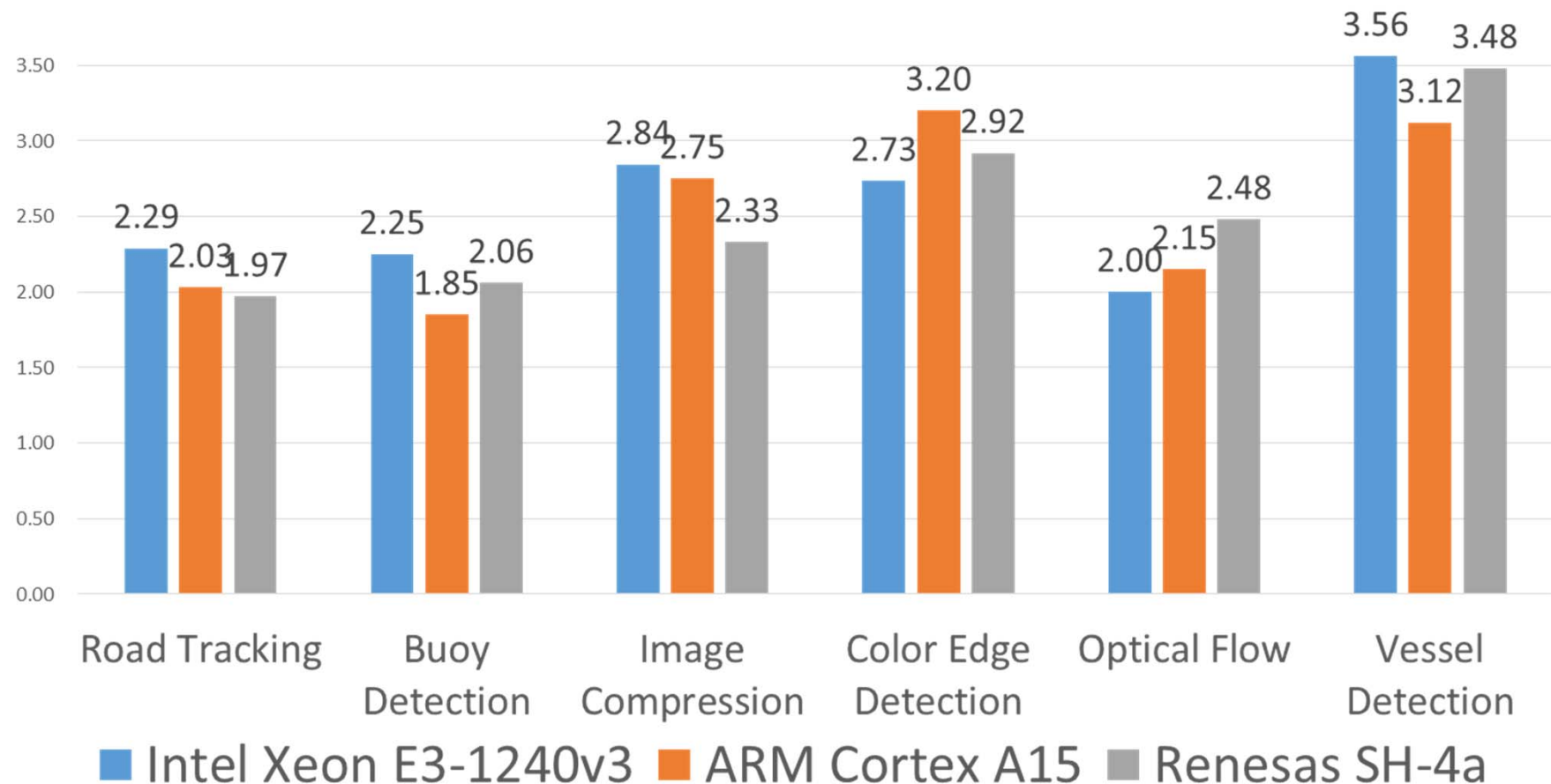
```
void thread_function_001 ( void )
{
  VesselExtraction_step_PE1 ( ) ;
}
```

**(1) Generate MTG
→ Parallelism**

**(2) Generate gantt chart
→ Scheduling in a multicore**

**(3) Generate parallelized C code
using the OSCAR API
→ Multiplatform execution
(Intel, ARM and SH etc)**

Speedups of MATLAB/Simulink Image Processing on Various 4core Multicores
(Intel Xeon, ARM Cortex A15 and Renesas SH4A)

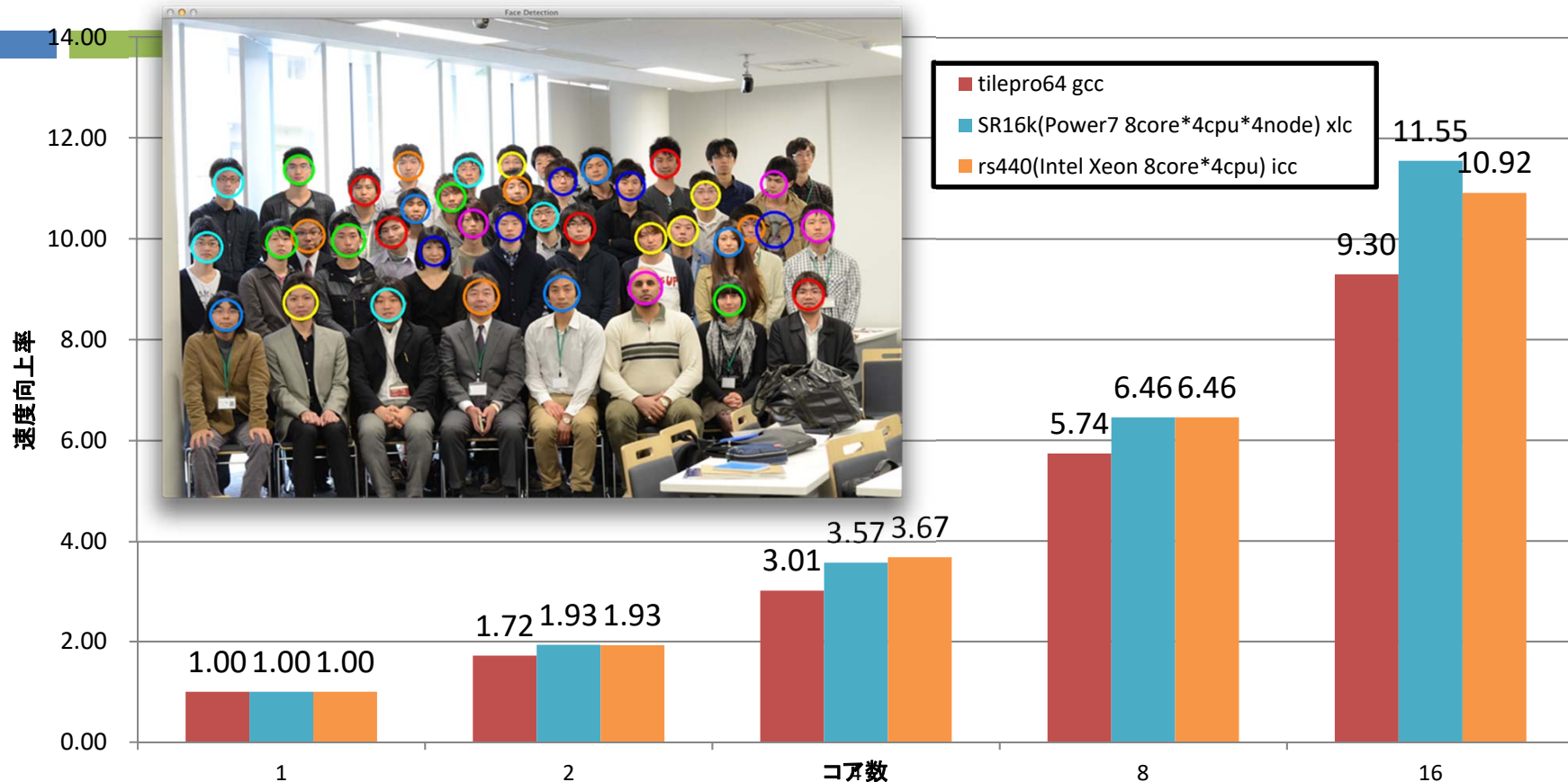|	Road Tracking	Buoy Detection	Image Compression	Color Edge Detection	Optical Flow	Vessel Detection
Intel Xeon E3-1240v3	2.29	2.25	2.84	2.73	2.00	3.56
ARM Cortex A15	2.03	1.85	2.75	3.20	2.15	3.12
Renesas SH-4a	1.97	2.06	2.33	2.92	2.48	3.48

Road Tracking, Image Compression : http://www.mathworks.co.jp/jp/help/vision/examples
Buoy Detection : http://www.mathworks.co.jp/matlabcentral/fileexchange/44706-buoy-detection-using-simulink
Color Edge Detection : http://www.mathworks.co.jp/matlabcentral/fileexchange/28114-fast-edges-of-a-color-image--actual-color--not-converting-to-grayscale-/
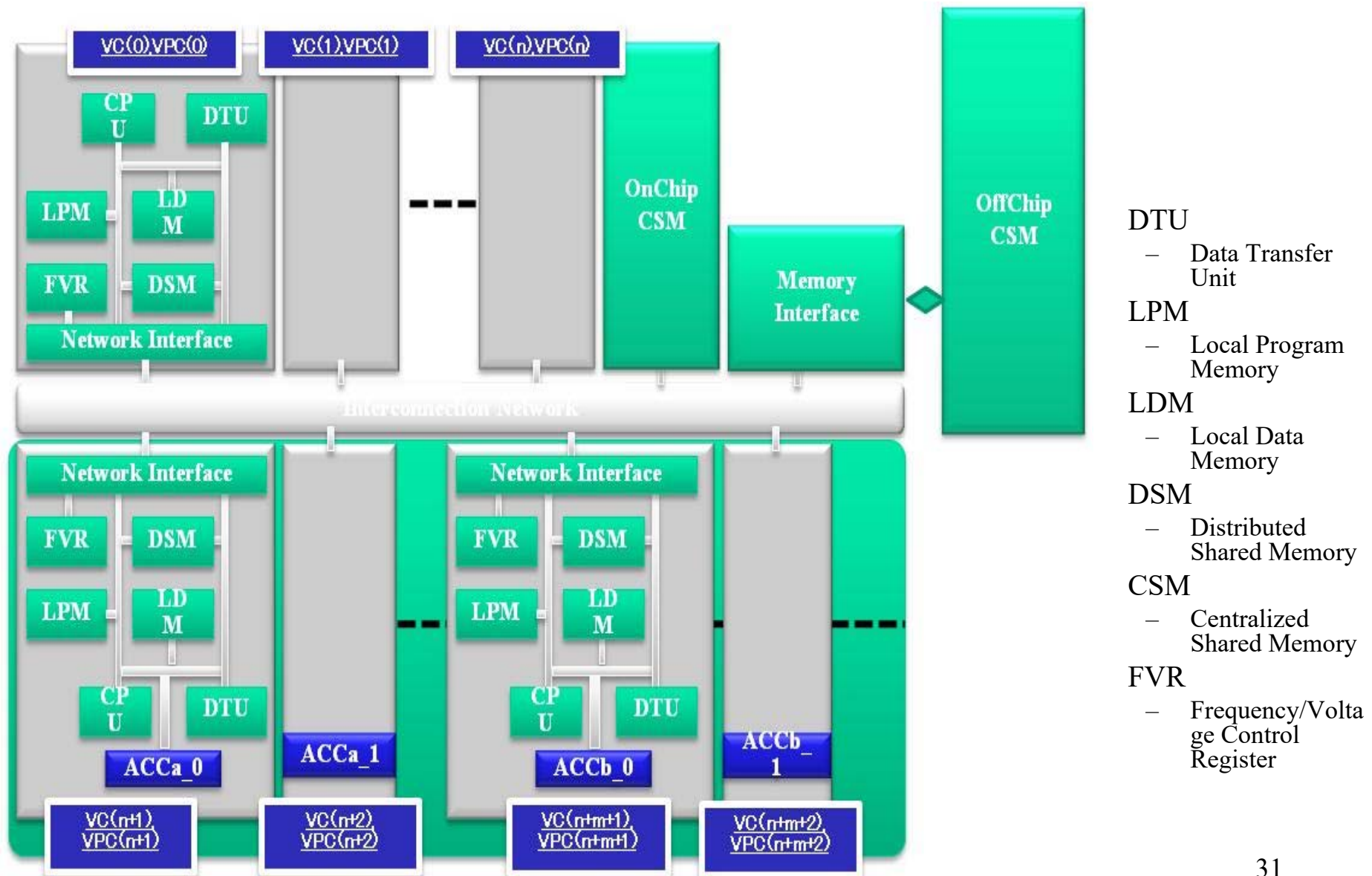Vessel Detection : http://www.mathworks.co.jp/matlabcentral/fileexchange/24990-retinal-blood-vessel-extraction/

# Parallel Processing of Face Detection on Manycore, Highend and PC Server

- ☐ OSCAR compiler gives us 11.55 times speedup for 16 cores against 1 core on SR16000 Power7 highend server.

OSCAR Heterogeneous Multicore

DTU
– Data Transfer Unit

LPM
– Local Program Memory

LDM
– Local Data Memory

DSM
– Distributed Shared Memory

CSM
– Centralized Shared Memory

FVR
– Frequency/Voltage Control Register

31

An Image of Static Schedule for Heterogeneous Multi-core with Data Transfer Overlapping and Power Control
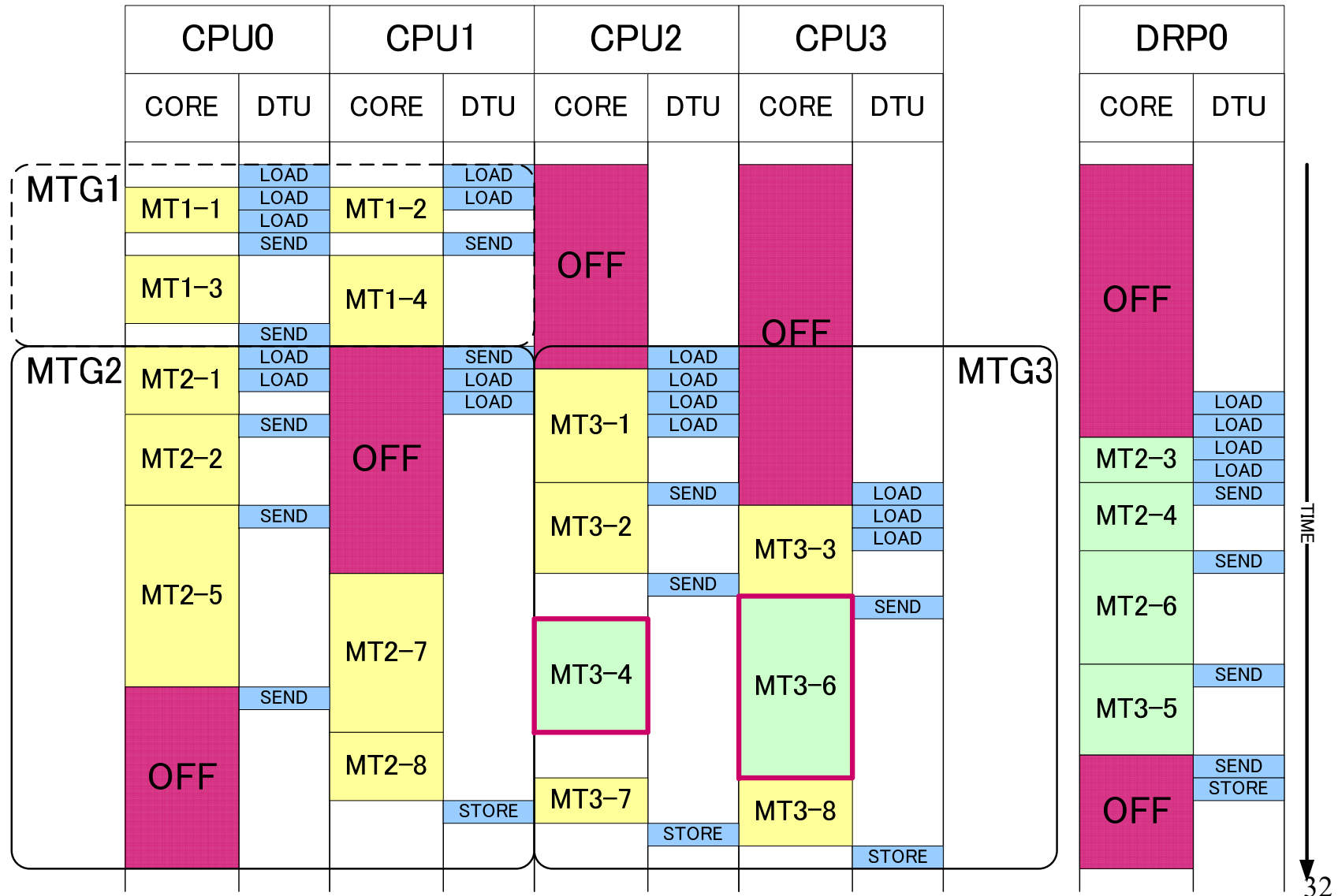
OSCAR API Ver. 2.0 for Homogeneous/Heterogeneous Multicores and Manycores (LCPC2009Homo, 2010 Hetero)

List of Directives (22 directives)

- **Parallel Execution API**
  - parallel sections (*)
  - flush (*)
  - critical (*)
  - execution
- **Memoay Mapping API**
  - threadprivate (*)
  - distributedshared
  - onchipshared
- **Synchronization API**
  - groupbarrier
- **Data Transfer API**
  - dma_transfer
  - dma_contiguous_parameter
  - dma_stride_parameter
  - dma_flag_check
  - dma_flag_send

(* from OpenMP)

- **Power Control API**
  - fvcontrol
  - get_fvstatus
- **Timer API**
  - get_current_time
- **Accelerator**
  - accelerator_task_entry
- **Cache Control**
  - cache_writeback
  - cache_selfinvalidate
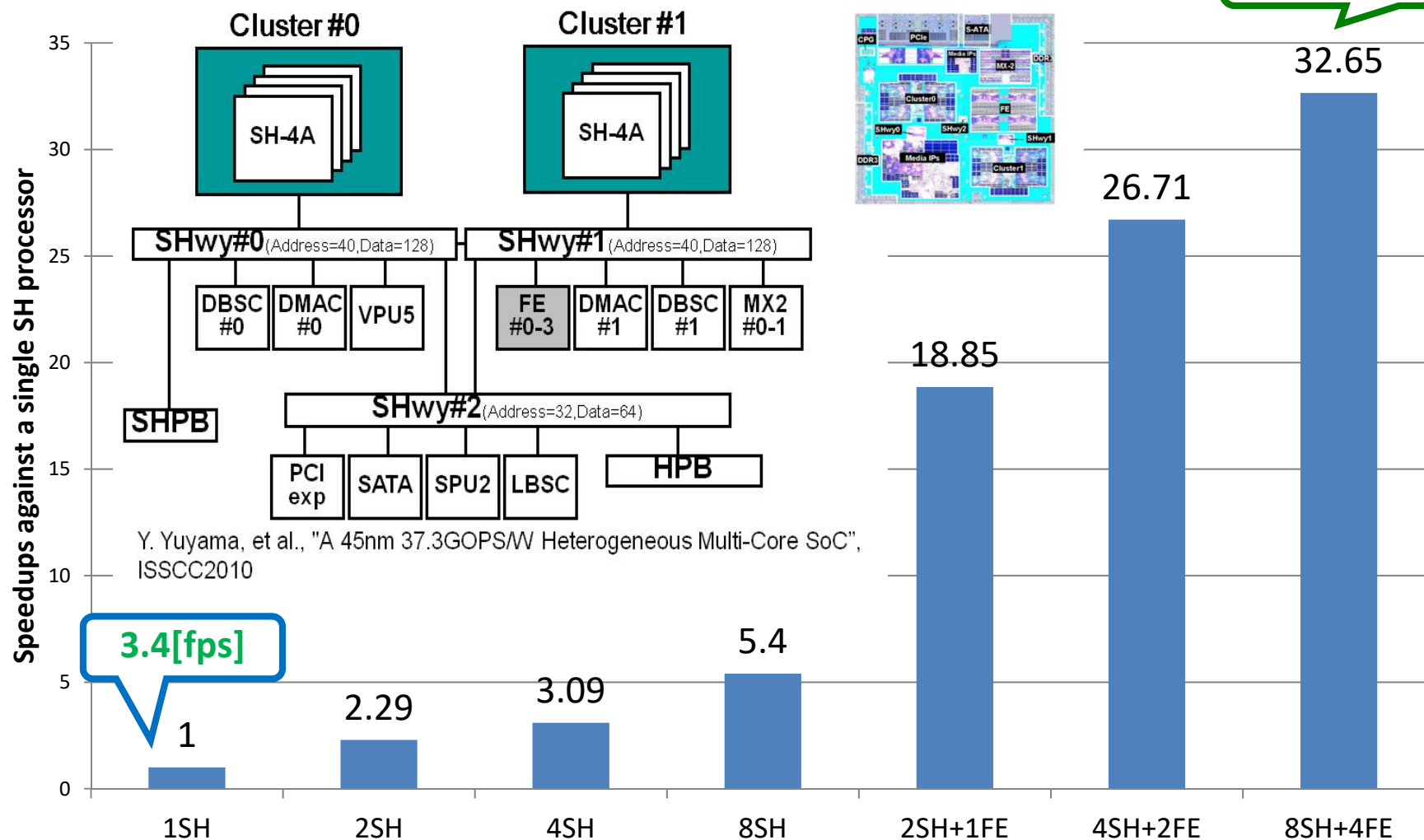 - complete_memop
  - noncacheable
  - aligncache

2 hint directives for OSCAR compiler
- accelerator_task
- oscar_comment

from V2.0

33 Times Speedup Using
OSCAR Compiler and OSCAR API on RP-X
(Optical Flow with a hand-tuned library)

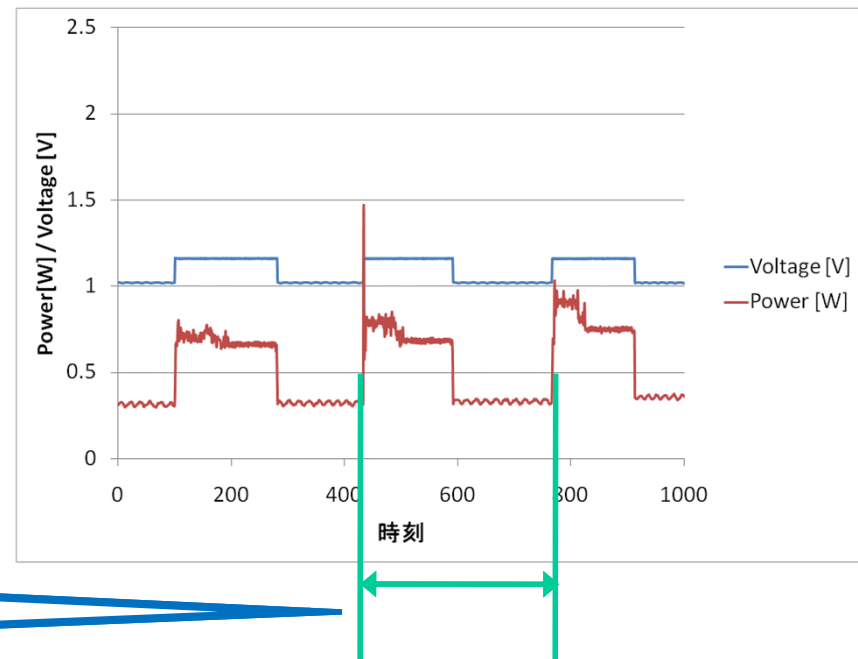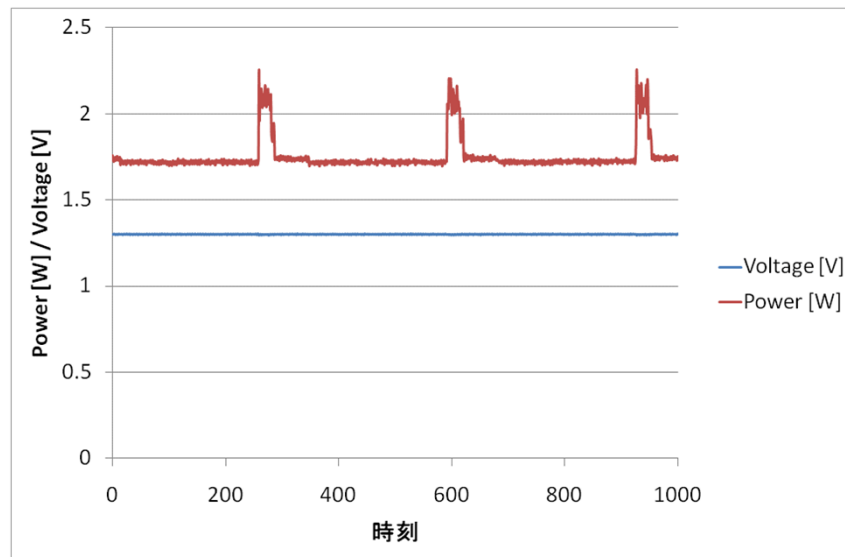Y. Yuyama, et al., "A 45nm 37.3GOPS/W Heterogeneous Multi-Core SoC", ISSCC2010

Power Reduction in a real-time execution controlled by OSCAR Compiler and OSCAR API on RP-X (Optical Flow with a hand-tuned library)

Without Power Reduction

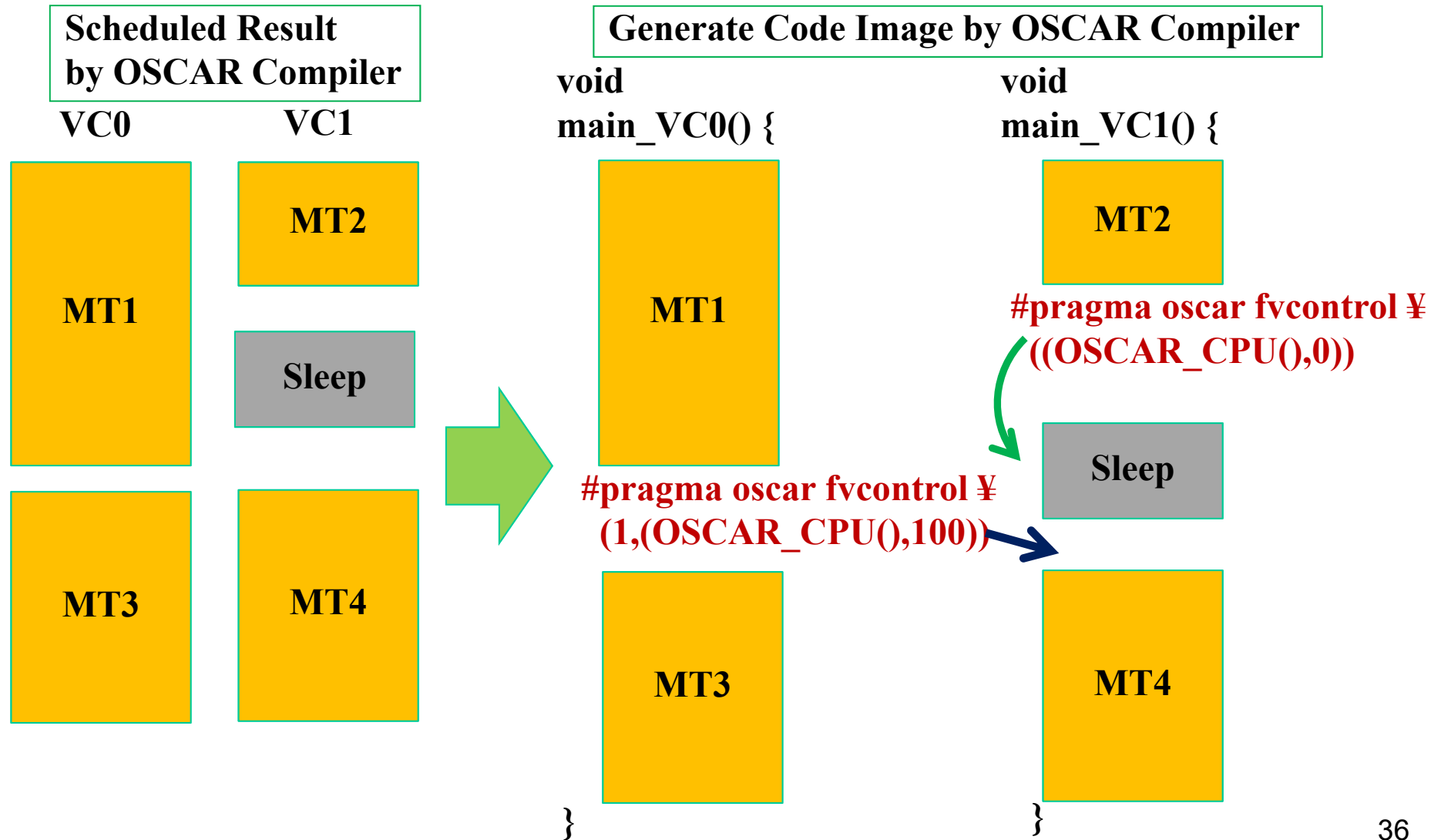**With Power Reduction by OSCAR Compiler**

70% of power reduction

Average:1.76[W] ➡ **Average:0.54[W]**
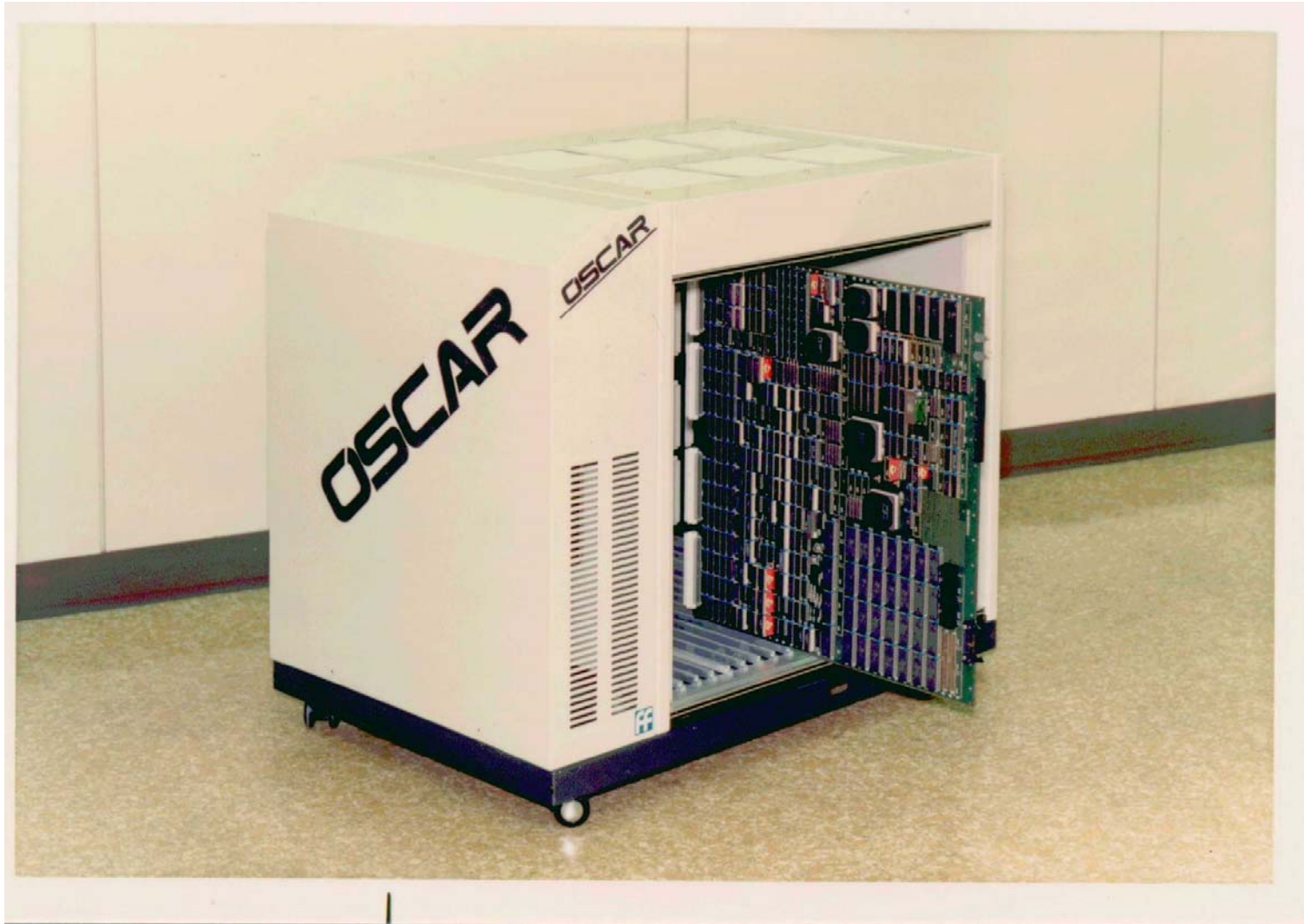

1cycle : 33[ms] →30[fps]

Low-Power Optimization with OSCAR API

Scheduled Result by OSCAR Compiler

VC0   VC1

MT1

MT2

Sleep

MT3   MT4

Generate Code Image by OSCAR Compiler

void
main_VC0() {

MT1

#pragma oscar fvcontrol ¥
(1,(OSCAR_CPU(),100))

MT3

}

void
main_VC1() {

MT2

#pragma oscar fvcontrol ¥
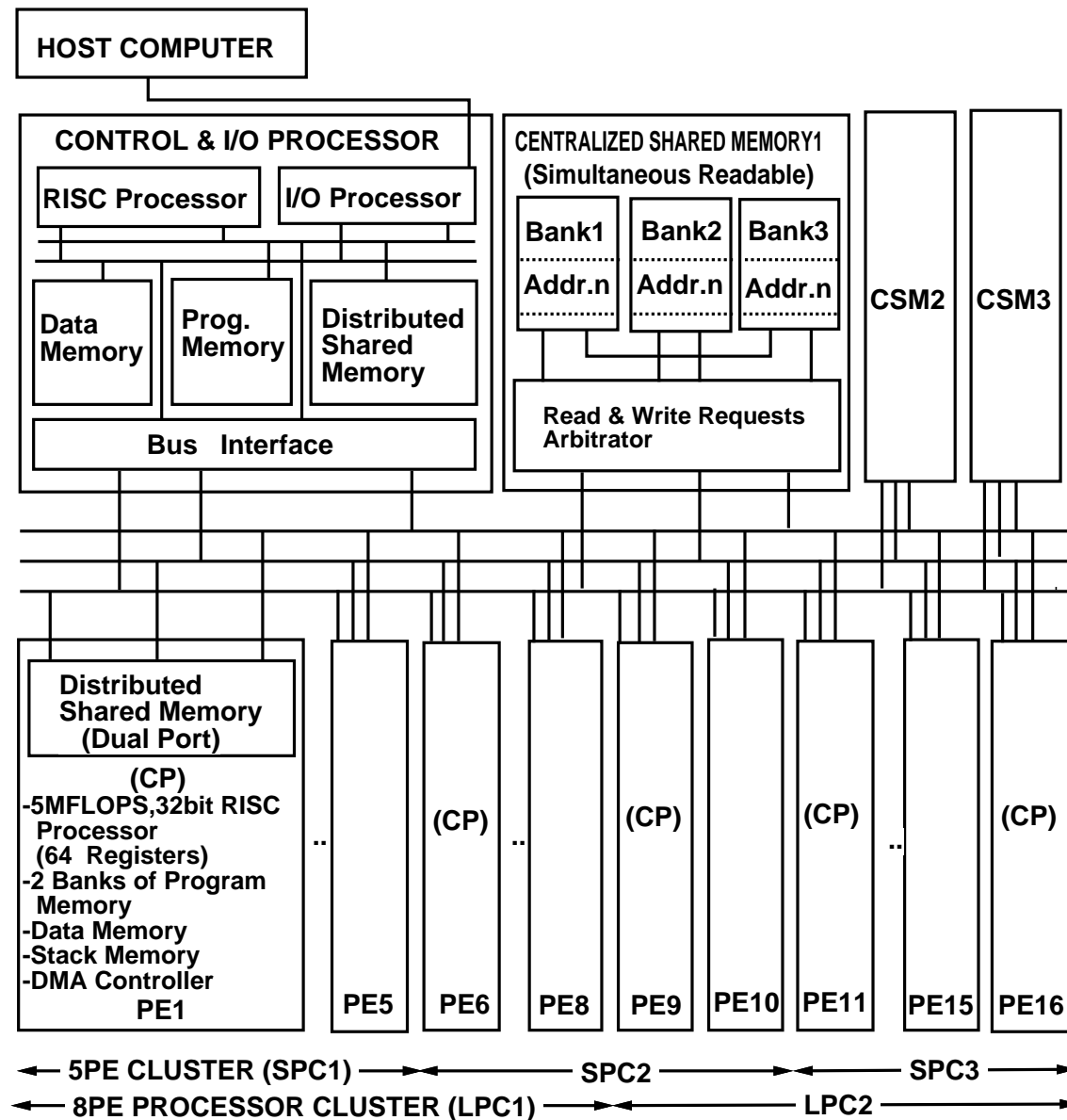((OSCAR_CPU(),0))

Sleep

MT4

}

36

1987 OSCAR(Optimally Scheduled Advanced Multiprocessor)
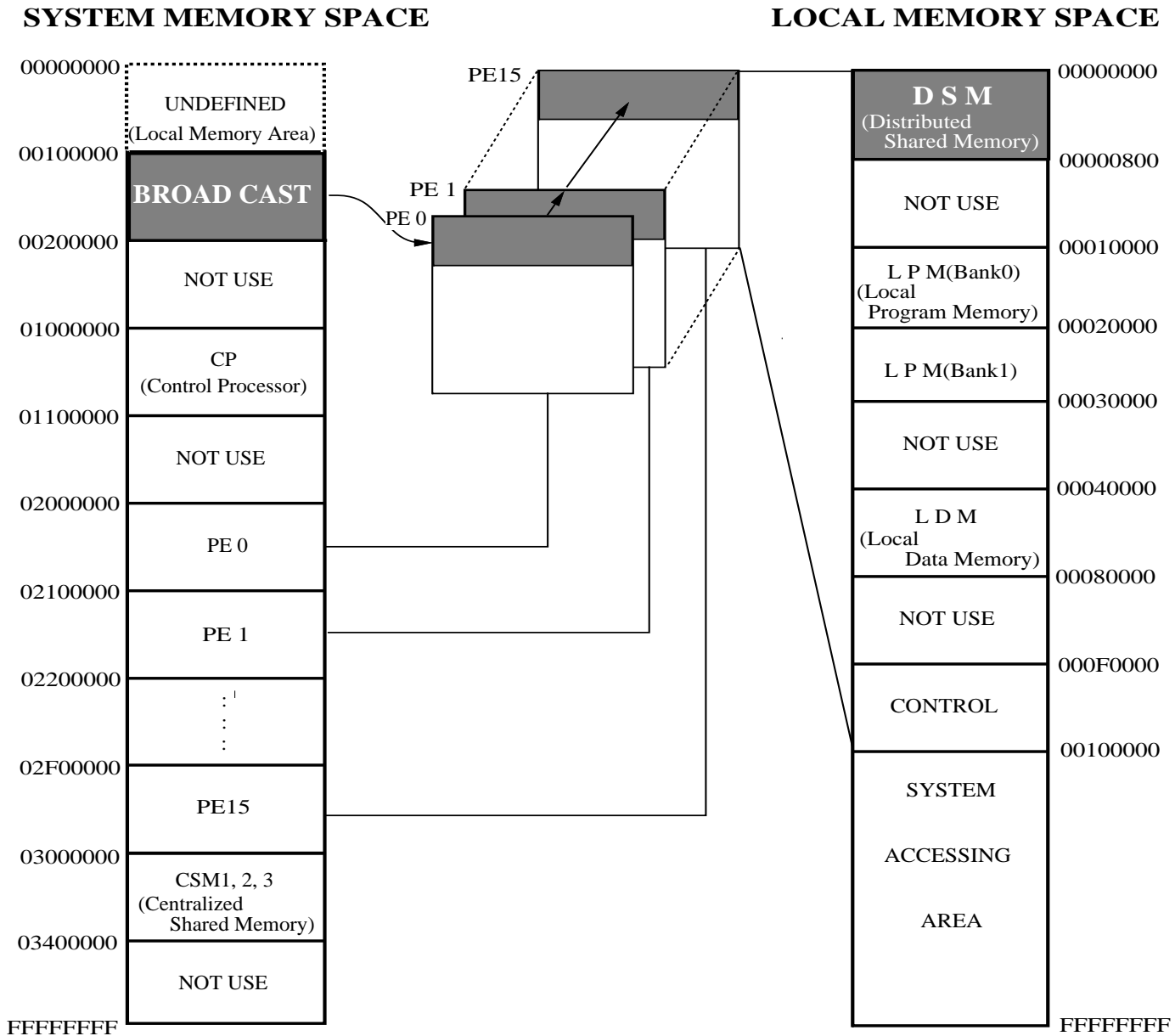
Co-design of Compiler and Architecture

Looking at various applications, design a parallelizing compiler and design a multiprocessor/multicore-processor to support compiler optimization
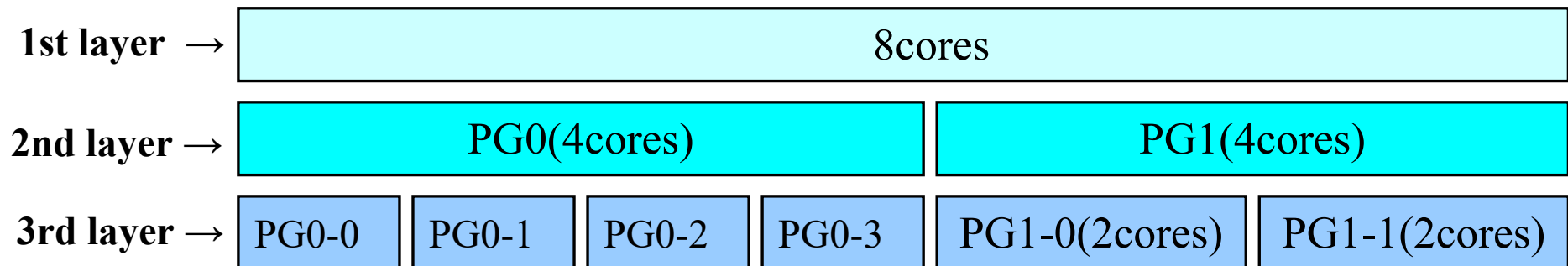
OSCAR(Optimally Scheduled Advanced Multiprocessor)

HOST COMPUTER

CONTROL & I/O PROCESSOR
- RISC Processor
- I/O Processor
- Data Memory
- Prog. Memory
- Distributed Shared Memory
- Bus Interface

CENTRALIZED SHARED MEMORY1 (Simultaneous Readable)
- Bank1 / Addr.n
- Bank2 / Addr.n
- Bank3 / Addr.n
- Read & Write Requests Arbitrator

CSM2

CSM3

Distributed Shared Memory (Dual Port)

(CP)
- 5MFLOPS,32bit RISC Processor (64 Registers)
- 2 Banks of Program Memory
- Data Memory
- Stack Memory
- DMA Controller

PE1

(CP) PE5 PE6

(CP) PE8 PE9

(CP) PE10 PE11

(CP) PE15 PE16

← 5PE CLUSTER (SPC1) → ← SPC2 → ← SPC3 →
← 8PE PROCESSOR CLUSTER (LPC1) → ← LPC2 →

38

OSCAR Memory Space (Global Address Space)

SYSTEM MEMORY SPACE

LOCAL MEMORY SPACE

SYSTEM MEMORY SPACE		LOCAL MEMORY SPACE	
00000000	UNDEFINED (Local Memory Area)	D S M (Distributed Shared Memory)	00000000
00100000	BROAD CAST	NOT USE	00000800
00200000	NOT USE	L P M(Bank0) (Local Program Memory)	00010000
01000000	CP (Control Processor)	L P M(Bank1)	00020000
01100000	NOT USE	NOT USE	00030000
02000000	PE 0	L D M (Local Data Memory)	00040000
02100000	PE 1	NOT USE	00080000
02200000	⋮	CONTROL	000F0000
02F00000	PE15	SYSTEM ACCESSING AREA	00100000
03000000	CSM1, 2, 3 (Centralized Shared Memory)		
03400000	NOT USE		
FFFFFFFF			FFFFFFFF

39

Hierarchical Barrier Synchronization

- ## Specifying a hierarchical group barrier
  - ### #pragma oscar group_barrier (C)
  - ### !$oscar group_barrier (Fortran)

1st layer →	8cores

2nd layer →	PG0(4cores)	PG1(4cores)

3rd layer →	PG0-0	PG0-1	PG0-2	PG0-3	PG1-0(2cores)	PG1-1(2cores)

NWT

Machine Cycle Time	9.5ns (105MHz)
PE Performance	1.68GFlops
PE Memory Size	256MB/PE
Crossbar Bandwidth	4B/cycle x 2 (send/receive simultaneous)/PE = 421MB/s x 2 /PE
Number of PEs	140PEs + 2Control Proc.

NAL computer center, Chofu, Tokyo, Feb. 1, 1993

Fujitsu Vector Parallel Supercomputer with Crossbar to a Chip
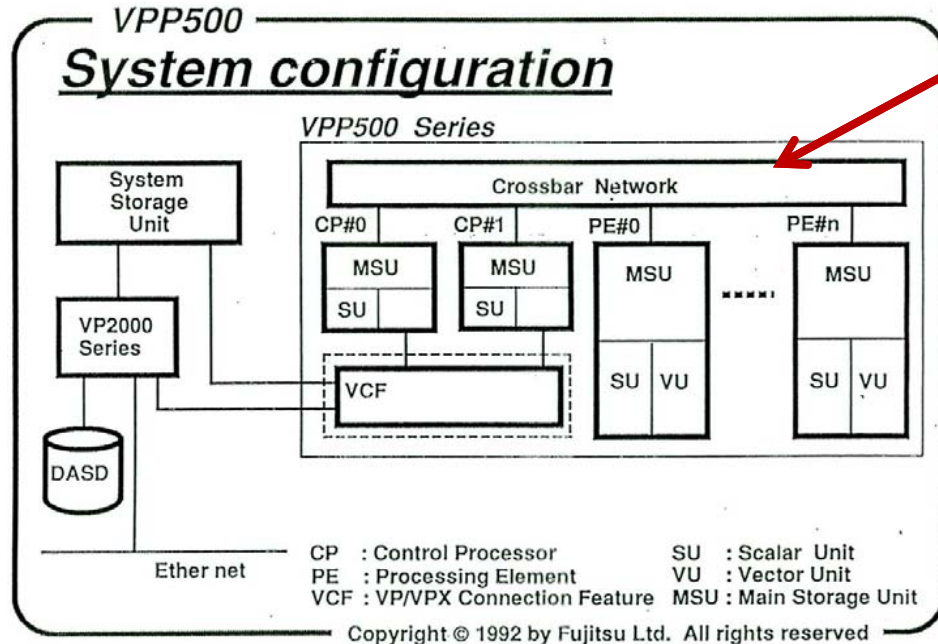
Crossbar Network
VPP500: 256*256
VPP5000: 1024*1024

VPP500
GaAs/BiCMOS/ECL
Water Cooling
10ns
1GB/PE
in Separate Cabinet
1.6GFLOPS/PE
32bit address
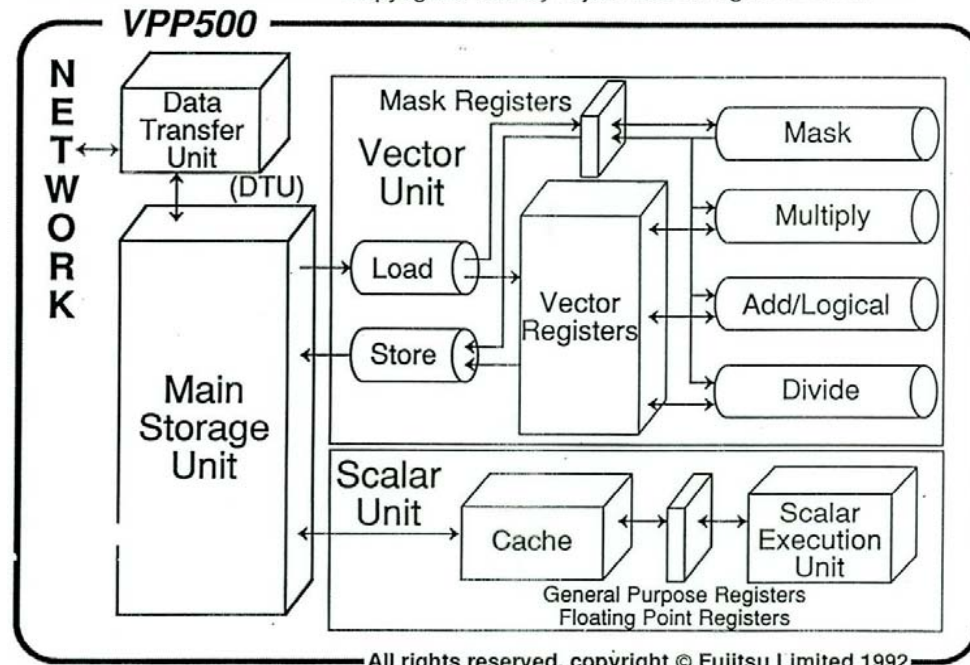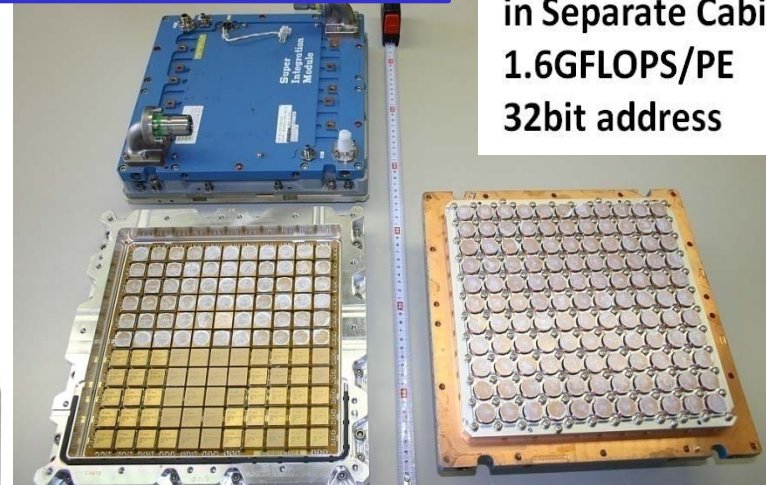
VPP5000
0.25um CMOS
30M Tr./Chip
Forced Air Cooling
3.5ns clock cycle
8GB/PE
on PE Board
9.1GFLOPS/PE
32/64 bit address

42

VPP500/NWT

PE Unit

Super
Integration
Module
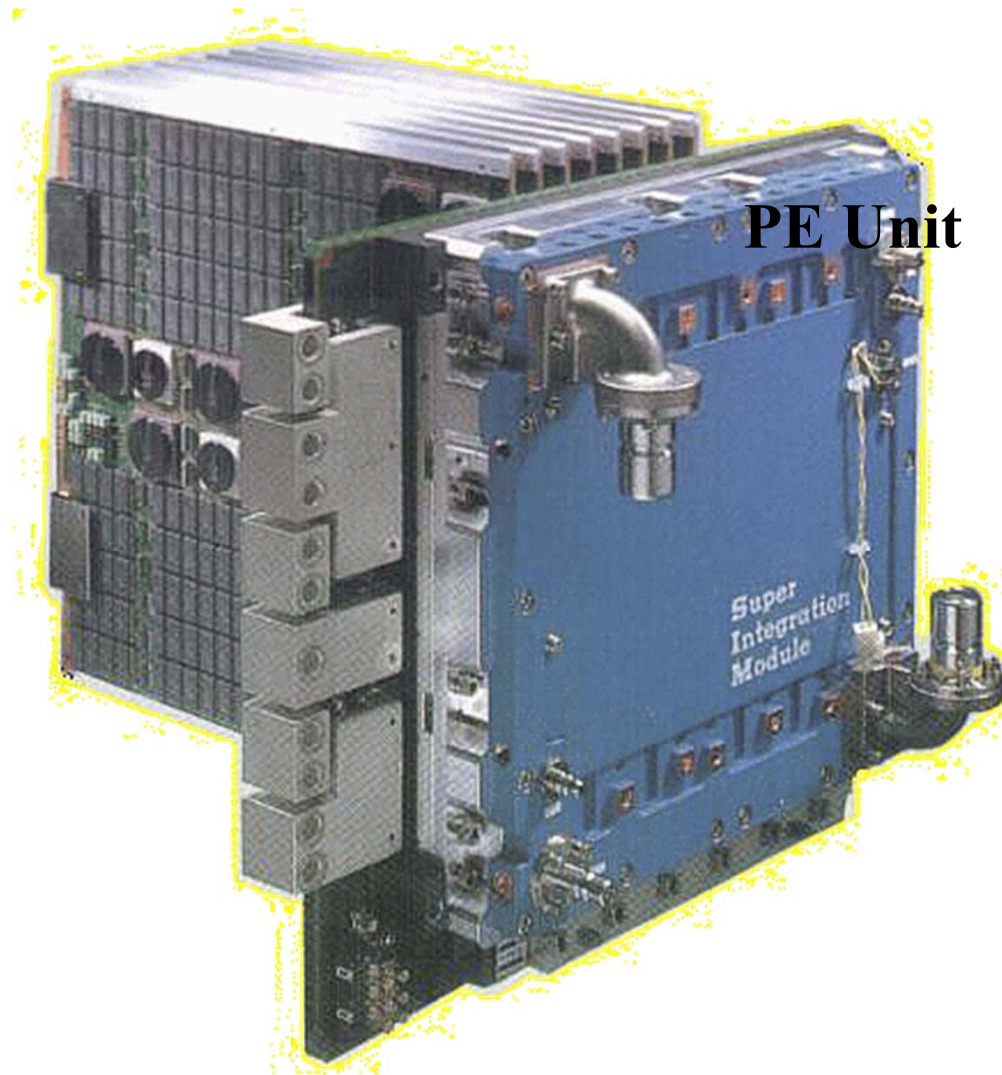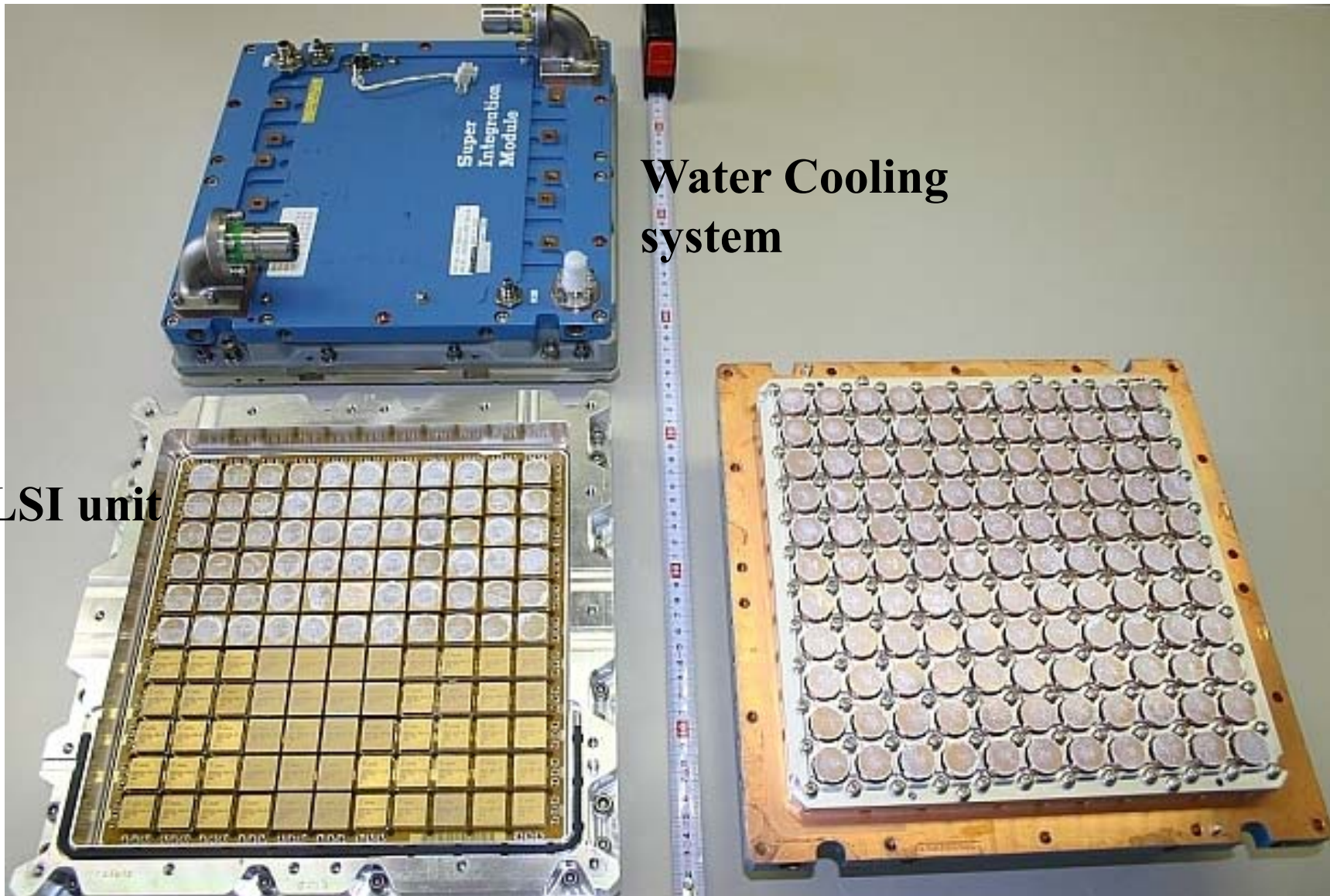
VPP500/NWT

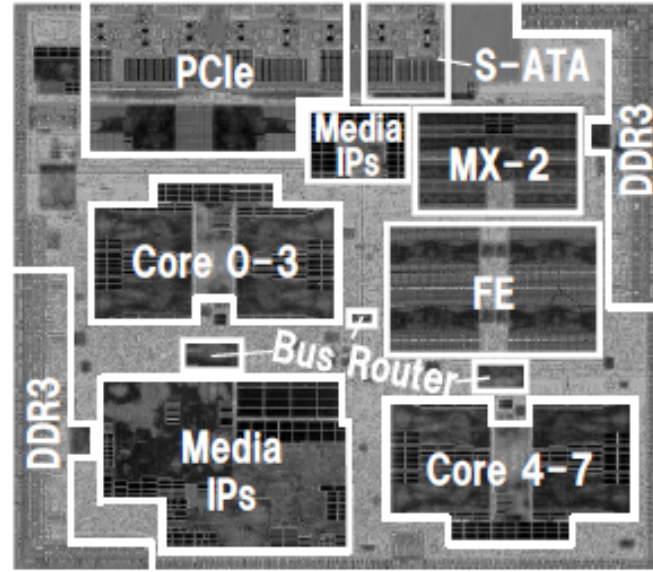**Water Cooling system**
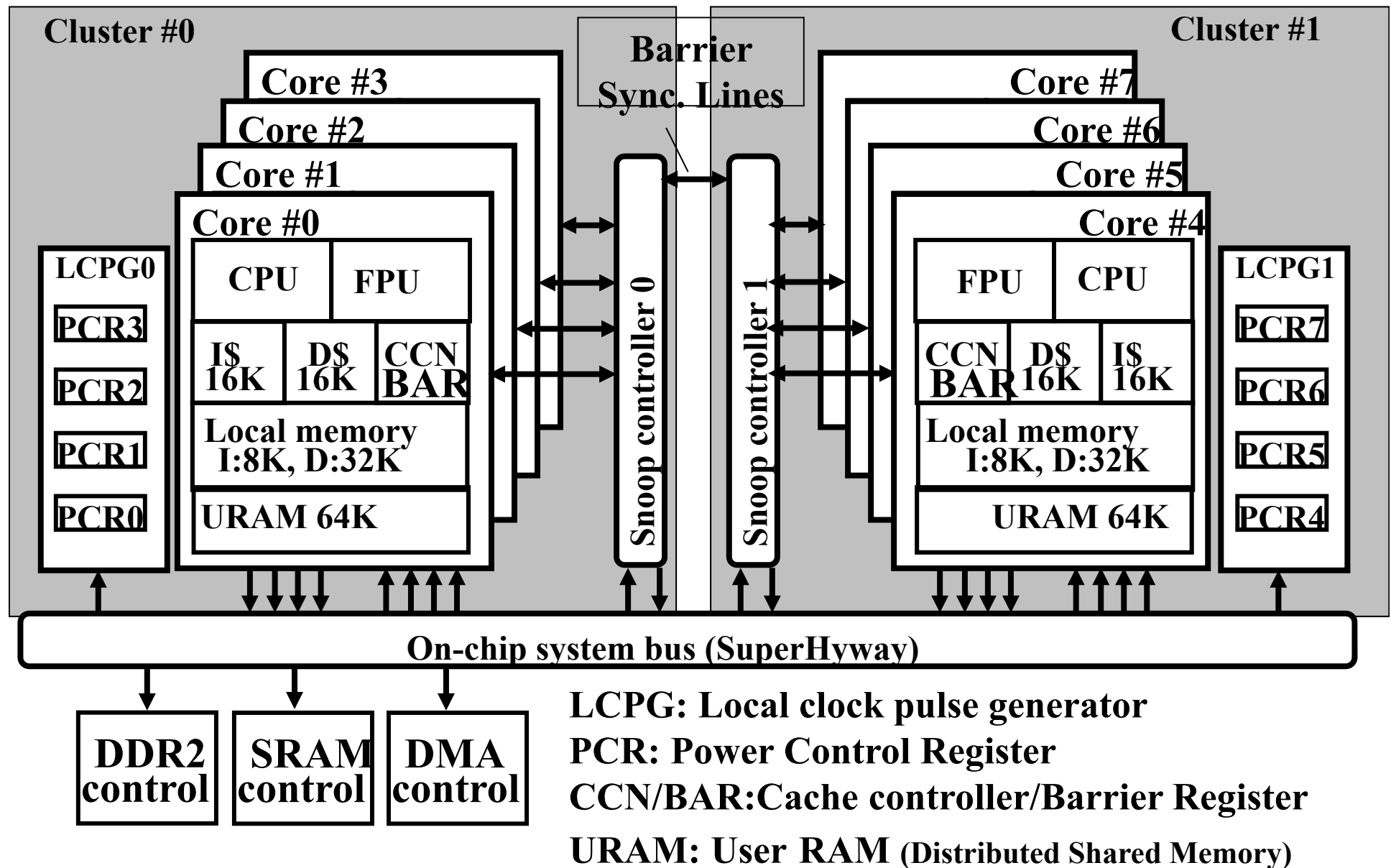
PE LSI unit

VPP500/NWT
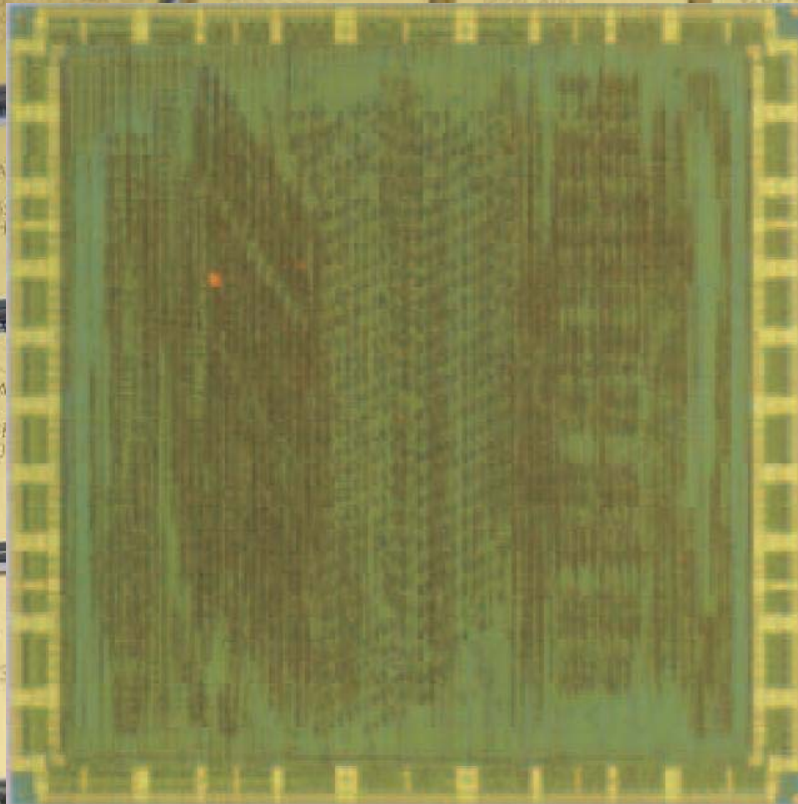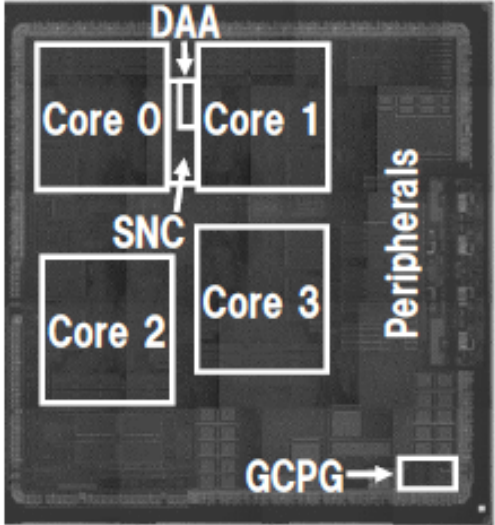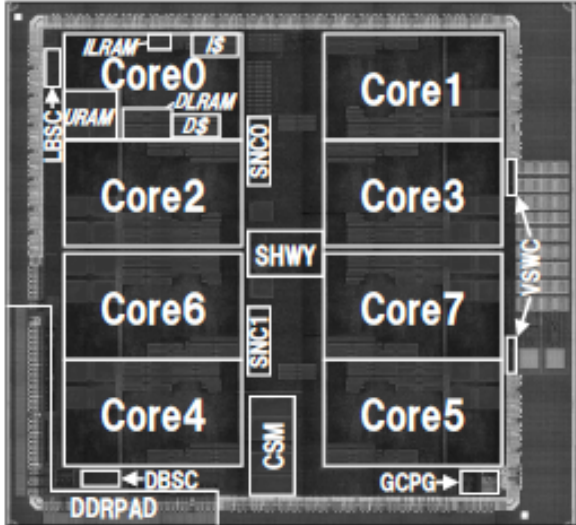
GaAs **BiCMOS**
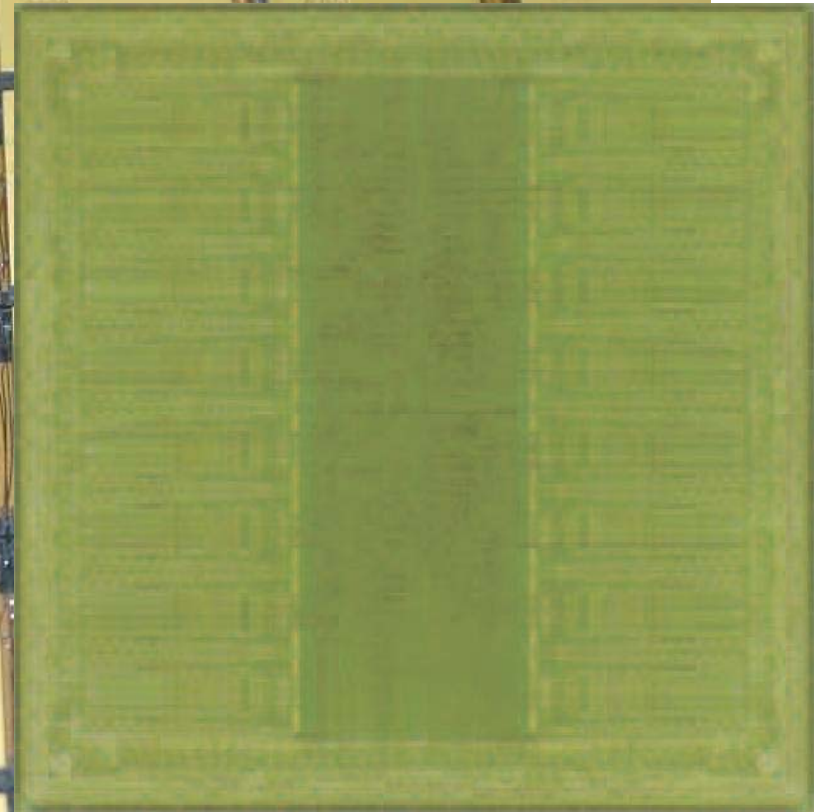
4 core multicore RP1 (2007) , 8 core multicore RP2 (2008) and 15 core Heterogeneous multicore RPX (2010) developed in NEDO Projects with Hitachi and Renesas

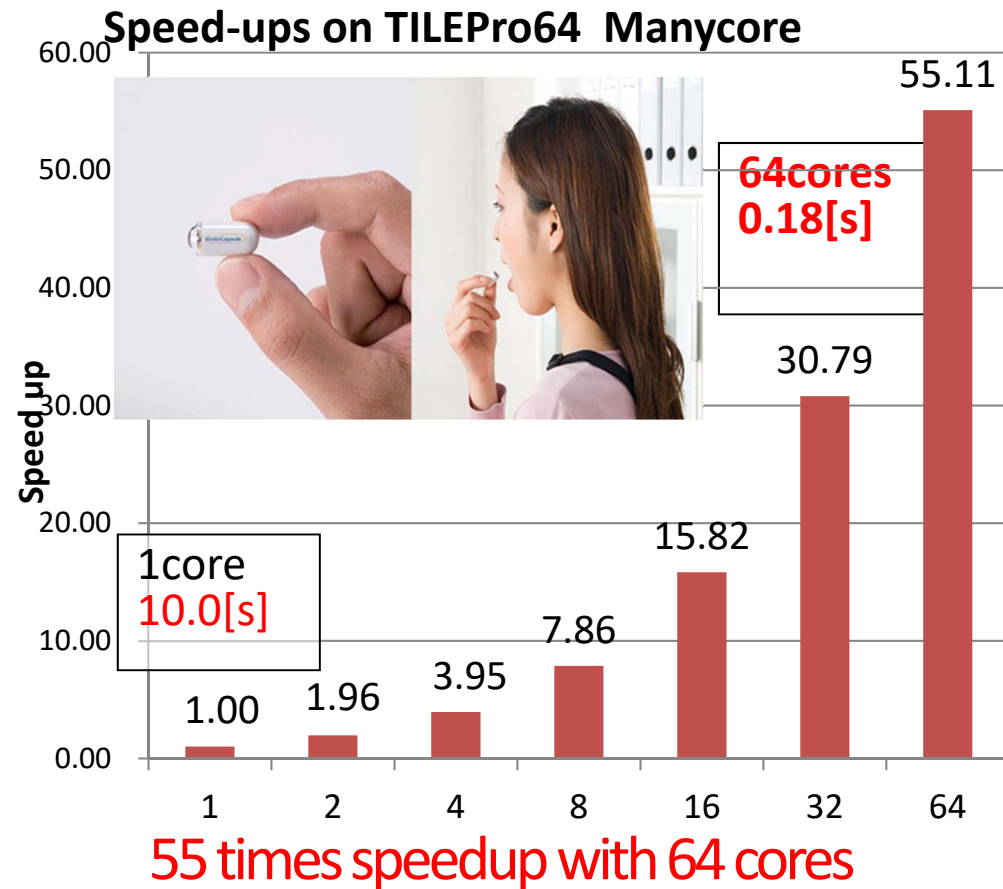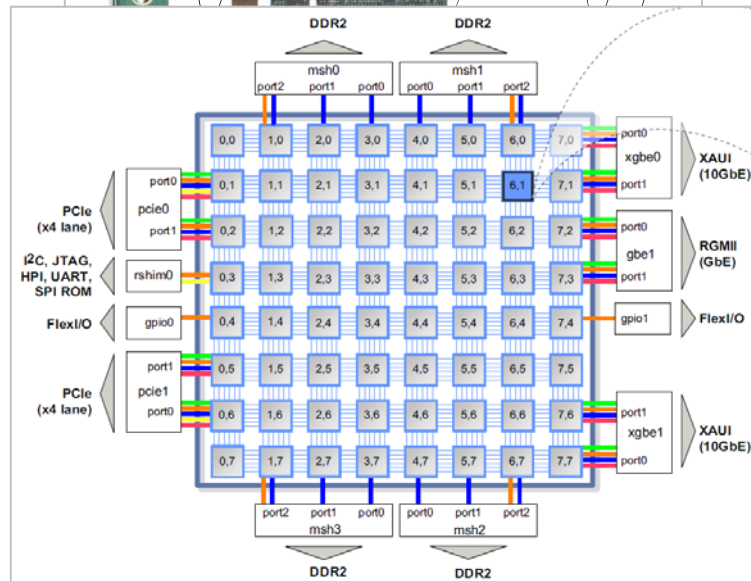| *RP-1* (ISSCC2007 #5.3)	*RP-2* (ISSCC2008 #4.5)	*RP-X* (ISSCC2010 #5.3)
90nm, 8-layer, triple-Vth, CMOS	90nm, 8-layer, triple-Vth, CMOS	45nm, 8-layer, triple-Vth, CMOS
97.6 mm^2 (9.88 x 9.88 mm)	104.8 mm^2 (10.61 x 9.88 mm)	153.8 mm^2 (12.4 x 12.4 mm)
1.0V (internal), 1.8/3.3V (I/O)	1.0-1.4V (internal), 1.8/3.3V (I/O)	1.0-1.2V (internal), 1.2-3.3V (I/O)
600MHz ,4.32 GIPS,16.8 GFLOPS	600MHz , 8.64 GIPS, 33.6 GFLOPS	648MHz, 13.7GIPS, 115GOPS, 36.2GFLOPS
11.4 GOPS/W（32b換算）	18.3 GOPS/W（32b換算）	37.3 GOPS/W（32b換算）

8 Core RP2 Chip Block Diagram

Cluster #0

Cluster #1

Barrier Sync. Lines

Core #3
Core #2
Core #1
Core #0

Core #7
Core #6
Core #5
Core #4

LCPG0
- PCR3
- PCR2
- PCR1
- PCR0

LCPG1
- PCR7
- PCR6
- PCR5
- PCR4

Core #0: CPU | FPU | I$ 16K | D$ 16K | CCN BAR | Local memory I:8K, D:32K | URAM 64K

Core #4: FPU | CPU | CCN BAR | D$ 16K | I$ 16K | Local memory I:8K, D:32K | URAM 64K

Snoop controller 0

Snoop controller 1

On-chip system bus (SuperHyway)

DDR2 control

SRAM control

DMA control

LCPG: Local clock pulse generator
PCR: Power Control Register
CCN/BAR:Cache controller/Barrier Register
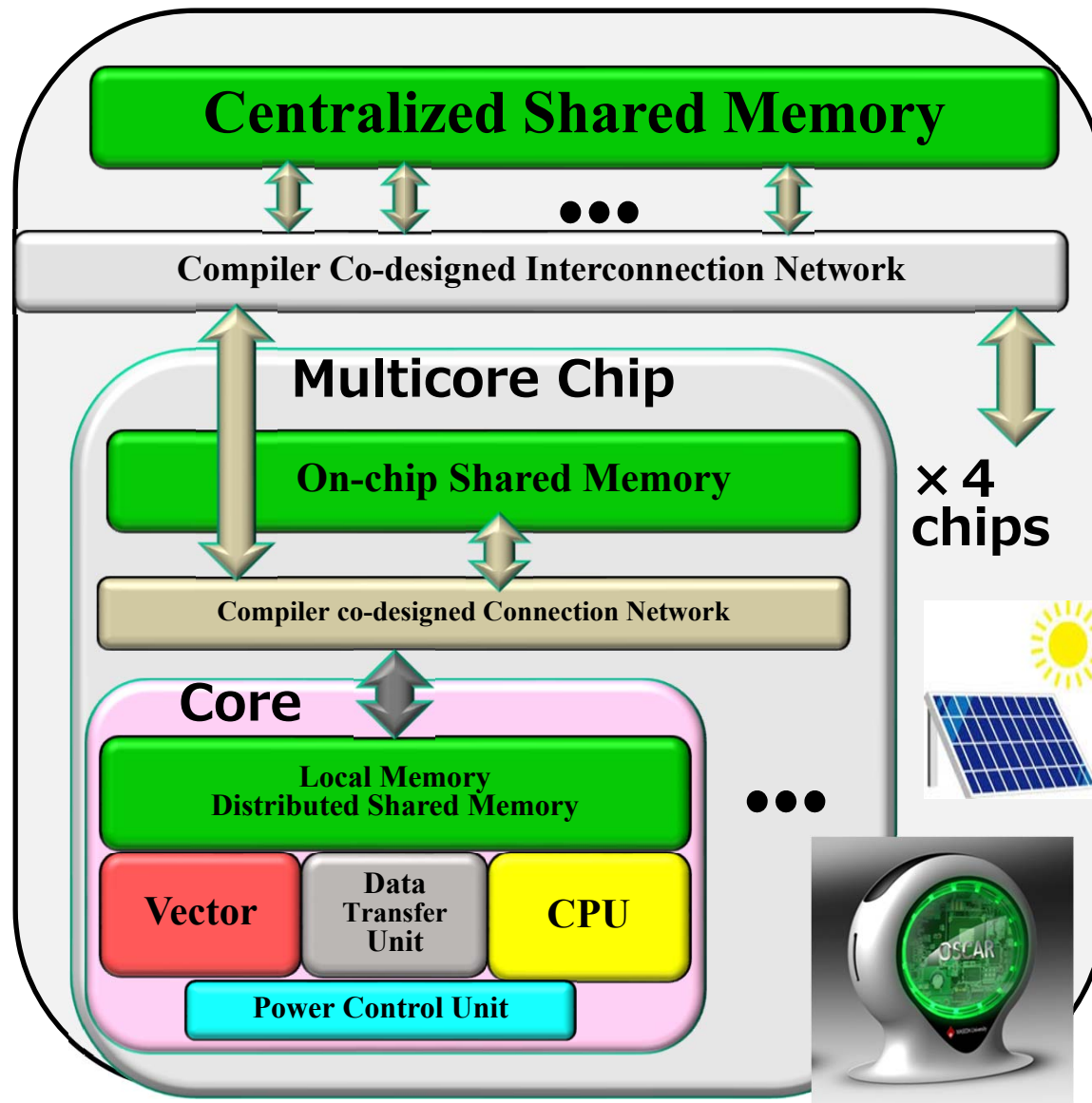URAM: User RAM (Distributed Shared Memory)

Automatic Parallelization of JPEG-XR for Drinkable Inner Camera (Endo Capsule)

10 times more speedup needed after parallelization for 128 cores of Power 7. Less than 35mW power consumption is required.

- TILEPro64

Speed-ups on TILEPro64 Manycore

64cores 0.18[s]

1core 10.0[s]

cores	speedup
1	1.00
2	1.96
4	3.95
8	7.86
16	15.82
32	30.79
64	55.11

55 times speedup with 64 cores
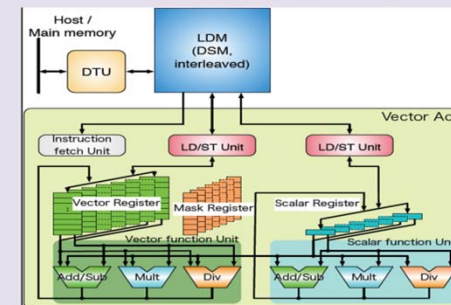
OSCAR Technology Corp.

Started up on Feb. 28, 2013:

Licensing the all patents and OSCAR compiler from Waseda Univ.

Founder and CEO: Dr. T. Ono **(Ex- CEO of First Section-listed Company, Director of National U., Invited Prof. of Waseda U.)**

Executives: Dr. M. Ohashi : COO (Ex- OO of Ono Sokki)

Mr. A. Nodomi : CTO (Ex- Spansion)

Mr. N. Ito (Ex- Visiting Prof. Tokyo Agricult. And Tech. U.)

Dr. K. Shirai (Ex- President of Waseda U., Ex- Chairman of Japanese Open U.)

Mr. K. Ashida (Ex- VP Sumitomo Trading, Adhida Consult. CEO)

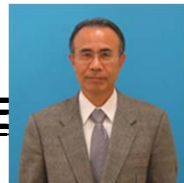**Mr. S. Tsuchida (Co-Chief Investment Officer of Innovation Network Corp. of Japan)**

Auditor: Mr. S. Honda (Ex- Senior VP and General Manager of MUFG)

Dr. S. Matuda (Emeritus Prof. of Waseda U., Chairman of WERU INVESTME
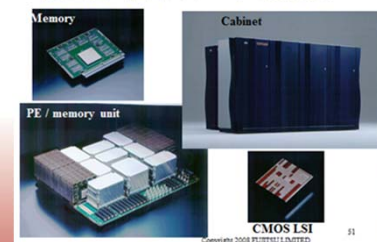
Mr. Y. Hirowatari (President of AGS Consulting)

Advisors: Prof. H. Kasahara (Waseda U.)

Prof. K. Kimura (Waseda U.)

OSCAR TECHNOLOGY CORPORATION

Future Multicore Products

Next Generation Automobiles

- Safer, more comfortable, energy efficient, environment friendly
- Cameras, radar, car2car communication, internet information integrated brake, steering, engine, moter control

Smart phones

-From everyday recharging to less than once a week
- Solar powered operation in emergency condition
- Keep health

Advanced medical systems

**Cancer treatment,
Drinkable inner camera**

- Emergency solar powered
- No cooling fun, No dust , clean usable inside OP room

Personal / Regional Supercomputers

Solar powered with more than 100 times power efficient : FLOPS/W

- Regional Disaster Simulators saving lives from tornadoes, localized heavy rain, fires with earth quakes

Summary

- Waseda University Green Computing Systems R&D Center supported by METI has been researching on low-power high performance Green Multicore hardware, software and application with industry including Hitachi, Fujitsu, NEC, Renesas, Denso, Toyota, Olympus and OSCAR Technology.

- OSCAR Automatic Parallelizing and Power Reducing Compiler has succeeded speedup and/or power reduction of scientific applications including "Earthquake Wave Propagation", medical applications including "Cancer Treatment Using Carbon Ion", and "Drinkable Inner Camera", industry application including "Automobile Engine Control", "Smartphone", and "Wireless communication Base Band Processing" on various multicores from different vendors including Intel, ARM, IBM, AMD, Qualcomm, Freescale, Renesas and Fujitsu.

- In automatic parallelization, 110 times speedup for "Earthquake Wave Propagation Simulation" on 128 cores of IBM Power 7 against 1 core, 55 times speedup for "Carbon Ion Radiotherapy Cancer Treatment" on 64cores IBM Power7, 1.95 times for "Automobile Engine Control" on Renesas 2 cores using SH4A or V850, 55 times for "JPEG-XR Encoding for Capsule Inner Cameras" on Tilera 64 cores Tile64 manycore.

  - The compiler will be available on market from OSCAR Technology.

- In automatic power reduction, consumed powers for real-time multi-media applications like Human face detection, H.264, mpeg2 and optical flow were reduced to 1/2 or 1/3 using 3 cores of ARM Cortex A9 and Intel Haswell and 1/4 using Renesas SH4A 8 cores against ordinary single core execution.

- Local memory management for automobiles and software coherent control have been patented and already realized by OSCAR compiler.