

OSCAR Parallelizing Compiler and Its Performance for Embedded Applications

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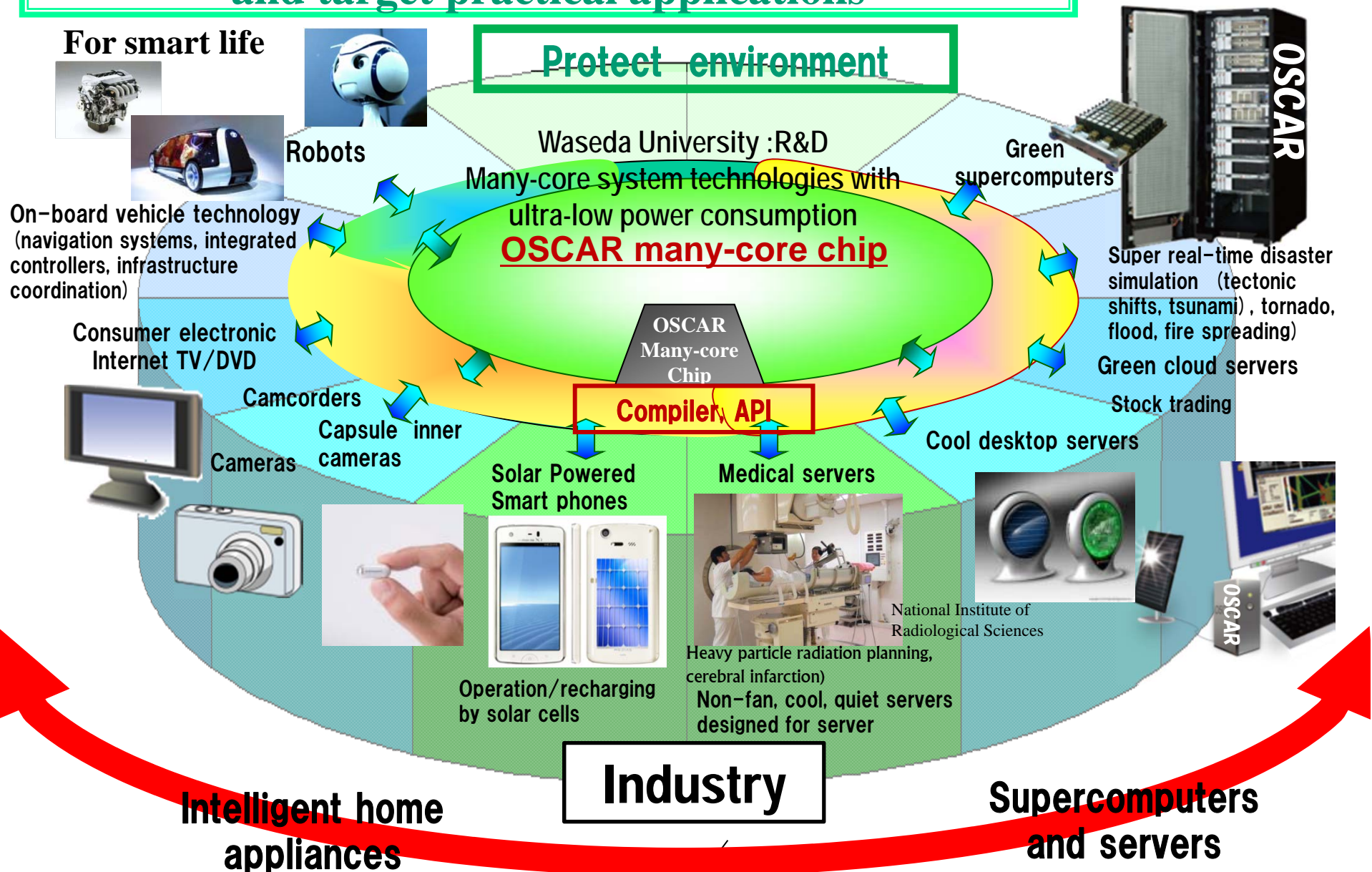
URL: <http://www.kasahara.cs.waseda.ac.jp/>

Industry-government-academia collaboration in R&D and target practical applications

Protect lives

For smart life

Protect environment



OSCAR Parallelizing Compiler

To improve **effective performance**, **cost-performance** and **software productivity** and **reduce power**

Multigrain Parallelization

coarse-grain parallelism among loops and subroutines, near fine grain parallelism among statements in addition to loop parallelism

Data Localization

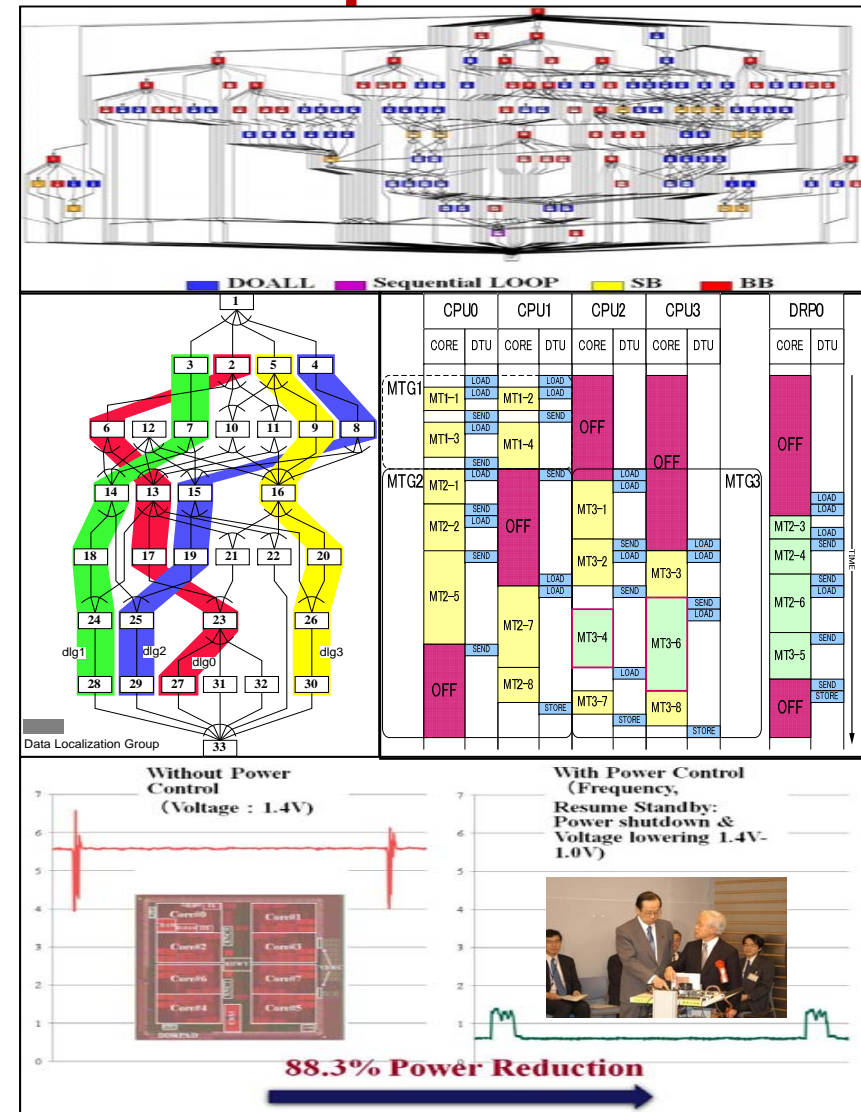
Automatic data management for distributed shared memory, cache and local memory

Data Transfer Overlapping

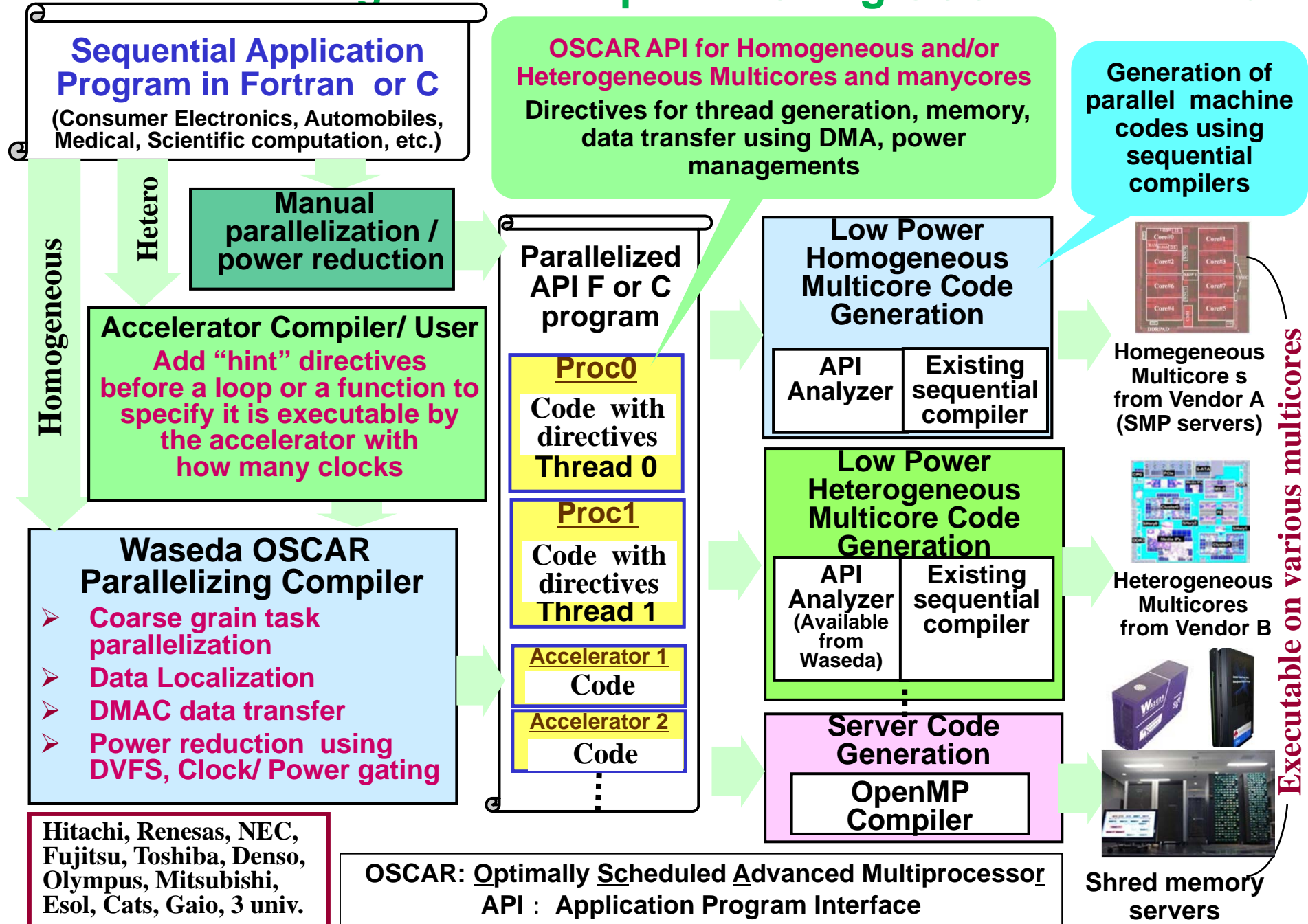
Data transfer overlapping using Data Transfer Controllers (DMAs)

Power Reduction

Reduction of consumed power by compiler control DVFS and Power gating with hardware supports.



Multicore Program Development Using OSCAR API V2.0



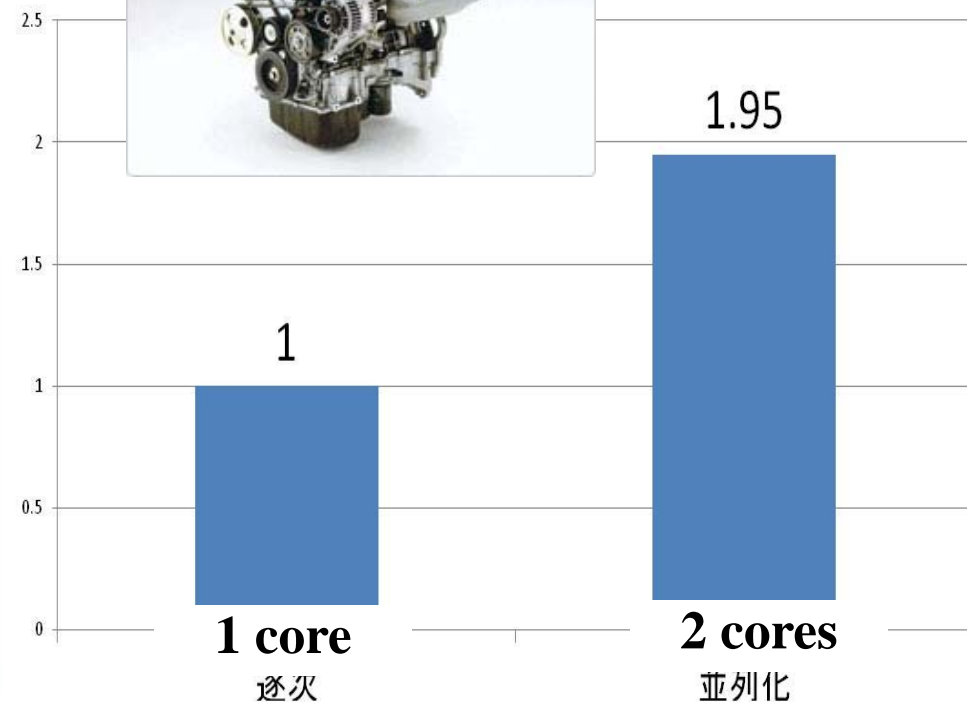
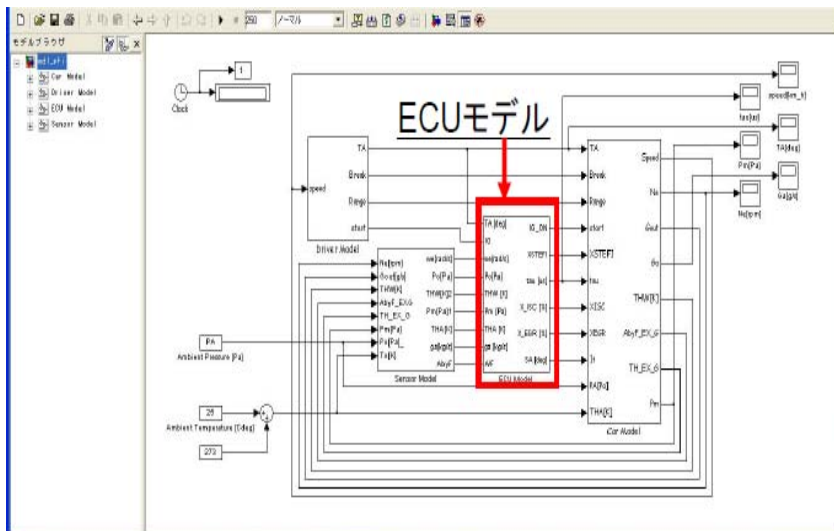


Engine Control by multicore with Denso

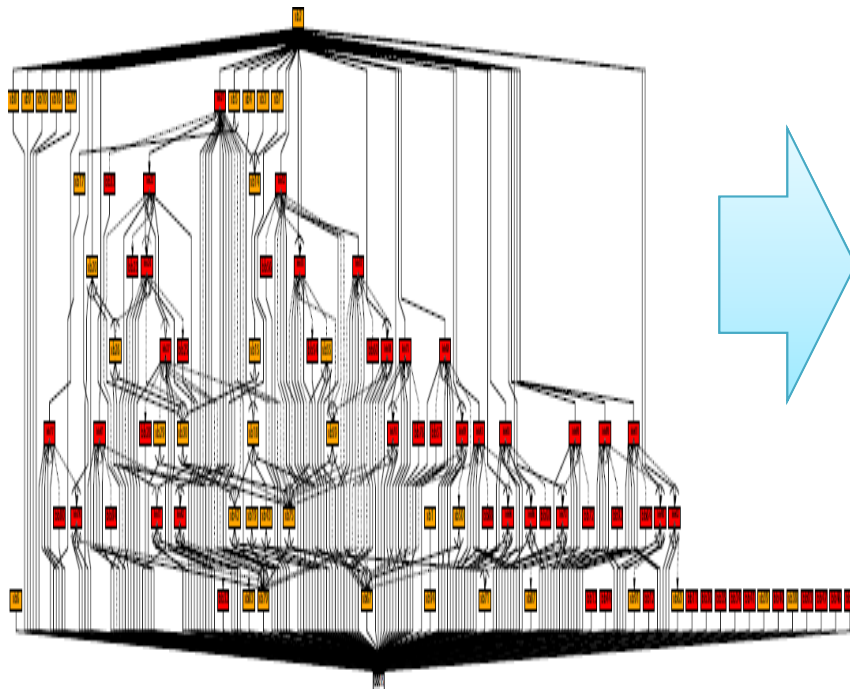
Though so far parallel processing of the engine control on multicore has been very difficult, Denso and Waseda succeeded 1.95 times speedup on 2core V850 multicore processor.



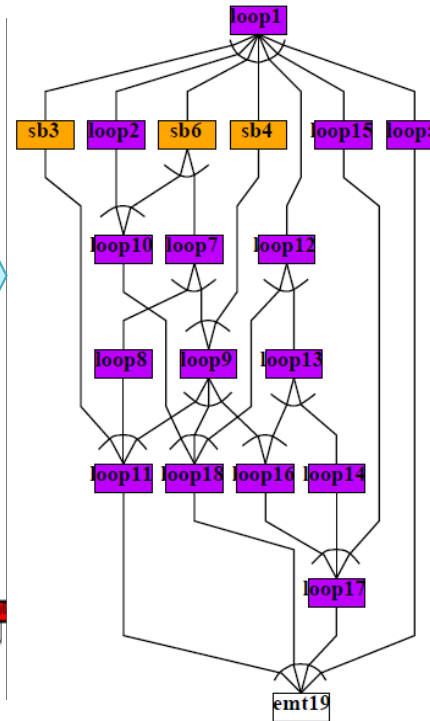
Hard real-time
automobile engine
control by multicore



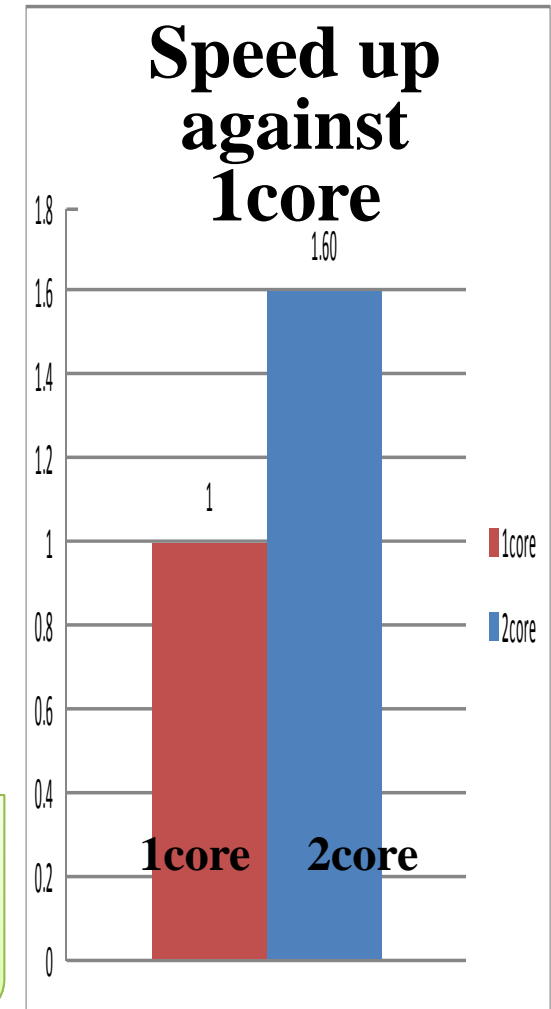
Speedup with 2cores for Engine Crankshaft Handwritten Program on RPX Multi-core Processor



**Macrotask graph with
plenty of conditional
branches**

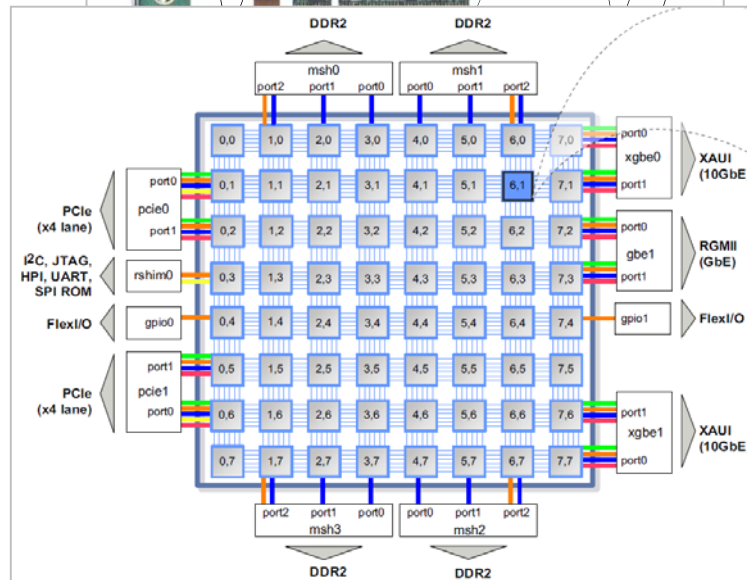


**Macrotask
graph after
task fusion**

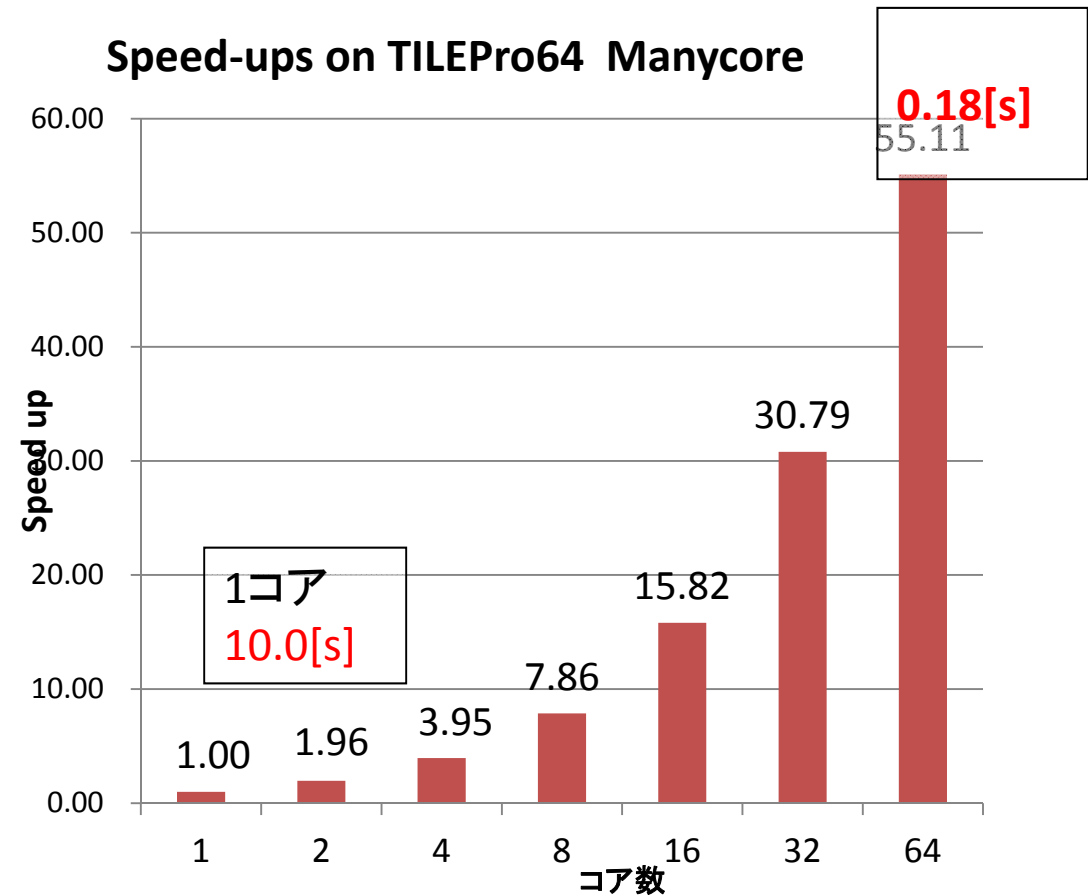


Automatic Parallelization of Still Image Encoding Using JPEG-XR for the Next Generation Cameras and Drinkable Inner Camera

- TILEPro64

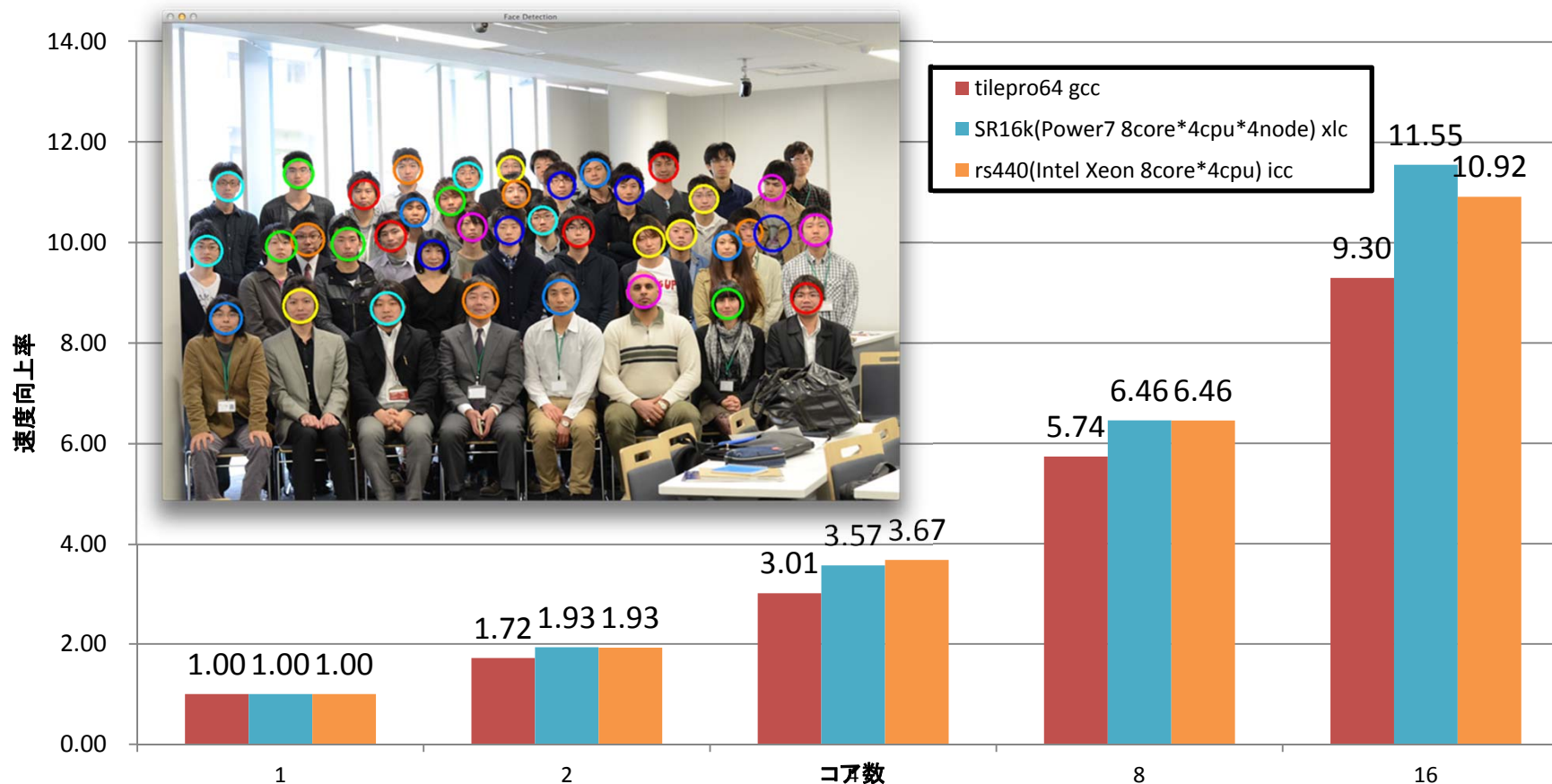


Speed-ups on TILEPro64 Manycore



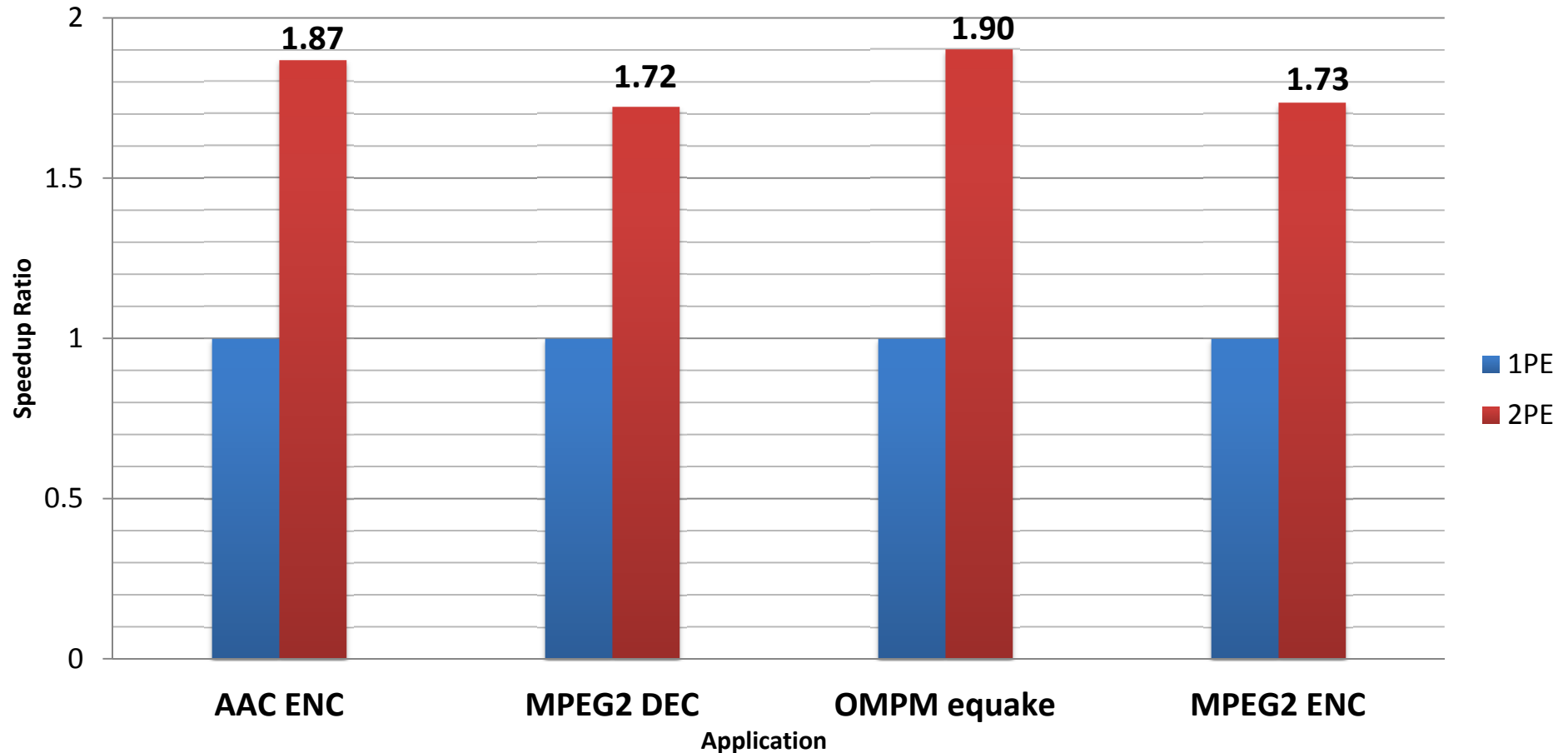
55 times speedup with 64 cores
against 1 core

Parallel Processing of Face Detection on Manycore, Highend and PC Server



- OSCAR compiler gives us **11.55 times** speedup for 16 cores against 1 core on SR16000 Power7 highend server.

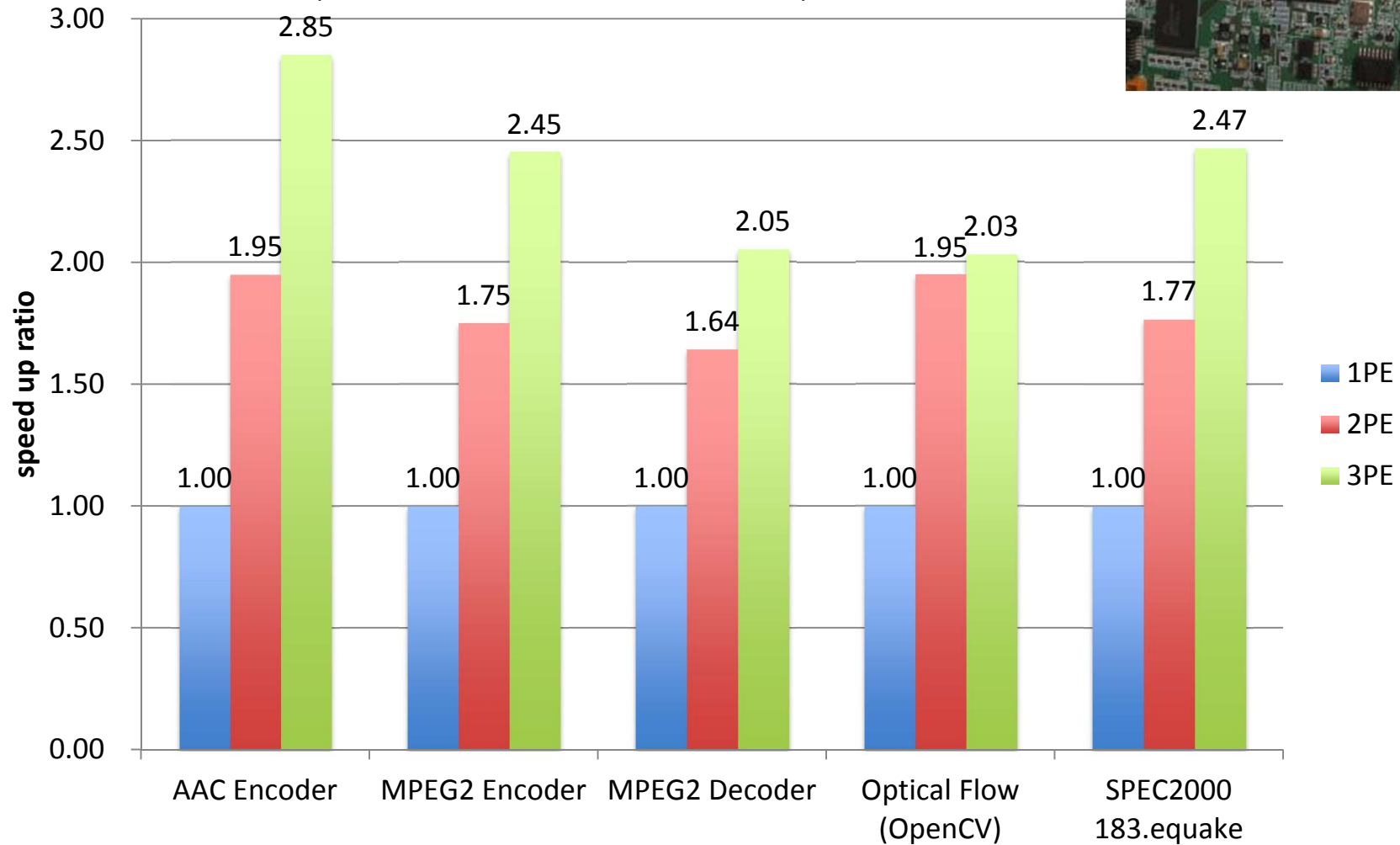
Performance of OSCAR Compiler & API on 2 ARMv7-cores Qualcomm MSM8960 (Snapdragon) Android 4.0 for Smart Phones



1.81 times speedup by 2 cores on the average against 1 core

Parallel Processing Performance on 3Cores NaviEngine with Realtime OS eT-Kernel Multi-Core Edition

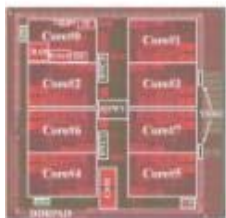
NaviEngine (ARM11 MPCore) 400MHz 3 core SMP
(Renesas Electronics EC-4260)



- 2.37 times speedup on 3ARM cores against 1 core

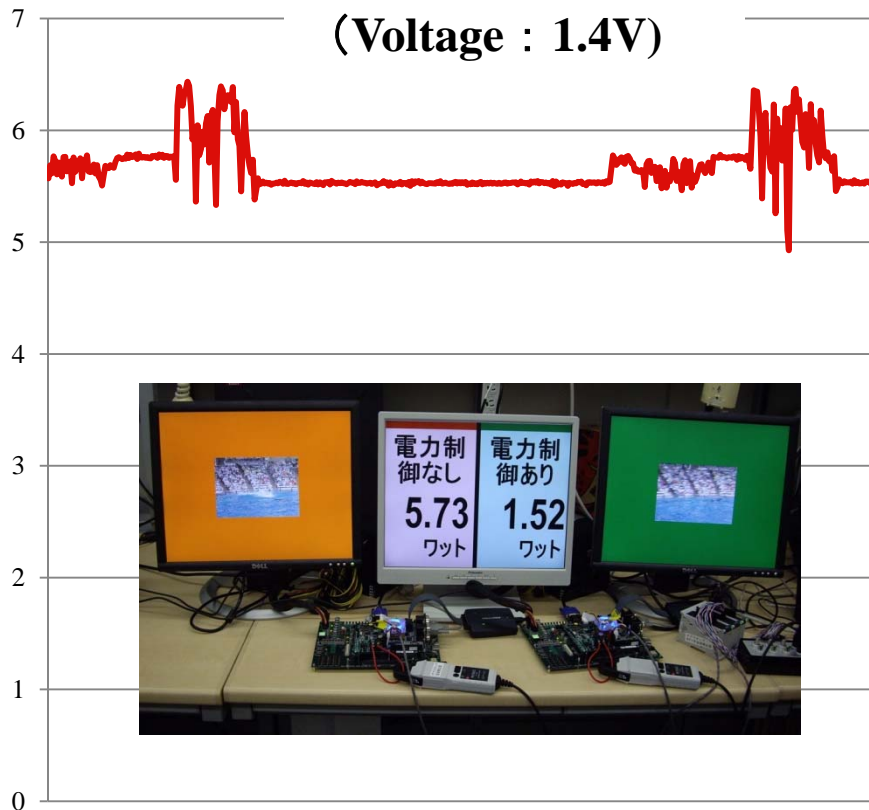
Power Reduction of MPEG2 Decoding to 1/4 on 8 Core Homogeneous Multicore RP-2 by OSCAR Parallelizing Compiler

MPEG2 Decoding with 8 CPU cores



Without Power
Control

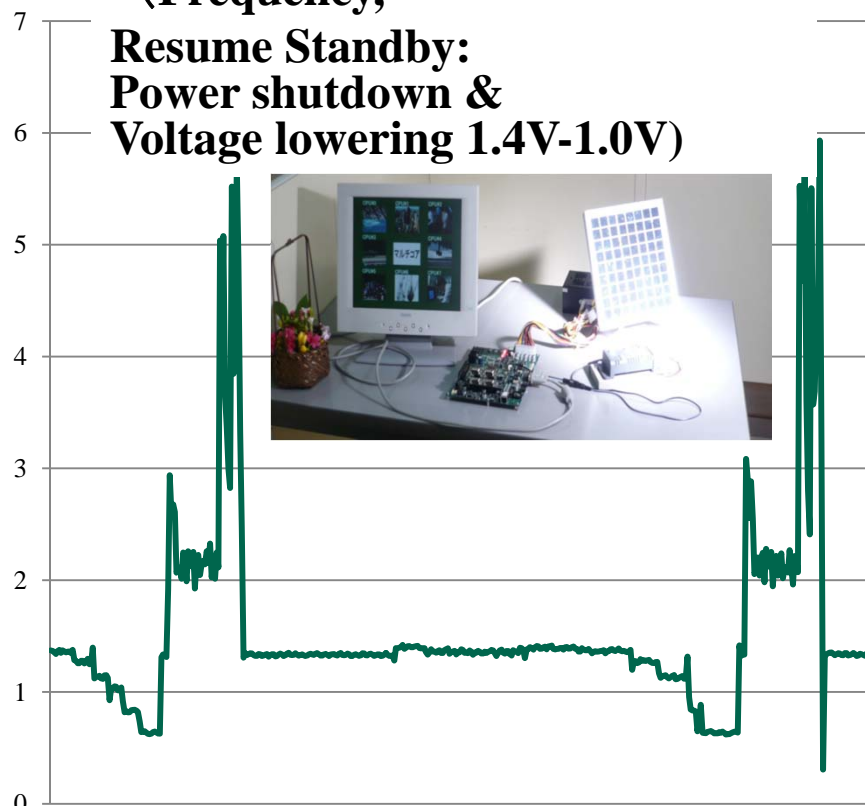
(Voltage : 1.4V)



Avg. Power
5.73 [W]

With Power Control
(Frequency,
Resume Standby:

Power shutdown &
Voltage lowering 1.4V-1.0V)



Avg. Power
1.52 [W]

73.5% Power Reduction





Future Multicore Products



Next Generation Automobiles

- Safer, more comfortable, energy efficient, environment friendly
- Cameras, radar, car2car communication, internet information integrated brake, steering, engine, motor control

Smart phones



- From everyday recharging to less than once a week
- Solar powered operation in emergency condition
- Keep health

Advanced medical systems



Cancer treatment, Drinkable inner camera

- Emergency solar powered
- No cooling fan, No dust, clean usable inside OP room



Personal / Regional Supercomputers



Solar powered with more than 100 times power efficient : FLOPS/W

- Regional Disaster Simulators saving lives from tornadoes, localized heavy rain, fires with earthquakes