

Green Computing Systems Research and Development with Industry

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IEEE Computer Society Board of Governors

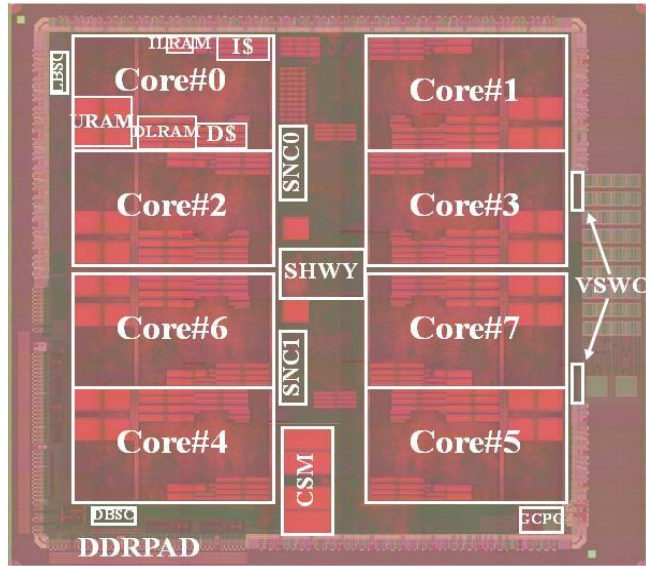
**IEEE Computer Society Multicore Strategic Technical
Committee (STC) Chair**

URL: <http://www.kasahara.cs.waseda.ac.jp/>

ITRI Waseda Forum, 2012.10.15(Monday), Waseda University

Multi/Many-core Everywhere

Multi-core from embedded to supercomputers



➤ Consumer Electronics (Embedded)

Mobile Phone, Game, TV, Car Navigation, Camera,

IBM/ Sony/ Toshiba Cell, Fujitsu FR1000,

Panasonic Uniphier, NEC/ARM MPCore/MP211/NaviEngine,

Renesas 4 core RP1, 8 core RP2, 15core Hetero RP-X,

Plurality HAL 64(Marvell), Tiler Tile64/ -Gx100(->1000cores),

DARPA UHPC (2017: 80GFLOPS/W)

➤ PCs, Servers

Intel Quad Xeon, Core 2 Quad, Montvale, Nehalem(8cores),

Larrabee(32cores), SCC(48cores), Night Corner(50 core+:22nm),

AMD Quad Core Opteron (8, 12 cores)

➤ WSs, Deskside & Highend Servers

IBM(Power4,5,6,7), Sun (SparcT1,T2), Fujitsu SPARC64fx8

➤ Supercomputers

Earth Simulator:**40TFLOPS**, 2002, 5120 vector proc.

BG/Q (A2:16cores) Water Cooled20PFLOPS, 3-4MW (2011-12),

BlueWaters(HPCS) Power7, 10 PFLOP+(2011.07),

Tianhe-1A (4.7PFLOPS,6coreX5670+ Nvidia Tesla M2050),

Godson-3B (1GHz40W 8core128GFLOPS) -T (64 core,192GFLOPS:2011)

RIKEN Fujitsu “K” 10PFLOPS(8core SPARC64VIIIifx, 128GGFLOPS)

High quality application software, Productivity, Cost performance, Low power consumption are important

Ex, Mobile phones, Games

Compiler cooperated multi-core processors are promising to realize the above futures

OSCAR Type Multi-core Chip by Renesas in METI/NEDO Multicore for Real-time Consumer Electronics Project (Leader: Prof.Kasahara)



The 37th (June 20,2011) &38th (Nov.14.2011) **Top 500 No.1**,
Riken Fujitsu “K” **705,024 cores**
Peak **11.28 PFLOPS**, (88,128procs)
LINPACK **10.510 PFLOPS** (93.2%)

Green Computing Systems R&D Center

Waseda University

Supported by METI (Mar. 2011 Completion)

<R & D Target>

Hardware, Software, Application
for Super Low-Power Manycore
Processors

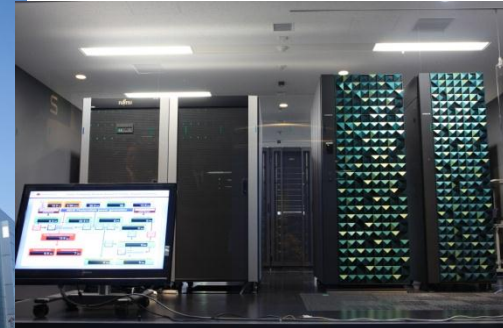
- More than 64 cores
- Natural air cooling (No fan)
Cool, Compact, Clear, Quiet
- Operational by Solar Panel

<Industry, Government, Academia>

Hitachi, Fujitsu, NEC, Renesas, Olympus,
Toyota, Denso, Mitsubishi, Toshiba, etc

<Ripple Effect>

- Low CO₂ (Carbon Dioxide) Emissions
- Creation Value Added Products
 - Consumer Electronics, Automobiles, Servers



Hitachi SR16000:

Power7 128coreSMP

Fujitsu M9000

SPARC VII 256 core SMP

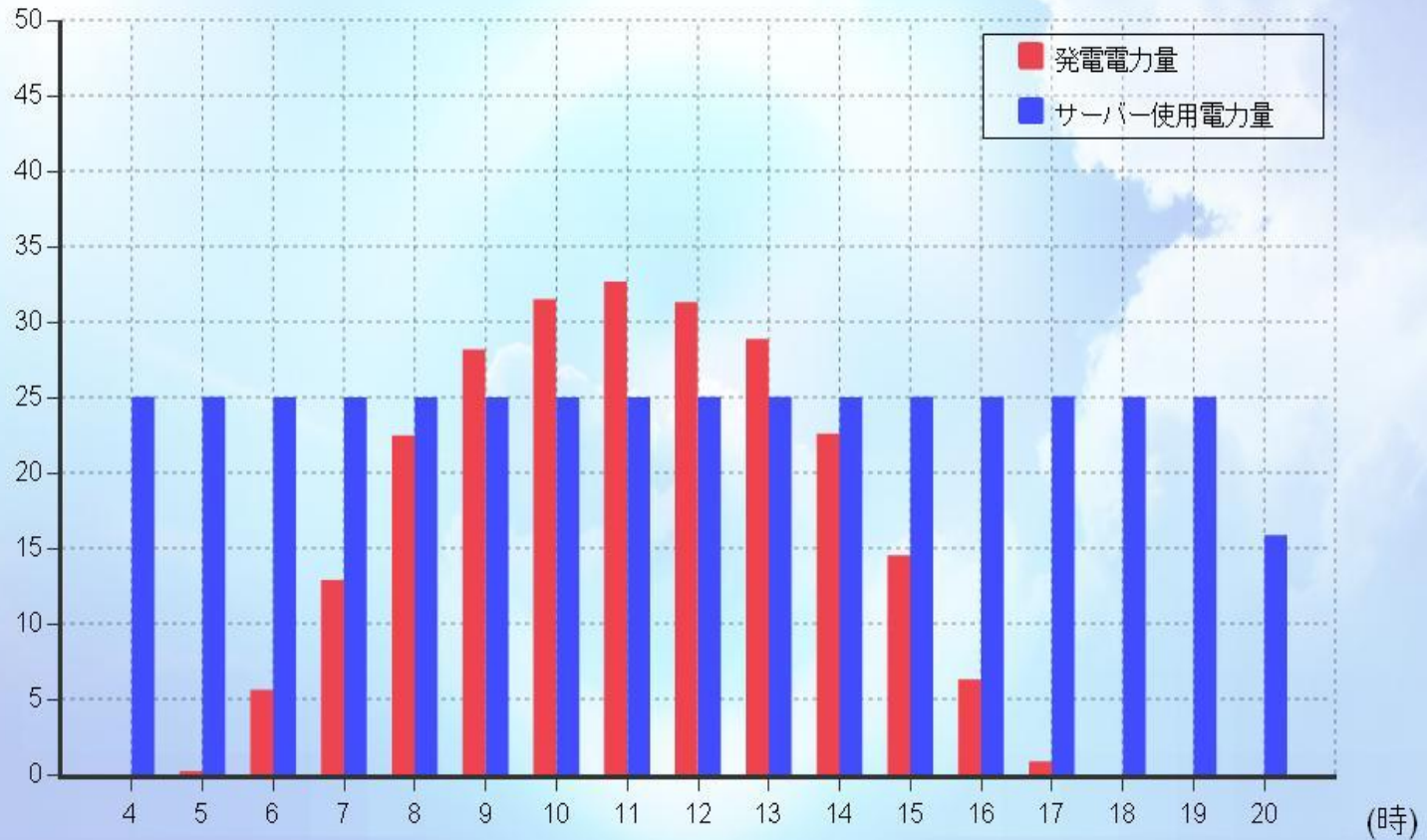


Beside Subway Waseda Station,
Near Waseda Univ. Main Campus

2012.4.2 (Clear) Power Generation and Server Consumption: One day Trends

電力量の1日の変化

電力量(kWh)



Super Low Power Web Server Using Embedded Multicore Processor RPX

1W with 8 SH4A processor cores



WASEDA UNIVERSITY Computer Science and Engineering
Kasahara Laboratory

Power consumption



0.96 W

[Japanese | English]

Private Page

by RPX embedded multicore Web-server.



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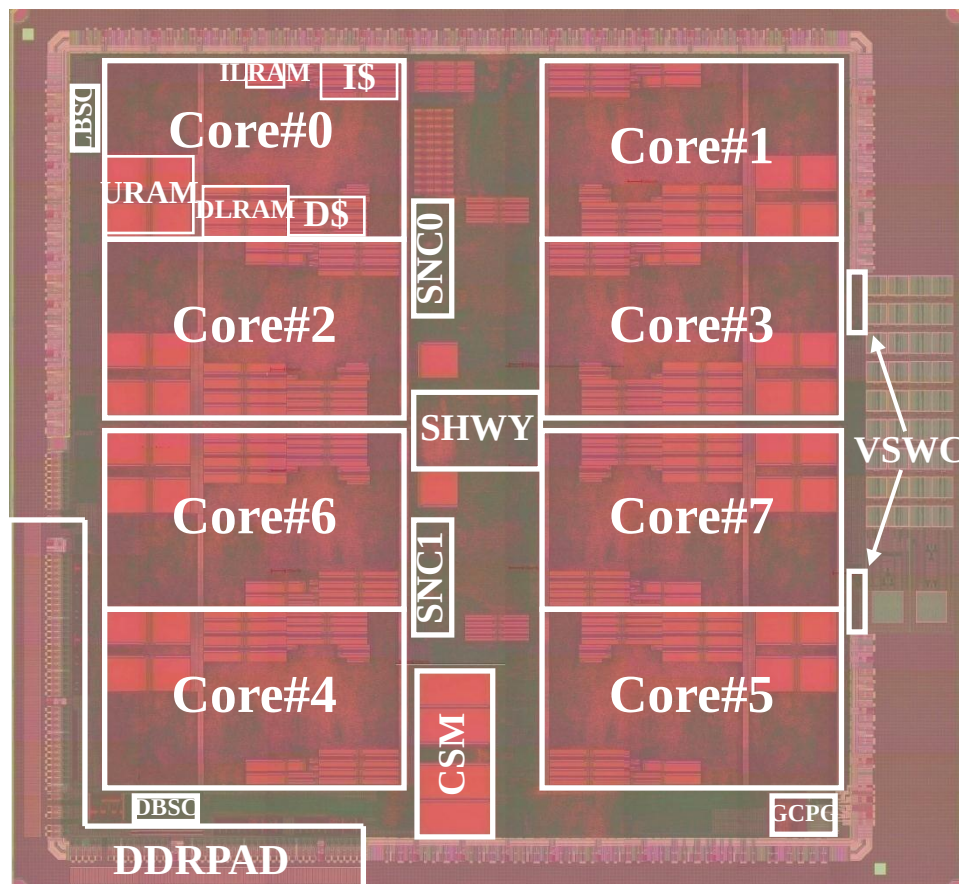
- ▶ Professor Kasahara
- ▶ Associate Professor
- ▶ Publications
- ▶ Members

News

- ▶ 2012.4.25 OSCAR API 2.0 has been released
- ▶ 2012.4.2 Low power embedded multicore RPX server started Kasahara & Kimura Laboratory's web service and power consumption indication.
- ▶ 2011.10.07 Prof. Hironori Kasahara has been elected to the IEEE Computer Society Board of Governors(2012-2014). Thank you very much for your kind supports.
- ▶ 2011.09.06 Information for the 25th Anniversary Workshop LCPC2012 (International Workshop on Languages and Compilers for Parallel Computing) Sep. 11-13, 2012 was upped.

Renesas-Hitachi-Waseda Low Power 8 core RP2

Developed in 2007 in METI/NEDO project



Process Technology	90nm, 8-layer, triple-Vth, CMOS
Chip Size	104.8mm ² (10.61mm x 9.88mm)
CPU Core Size	6.6mm ² (3.36mm x 1.96mm)
Supply Voltage	1.0V–1.4V (internal), 1.8/3.3V (I/O)
Power Domains	17 (8 CPUs, 8 URAMs, common)

IEEE ISSCC08: Paper No. 4.5, M.ITO, ... and H. Kasahara, “An 8640 MIPS SoC with Independent Power-off Control of 8 CPUs and 8 RAMs by an Automatic Parallelizing Compiler”

Demo of NEDO Multicore for Real Time Consumer Electronics at the Council of Science and Engineering Policy on April 10, 2008

第74回総合科学技術会議【平成20年4月10日】



第74回総合科学技術会議の様子(1)



第74回総合科学技術会議の様子(2)



第74回総合科学技術会議の様子(3)



第74回総合科学技術会議の様子(4)

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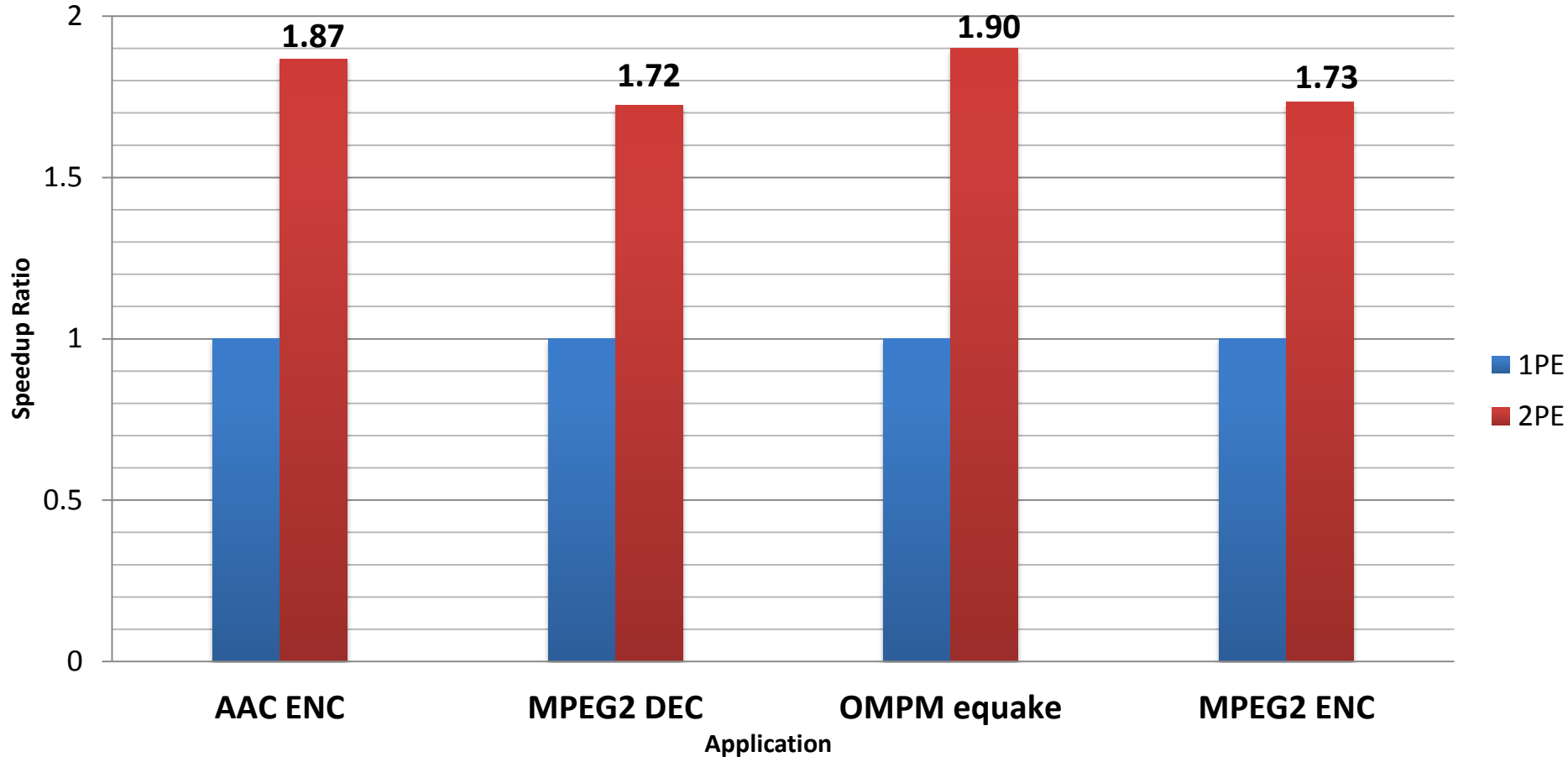
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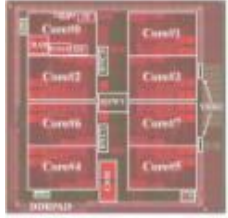
Performance of OSCAR Compiler & API on 2 ARMv7-cores Qualcomm MSM8960 (Snapdragon) Android 4.0 for Smart Phones



1.81 times speedup by 2 cores on the average against 1 core

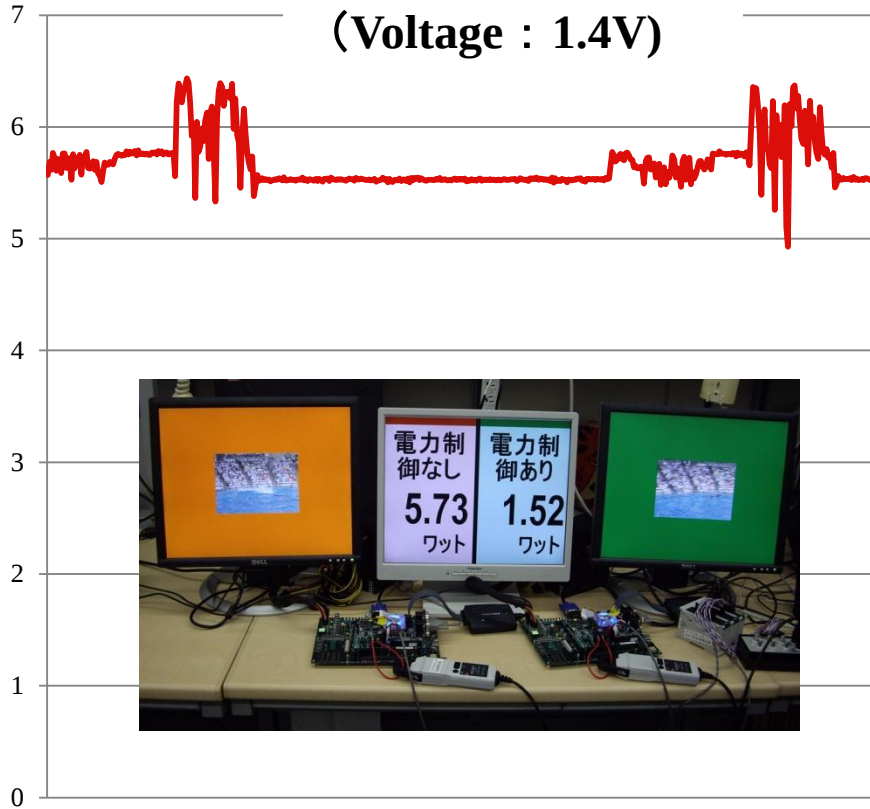
Power Reduction of MPEG2 Decoding to 1/4 on 8 Core Homogeneous Multicore RP-2 by OSCAR Parallelizing Compiler

MPEG2 Decoding with 8 CPU cores



Without Power
Control

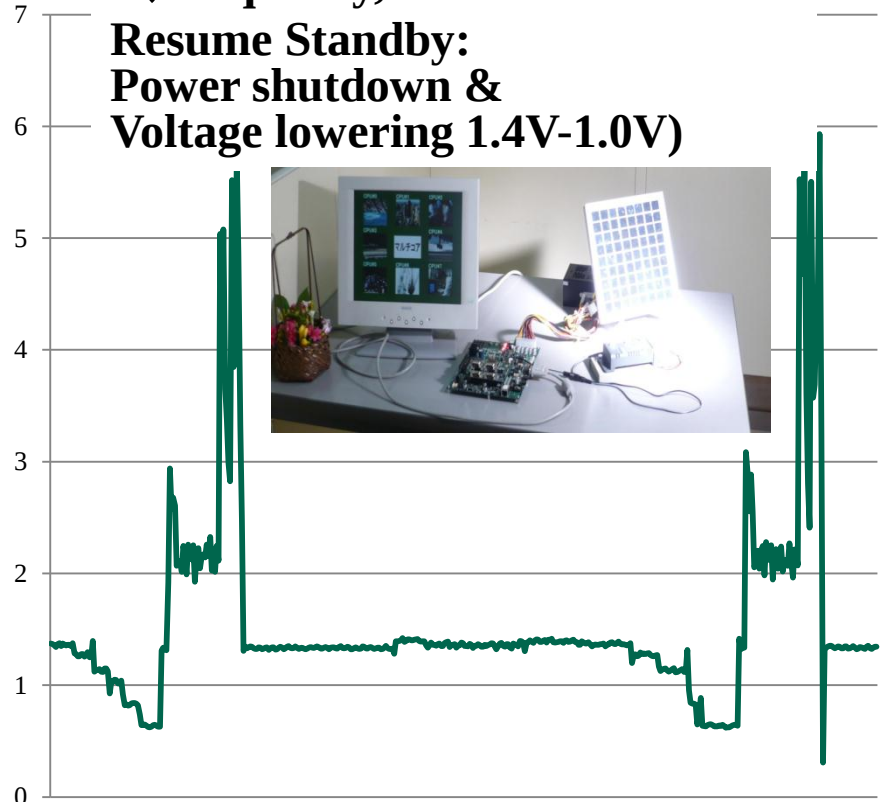
(Voltage : 1.4V)



Avg. Power
5.73 [W]

With Power Control
(Frequency,

Resume Standby:
Power shutdown &
Voltage lowering 1.4V-1.0V)

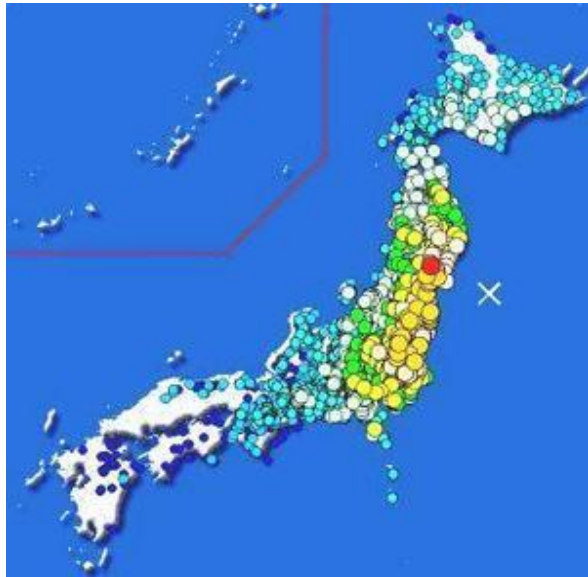
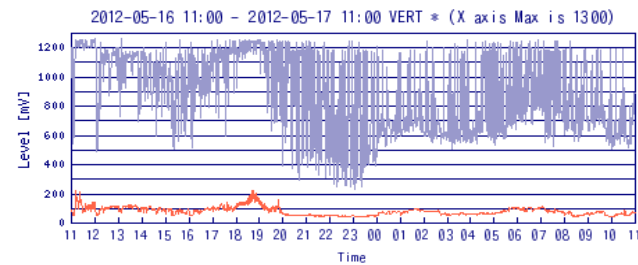


Avg. Power
1.52 [W]

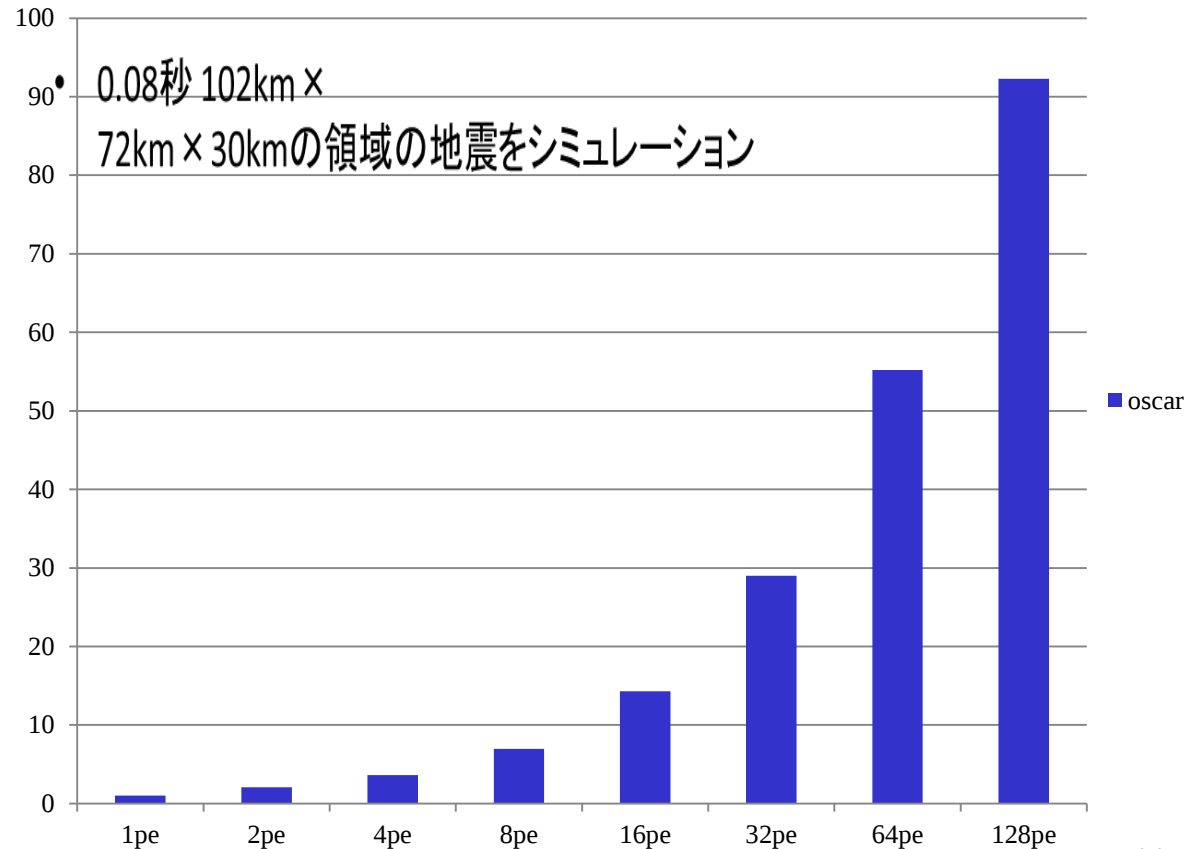
73.5% Power Reduction



92 Times Speedup against the Sequential Processing for GMS Earthquake Wave Propagation Simulation on Hitachi SR16000 (Power7 Based 128 Core Linux SMP)

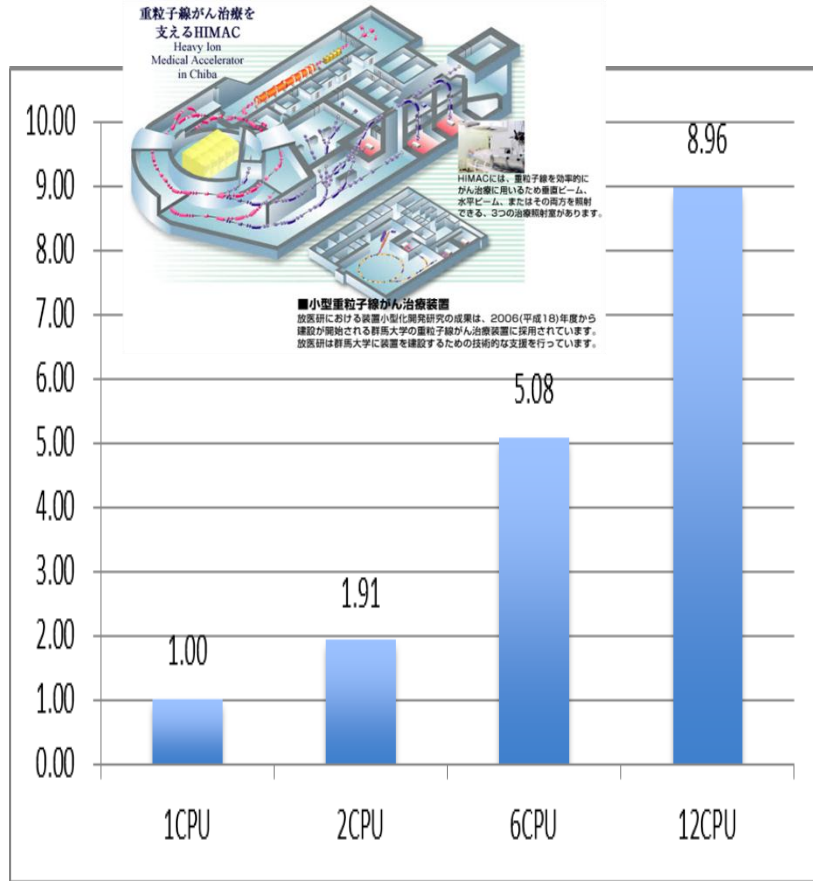


Speedup against sequential processing



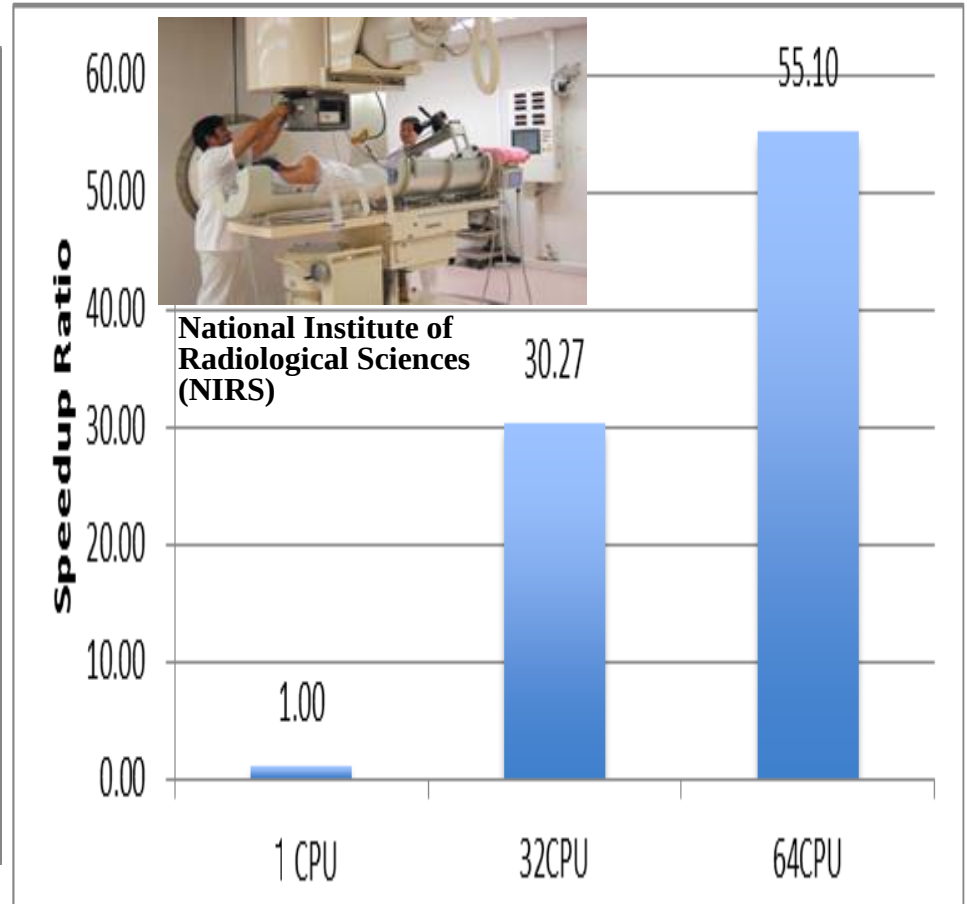
Cancer Treatment Carbon Ion Radiotherapy

(Previous best was 2.5 times speedup on 16 processors with hand optimization)



8.9times speedup by 12 processors

Intel Xeon X5670 2.93GHz 12 core SMP (Hitachi HA8000)



55 times speedup by 64 processors

IBM Power 7 64 core SMP (Hitachi SR16000)