Future of Low Energy Computing Systems

--- Low Power Multi-core and Many-core processors and Their Software ---

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IEEE Computer Society Board of Governor

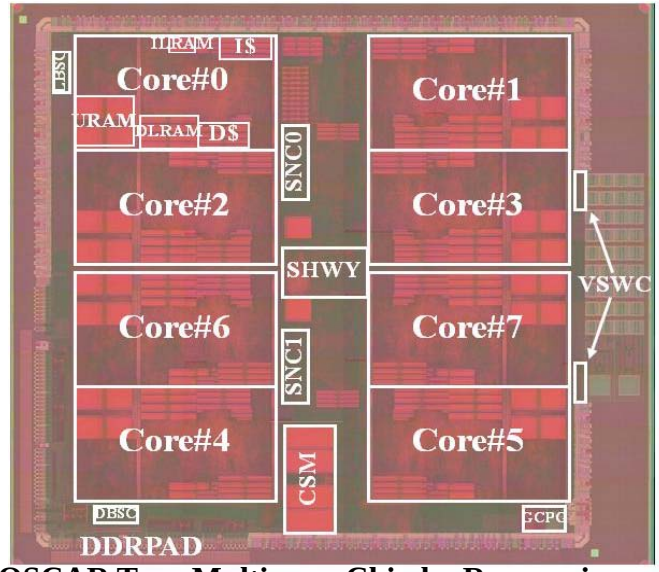
http://www.kasahara.cs.waseda.ac.jp

IEEE 125 Anniversary Memorial Seminar

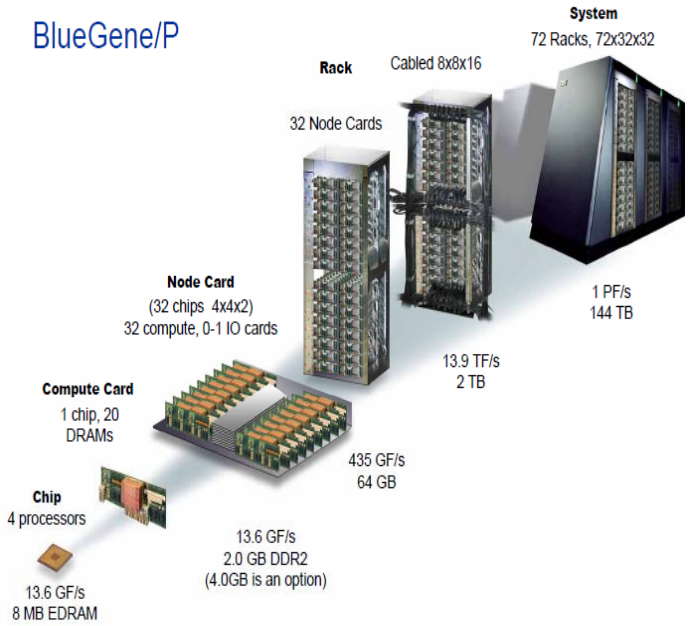
Future of Information & Telecommunications Technologies

15:15-15:45, 2009.10.16 @ Waseda University

Multi-core Everywhere



OSCAR Type Multi-core Chip by Renesas in METI/NEDO Multicore for Real-time Consumer Electronics Project (Leader: Prof.Kasahara)



Multi-core from embedded to supercomputers

- **Consumer Electronics (Embedded)**
  - Mobile Phone, Game, Digital TV, Car Navigation, DVD, Camera,
  - IBM/ Sony/ Toshiba Cell, Fuijtsu FR1000,
  - NEC/ARMMPCore&MP211, Panasonic Uniphier,
  - Renesas SH multi-core(4 core RP1, 8 core RP2)
  - Tilera Tile64, SPI Storm-1(16 VLIW cores)
- **PCs, Servers**
  - Intel Quad Xeon, Core 2 Quad, Montvale, Nehalem(8core), 80 core, Larrabee(32core)
  - AMD Quad Core Opteron, Phenom
- **WSs, Deskside & Highend Servers**
  - IBM Power4,5,5+,6 Sun Niagara(SparcT1,T2), Rock
- **Supercomputers**
  - Earth Simulator:40TFLOPS, 2002, 5120 vector proc.
  - IBM Blue Gene/L: 360TFLOPS, 2005, Low power CMP d 128K processor chips, BG/Q :20PFLOPS.2011, BlueWaters: Effective 1PFLOPS, Julty2011,NCSA UIUC

High quality application software, Productivity, Cost performance, Low power consumption are important

Ex, Mobile phones, Games

Compiler cooperated multi-core processors are promising to realize the above futures

METI/NEDO National Project

Multi-core for Real-time Consumer Electronics

<Goal> R&D of compiler cooperative multi-core processor technology for consumer electronics like Mobile phones, Games, DVD, Digital TV, Car navigation systems.

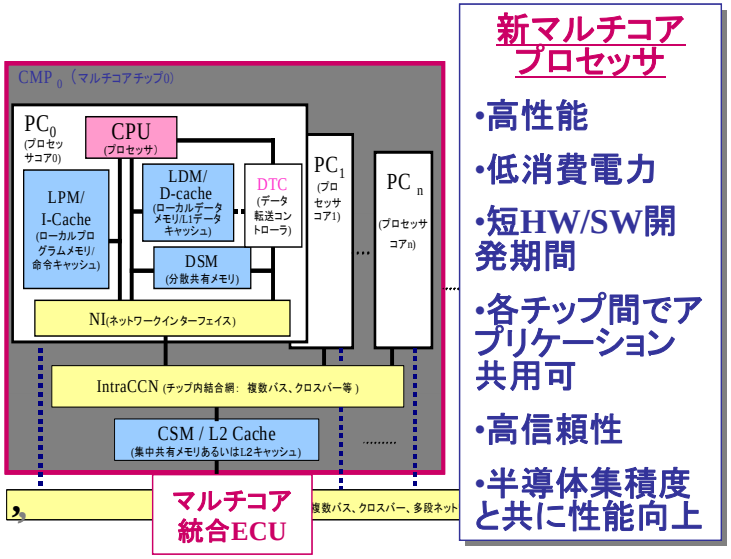
<Period> From July 2005 to March 2008

<Features>

- Good cost performance
- Short hardware and software development periods
- Low power consumption
- Scalable performance improvement with the advancement of semiconductor
- Use of the same parallelizing compiler for multi-cores from different vendors using newly developed API

API : Application Programming Interface

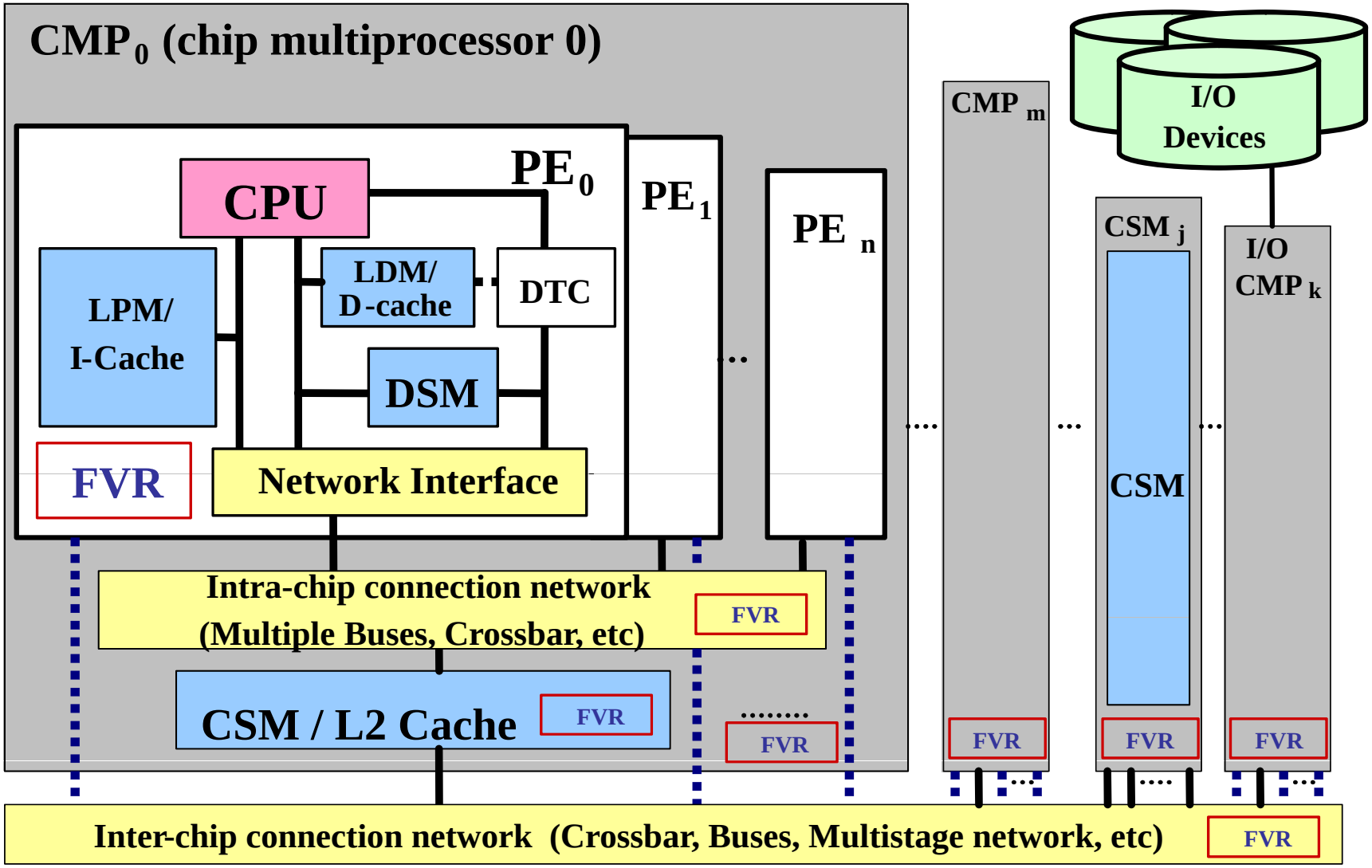
(2005.7～2008.3)**



開発マルチコアチップは情報家電へ

**Hitachi, Renesas, Fujitsu, Toshiba, Panasonic, NEC

OSCAR Multi-Core Architecture



CSM: central shared mem.

DSM: distributed shared mem.

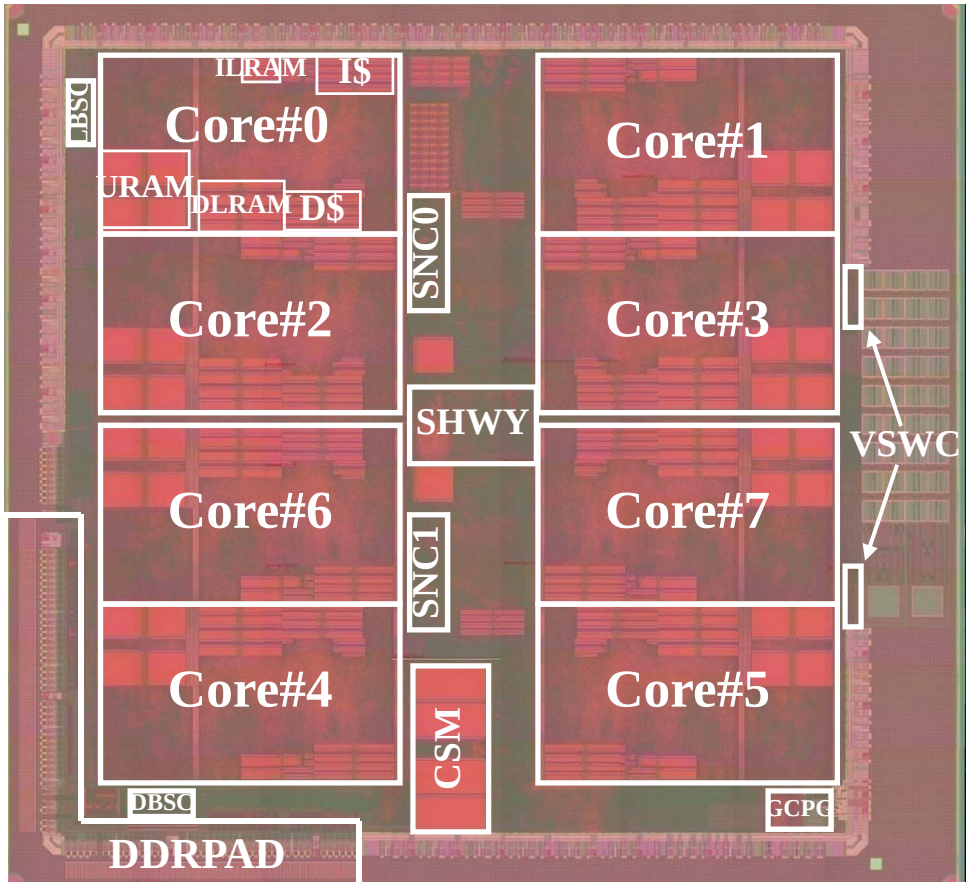
DTC: Data Transfer Controller

LDM : local data mem.

LPM : local program mem.

FVR: frequency / voltage control register

Renesas-Hitachi-Waseda 8 core RP2 Chip Photo and Specifications



Process Technology	90nm, 8-layer, triple-Vth, CMOS
Chip Size	104.8mm^2 (10.61mm x 9.88mm)
CPU Core Size	6.6mm^2 (3.36mm x 1.96mm)
Supply Voltage	1.0V–1.4V (internal), 1.8/3.3V (I/O)
Power Domains	17 (8 CPUs, 8 URAMs, common)

IEEE ISSCC08: Paper No. 4.5, M.ITO, … and H. Kasahara, "An 8640 MIPS SoC with Independent Power-off Control of 8 CPUs and 8 RAMs by an Automatic Parallelizing Compiler"

Demo of NEDO Multicore for Real Time Consumer Electronics at the Council of Science and Engineering Policy on April 10, 2008

第74回総合科学技術会議【平成20年4月10日】


第74回総合科学技術会議の様子(1)


第74回総合科学技術会議の様子(2)


第74回総合科学技術会議の様子(3)


第74回総合科学技術会議の様子(4)

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OSCAR Parallelizing Compiler

To improve effective performance, cost-performance and software productivity and reduce power

Multigrain Parallelization

coarse-grain parallelism among loops and subroutines, near fine grain parallelism among statements in addition to loop parallelism

Data Localization

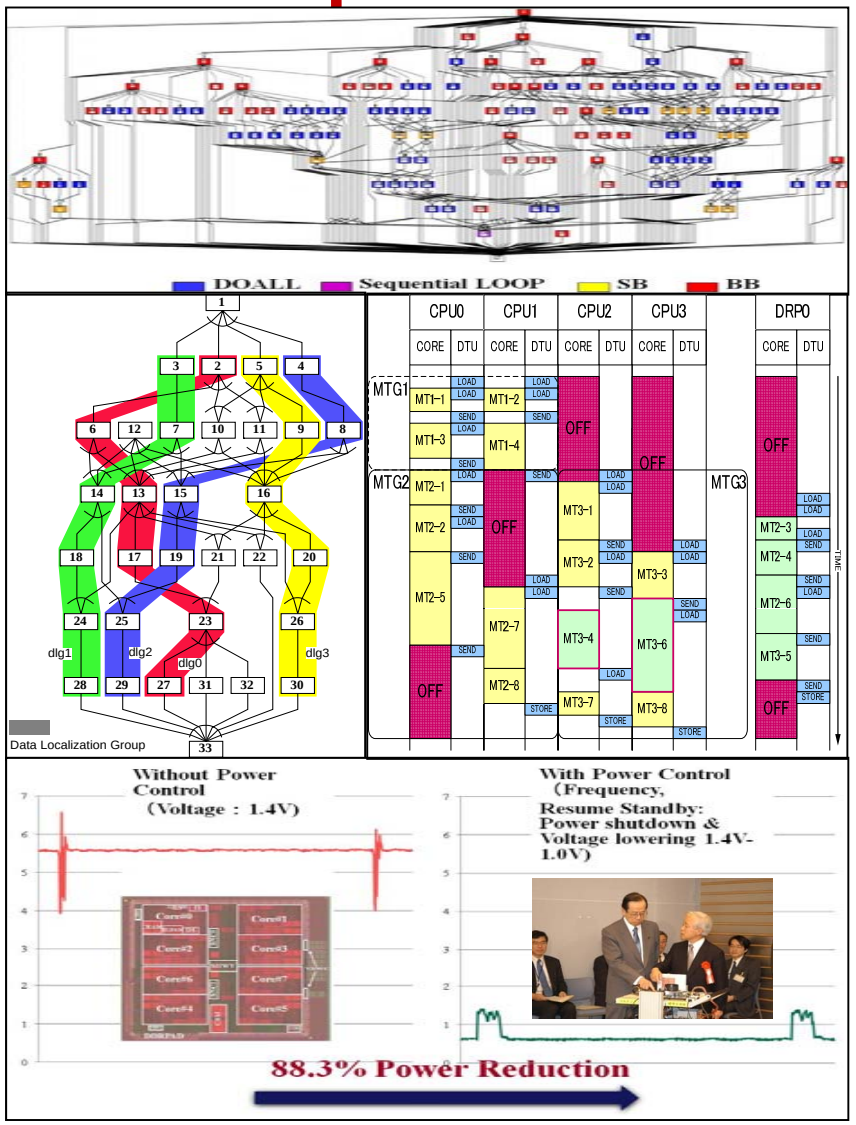
Automatic data management for distributed shared memory, cache and local memory

Data Transfer Overlapping

Data transfer overlapping using Data Transfer Controllers (DMAs)

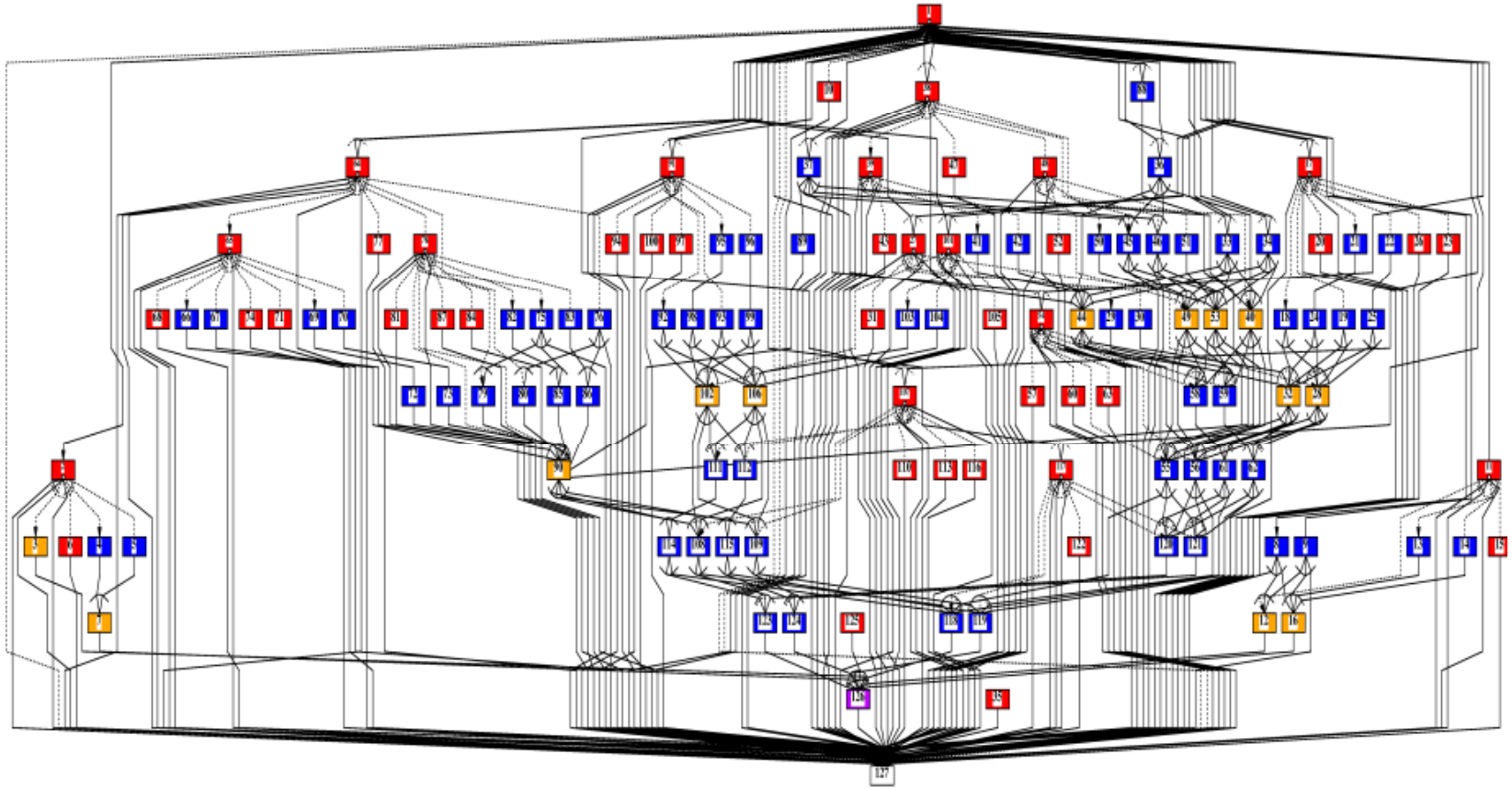
Power Reduction

Reduction of consumed power by compiler control DVFS and Power gating with hardware supports.



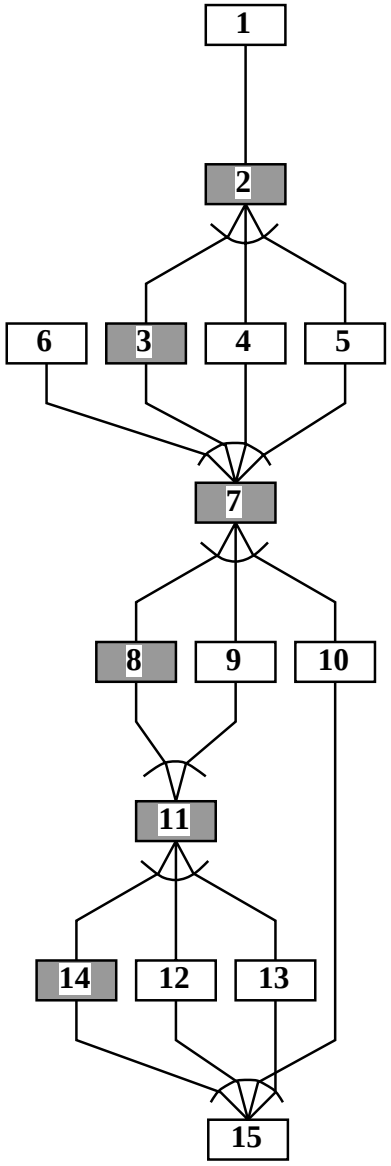
MTG of Su2cor-LOOPS-DO400

- **Coarse grain parallelism PARA_ALD = 4.3**

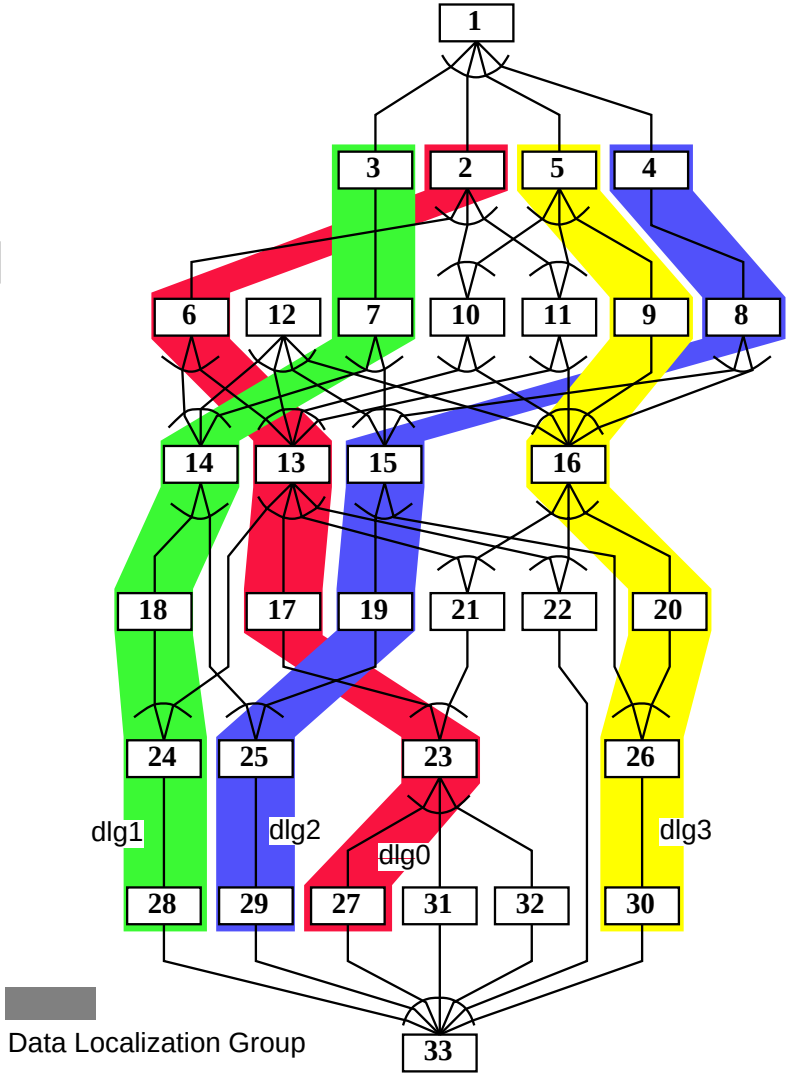


DOALL **Sequential LOOP** **SB** **BB**

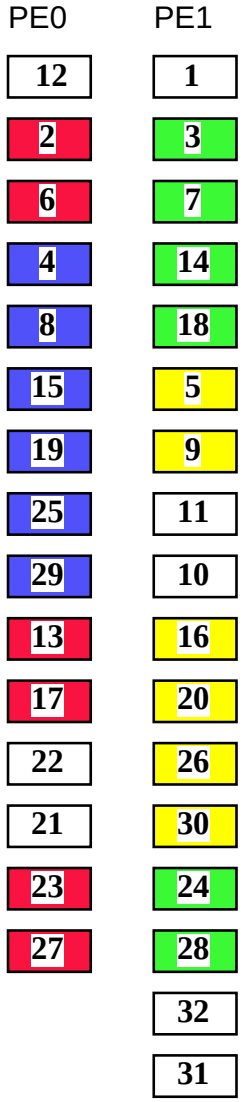
Data Localization



MTG

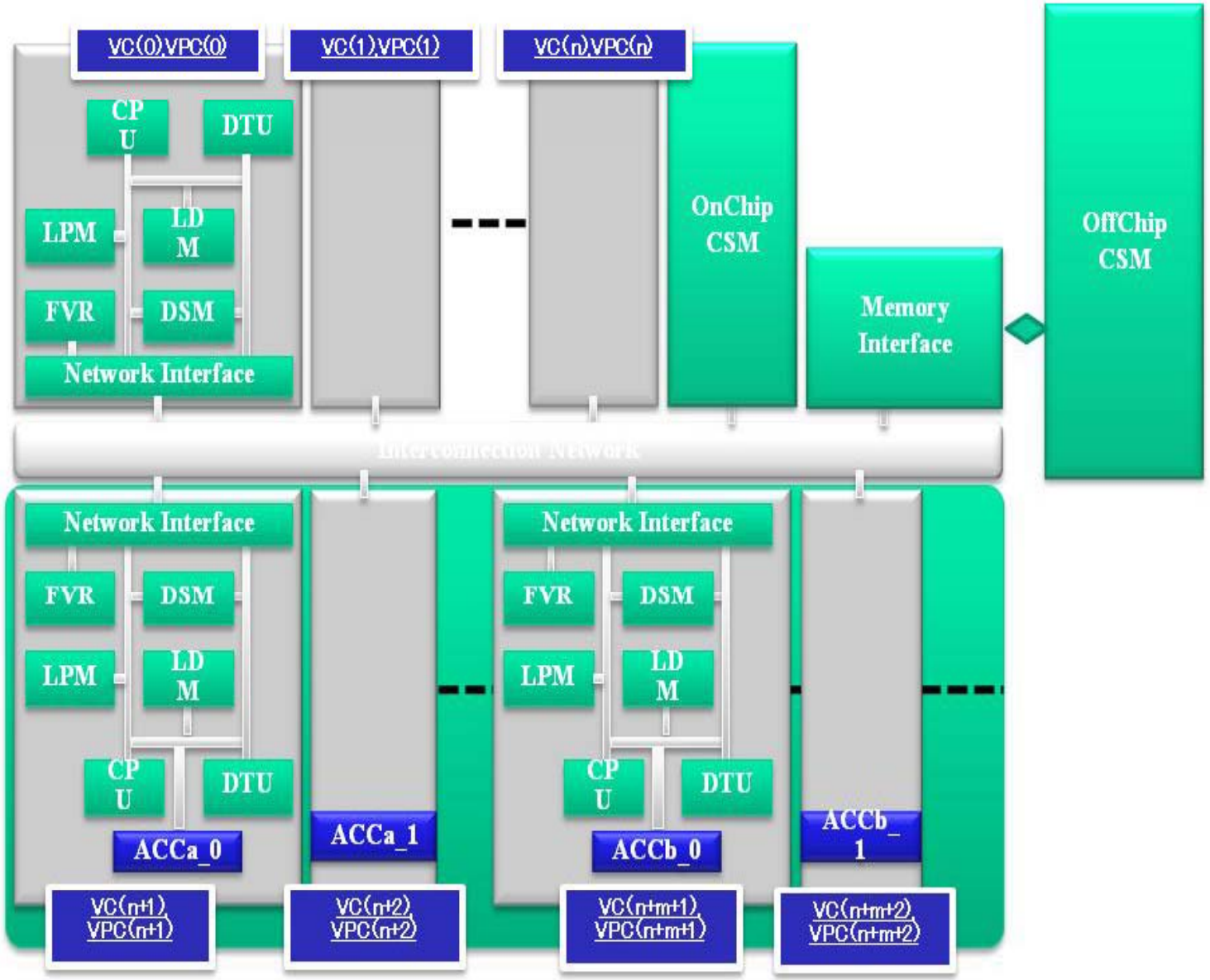


MTG after Division



A schedule for two processors

OSCAR Heterogeneous Multicore



DTU
- Data Transfer Unit

LPM
- Local Program Memory

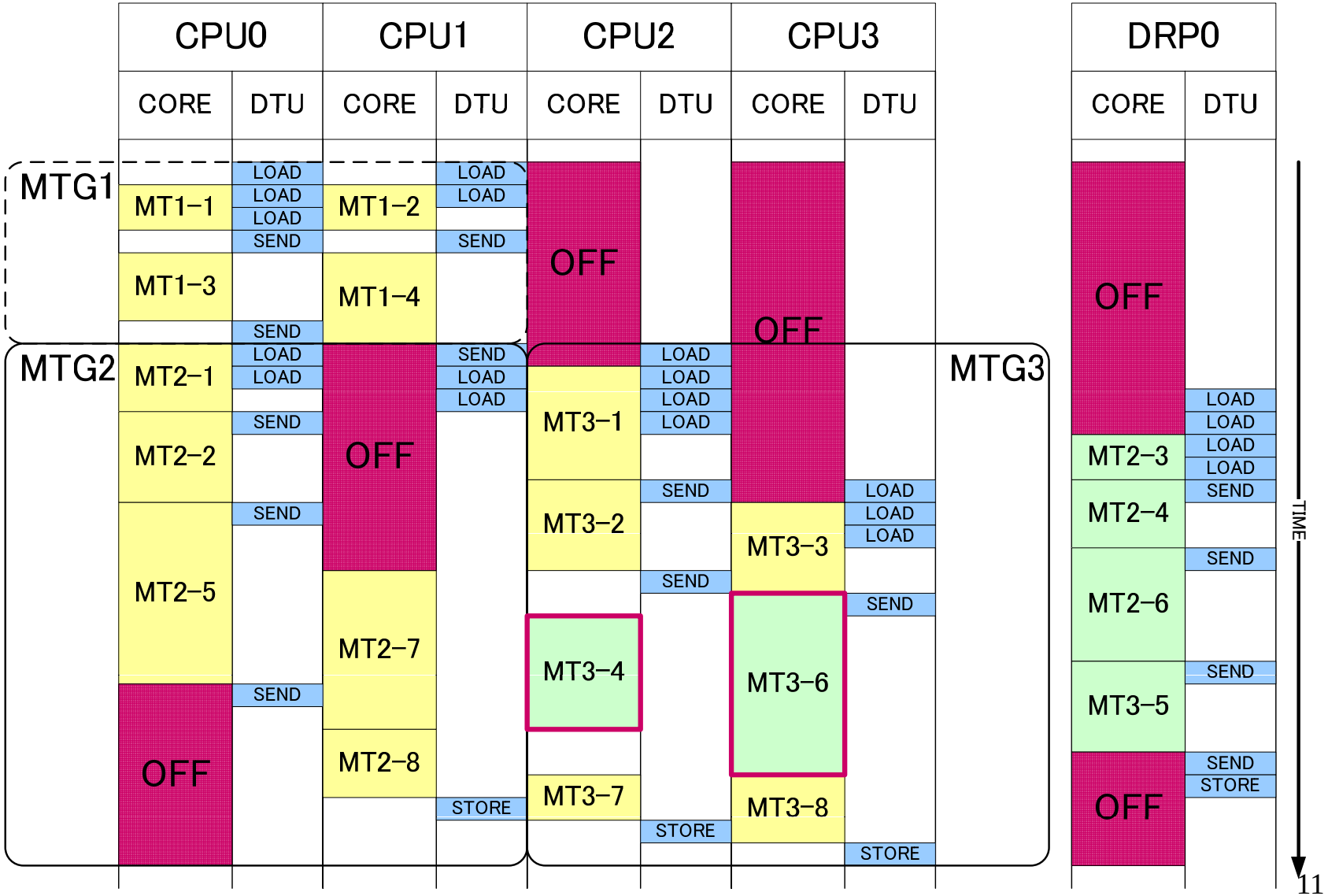
LDM
- Local Data Memory

DSM
- Distributed Shared Memory

CSM
- Centralized Shared Memory

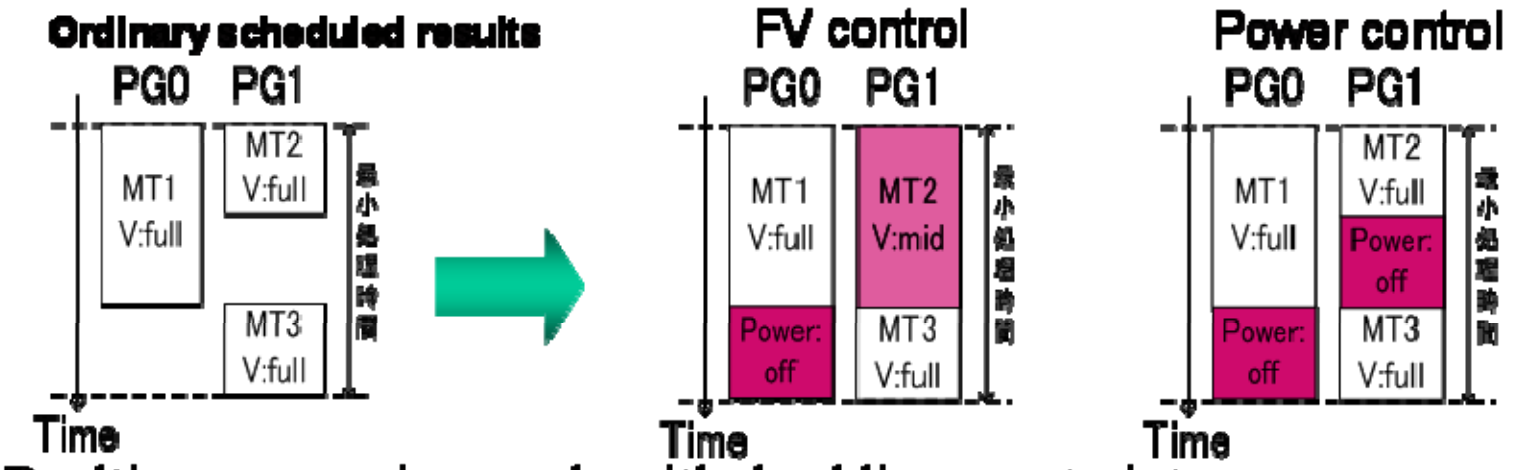
FVR
- Frequency/Voltage Control Register

An Image of Static Schedule for Heterogeneous Multi-core with Data Transfer Overlapping and Power Control



Power Reduction by Power Supply, Clock Frequency and Voltage Control by OSCAR Compiler

- Shortest execution time mode



- Realtime processing mode with dead line constraints

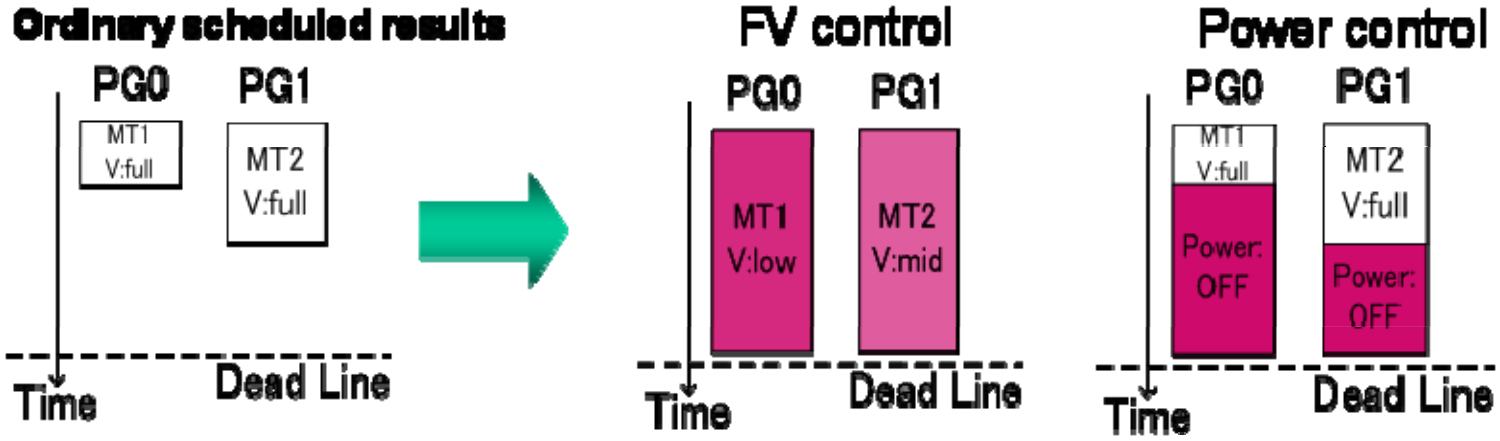
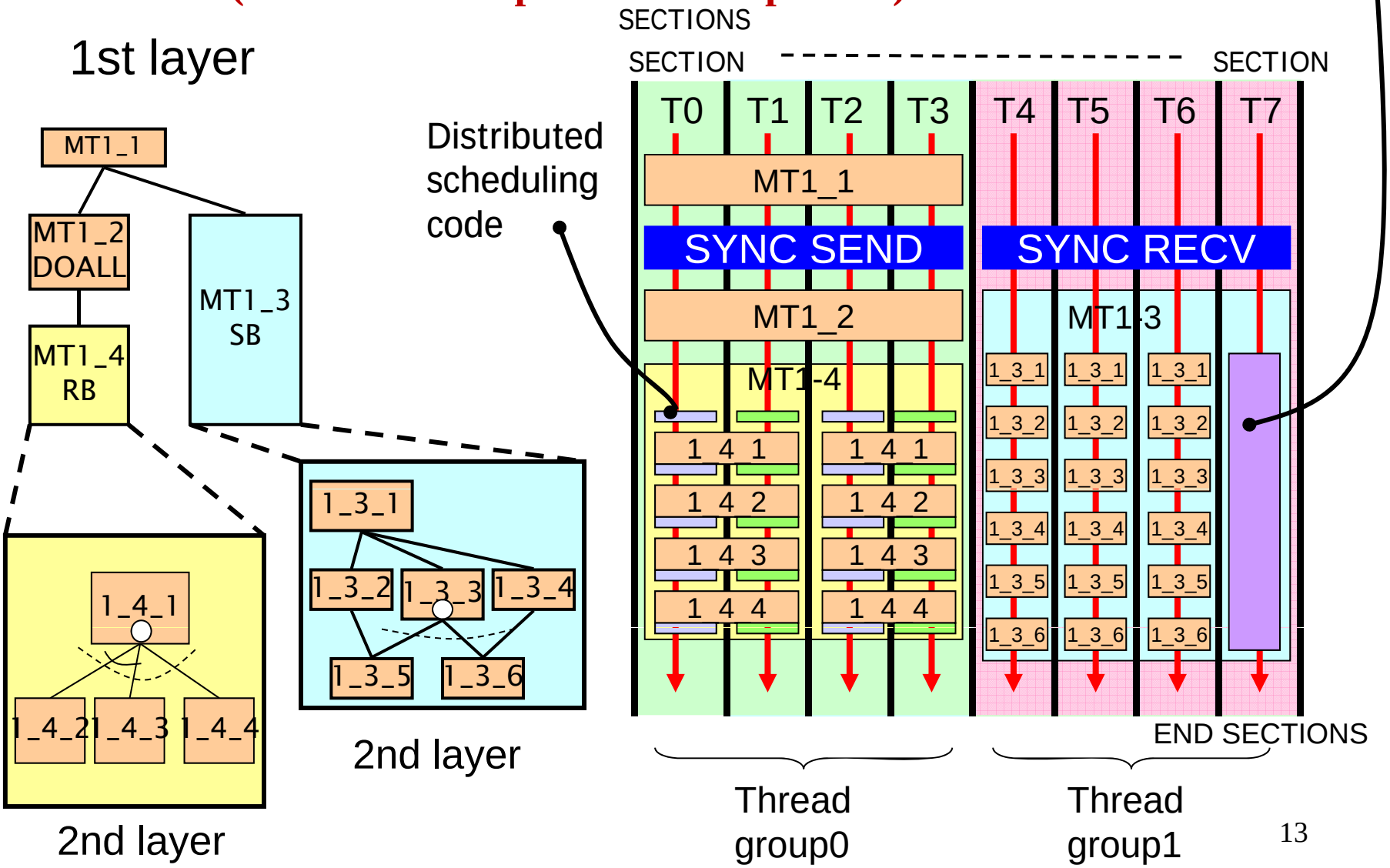


Image of Generated Multigrain Parallelized Code using the developed Multicore API

(The API is compatible with OpenMP)



Compilation Flow Using OSCAR API

Application Program
Fortran or Parallelizable C
(Sequential program)

Waseda Univ. OSCAR Parallelizing Compiler

- Coarse grain task parallelization
- Global data Localization
- Data transfer overlapping using DMA
- Power reduction control using DVFS, Clock and Power gating

OSCAR API for Real-time Low Power High Performance Multicores

Directives for thread generation, memory, data transfer using DMA, power managements

Generation of parallel machine codes using sequential compilers

Parallelized Fortran or C program with APIl

Proc0
Code with directives
Thread 0

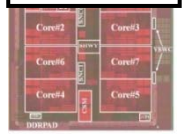
Proc1
Code with directives
Thread 1

Backend compiler
API Analyzer
Existing sequential compiler

Backend compiler
API Analyzer
Existing sequential compiler

Backend compiler
OpenMP Compiler

Machine codes



Multicore from Vendor A

Machine codes

Multicore from Vendor B

Shred memory servers

Executable on various multicores

Hitachi, Renesas, Fujitsu, Toshiba, Panasonic, NEC

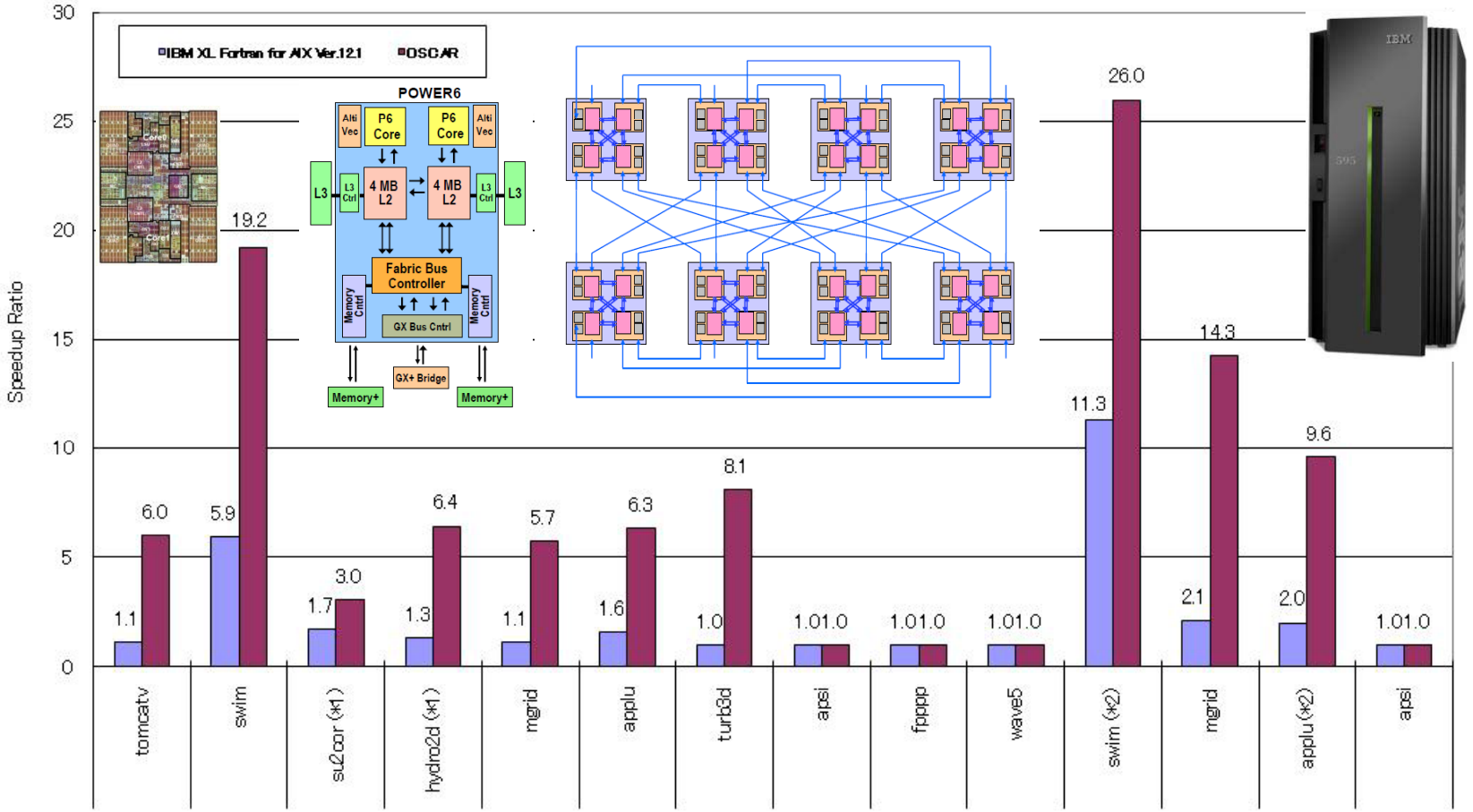
OSCAR: Optimally Scheduled Advanced Multiprocessor
API : Application Program Interface

OSCAR API

Now Open! (http://www.kasahara.cs.waseda.ac.jp/)

- **Targeting mainly realtime consumer electronics devices**
  - **embedded computing**
  - **various kinds of memory architecture**
    - **SMP, local memory, distributed shared memory, ...**
- **Developed with Japanese 6 companies**
  - **Fujitsu, Hitachi, NEC, Toshiba, Panasonic, Renesas**
  - **Supported by METI/NEDO**
- **Based on the subset of OpenMP**
  - **very popular parallel processing API**
  - **shared memory programming model**
- **Six Categories**
  - **Parallel Execution (4 directives from OpenMP)**
  - **Memory Mapping (Distributed Shared Memory, Local Memory)**
  - **Data Transfer Overlapping Using DMA Controller**
  - **Power Control (DVFS, Clock Gating, Power Gating)**
  - **Timer for Real Time Control**
  - **Synchronization (Hierarchical Barrier Synchronization)**

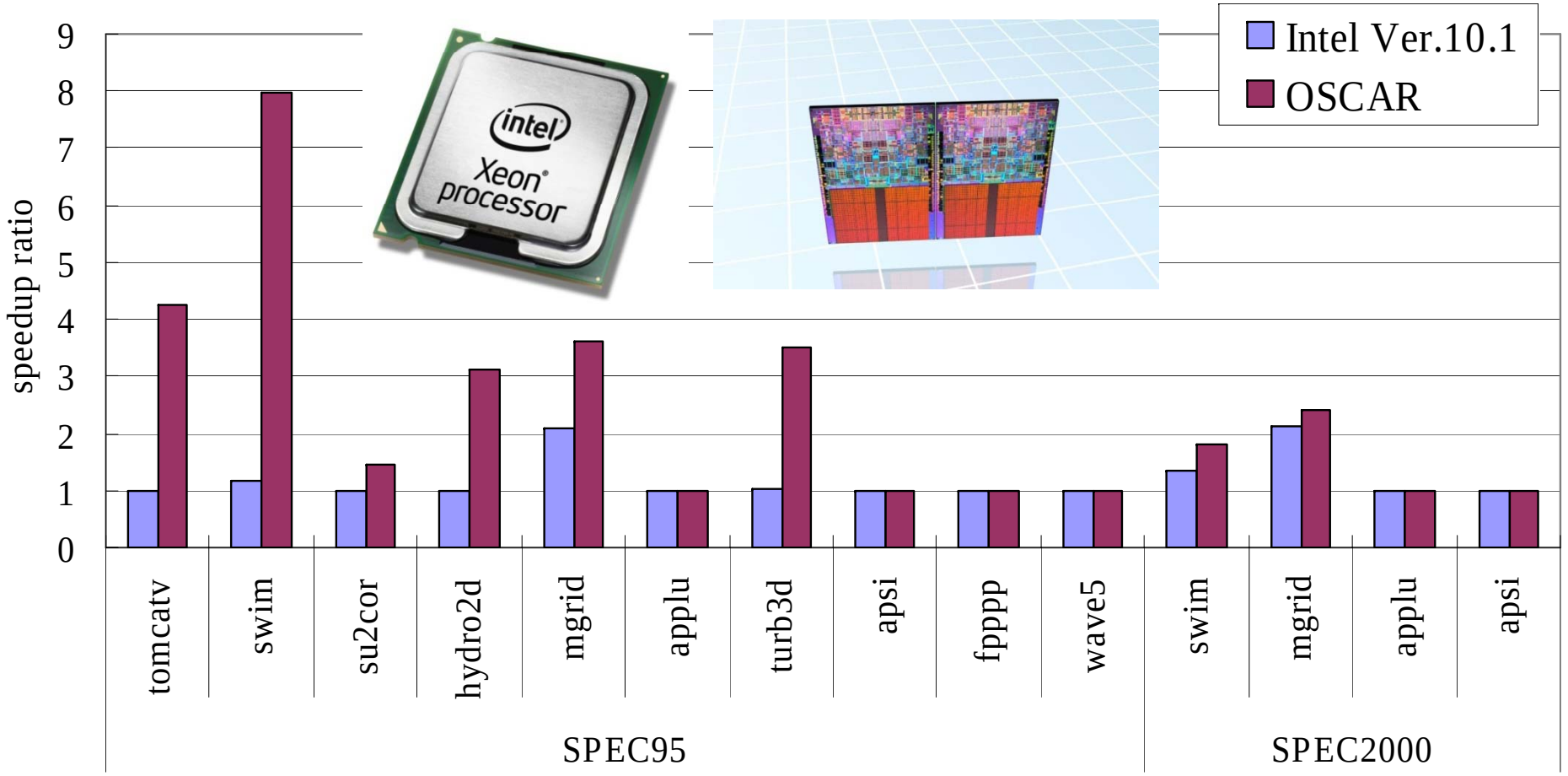
Performance of OSCAR Compiler on IBM p6 595 Power6 (4.2GHz) based 32-core SMP Server



OpenMP codes generated by OSCAR compiler accelerate IBM XL Fortran for AIX Ver.12.1 about 3.3 times on the average

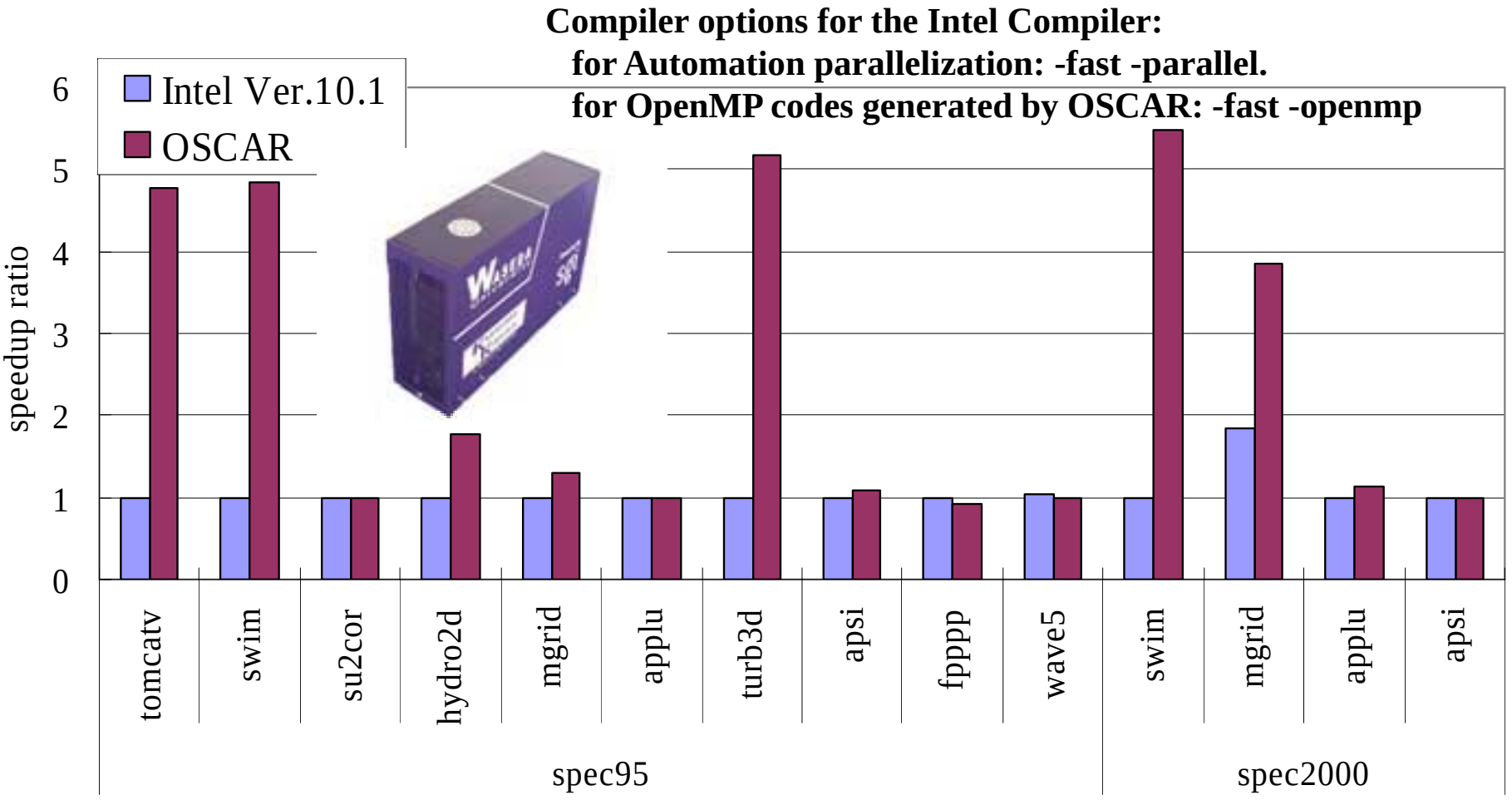
Compile Option:
(*1) Sequential: -O3 –qarch=pwr6, XLF: -O3 –qarch=pwr6 –qsmp=auto, OSCAR: -O3 –qarch=pwr6 –qsmp=noauto
(*2) Sequential: -O5 -q64 –qarch=pwr6, XLF: -O5 –q64 –qarch=pwr6 –qsmp=auto, OSCAR: -O5 –q64 –qarch=pwr6 –qsmp=noauto
(Others) Sequential: -O5 –qarch=pwr6, XLF: -O5 –qarch=pwr6 –qsmp=auto, OSCAR: -O5 –qarch=pwr6 –qsmp=noauto

Performance of OSCAR Compiler Using the Multicore API on Intel Quad-core Xeon



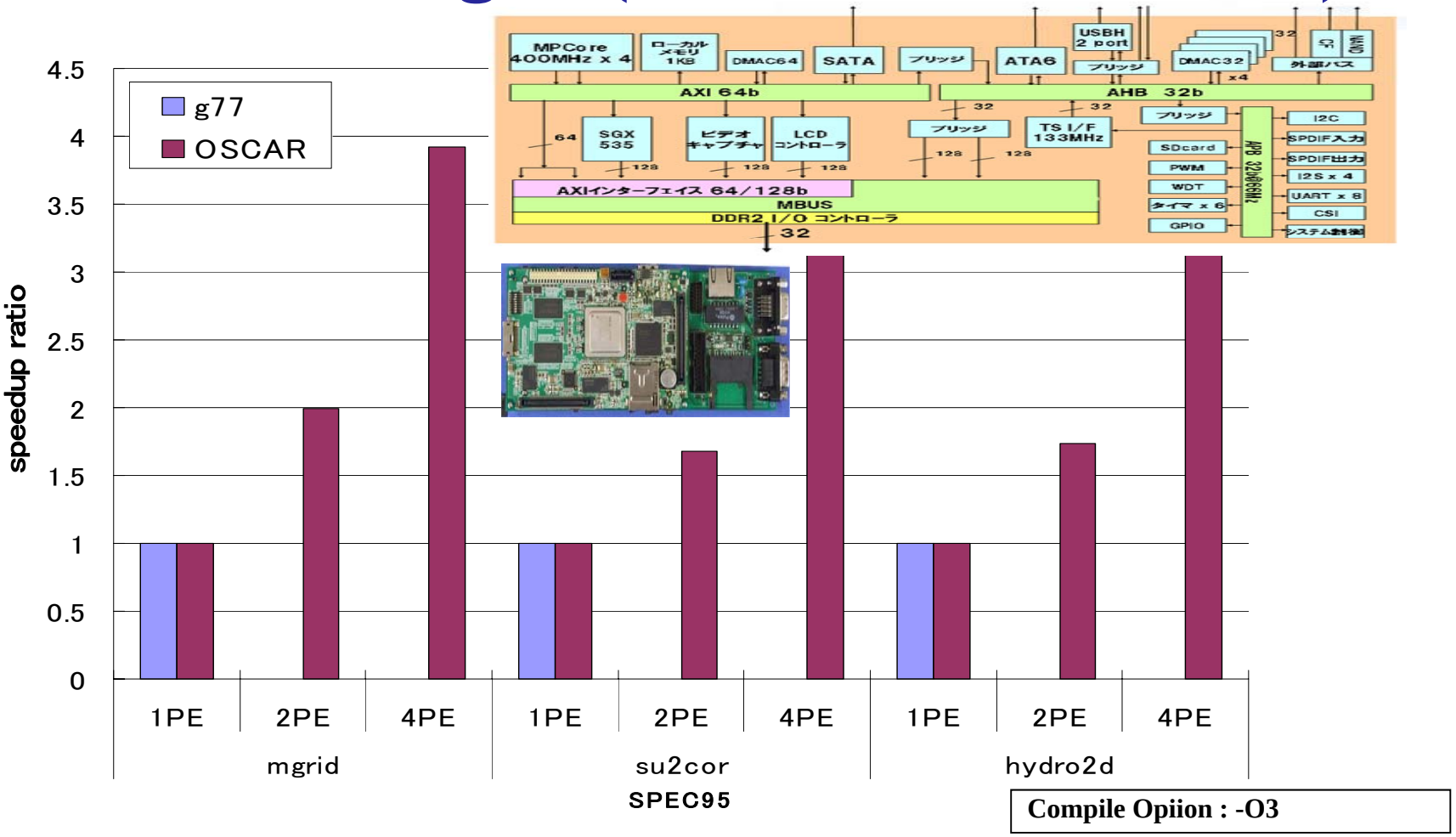
- **OSCAR Compiler gives us 2.1 times speedup on the average against Intel Compiler ver.10.1**

Performance of OSCAR compiler on 16 cores SGI Altix 450 Montvale server



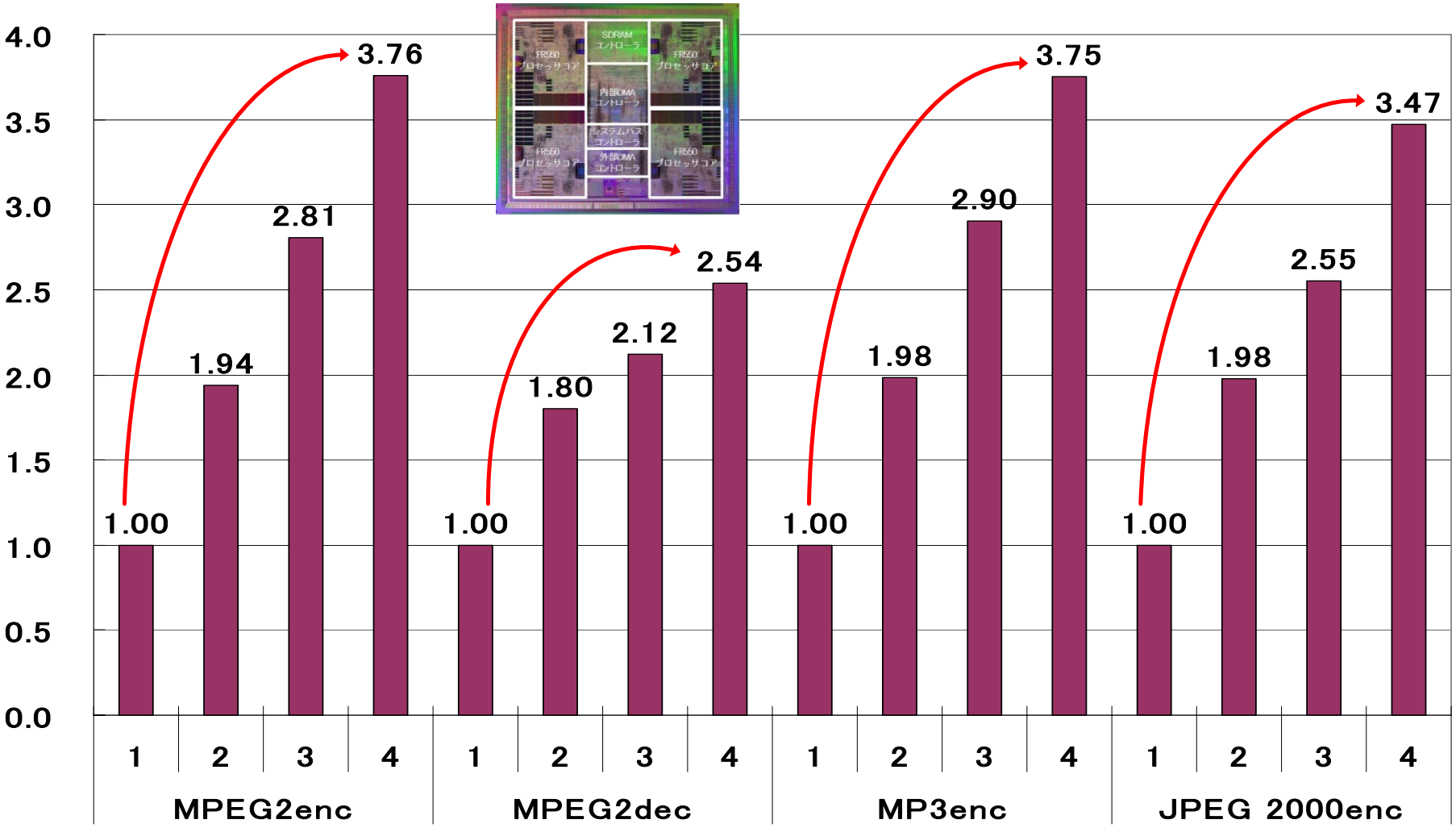
- **OSCAR compiler gave us 2.3 times speedup against Intel Fortran Itanium Compiler revision 10.1**

Performance of OSCAR compiler on NEC NaviEngine(ARM-NEC MPcore)



- **OSCAR compiler gave us 3.43 times speedup against 1 core on ARM/NEC MPCore with 4 ARM 400MHz cores**

Performance of OSCAR Compiler Using the multicore API on Fujitsu FR1000 Multicore

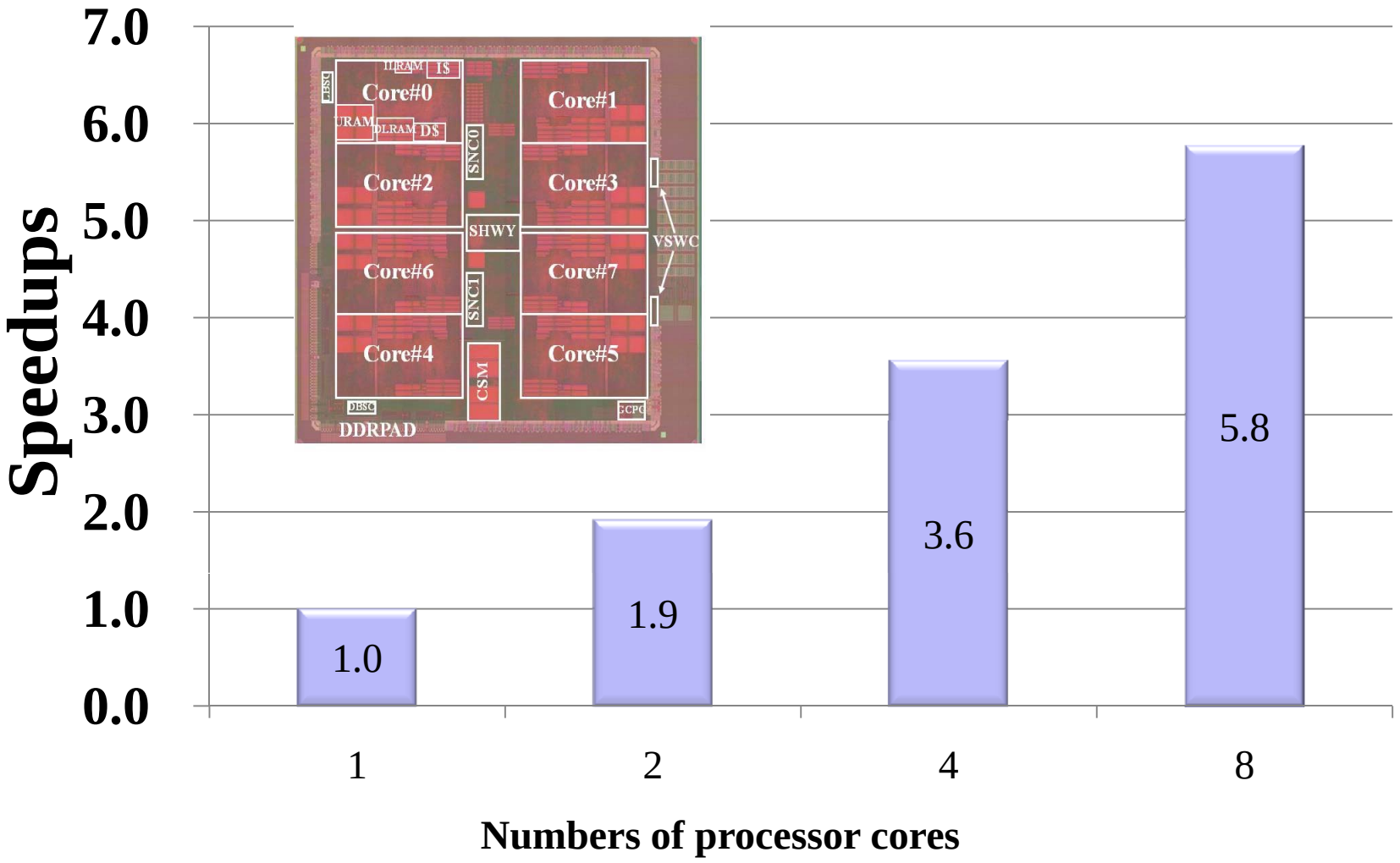


3.38 times speedup on the average for 4 cores against a single core execution

Processing Performance on the Developed Multicore Using Automatic Parallelizing Compiler

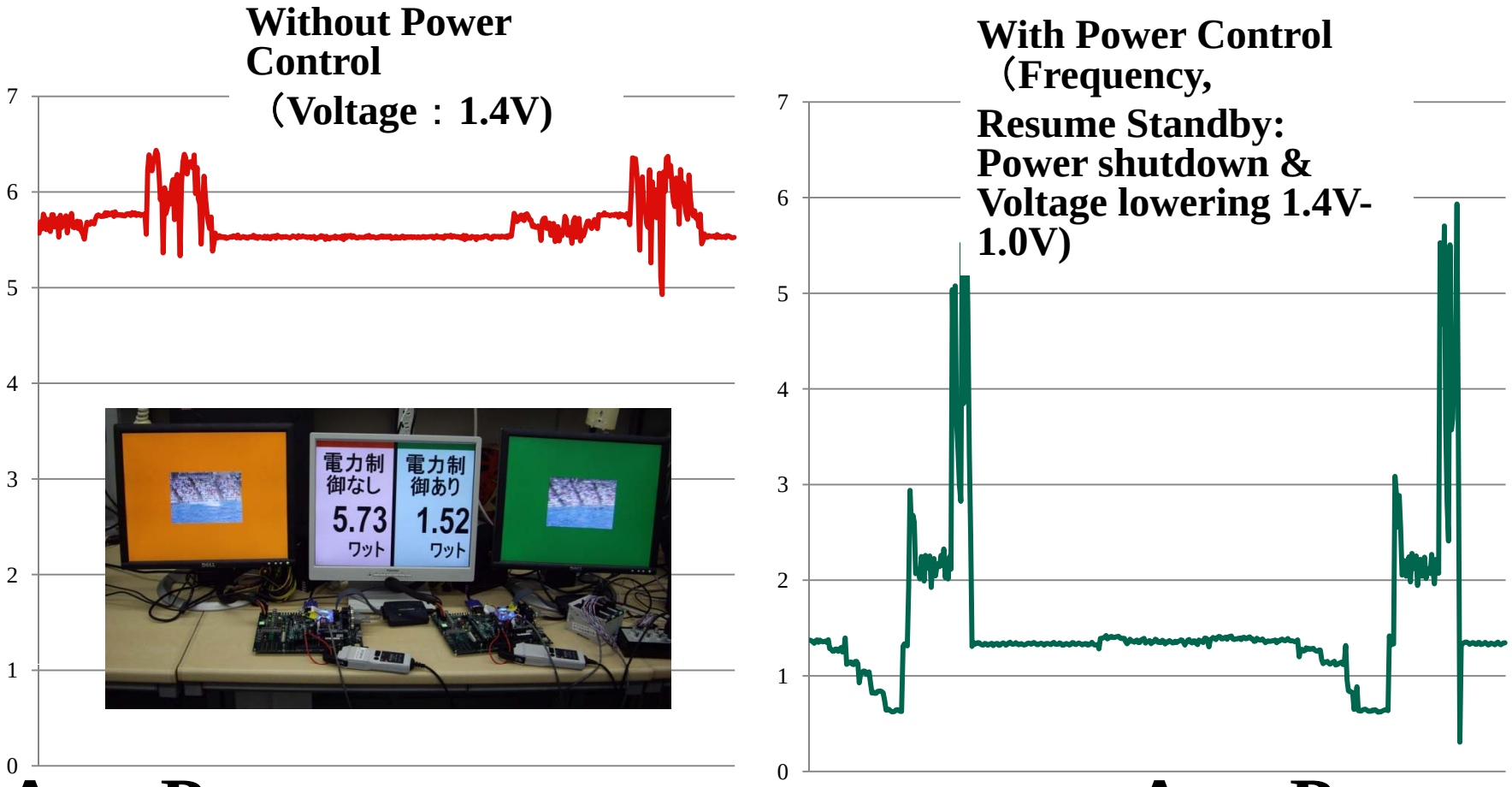
Speedup against single core execution for audio AAC encoding

*) Advanced Audio Coding



Power Reduction by OSCAR Parallelizing Compiler for MPEG2 Decoding

MPEG2 Decoding with 8 CPU cores



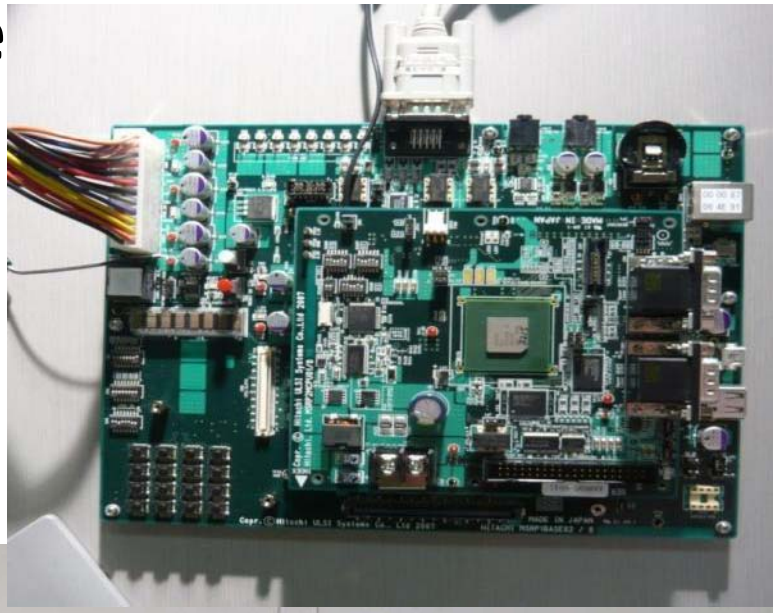
Avg. Power 5.73 [W]

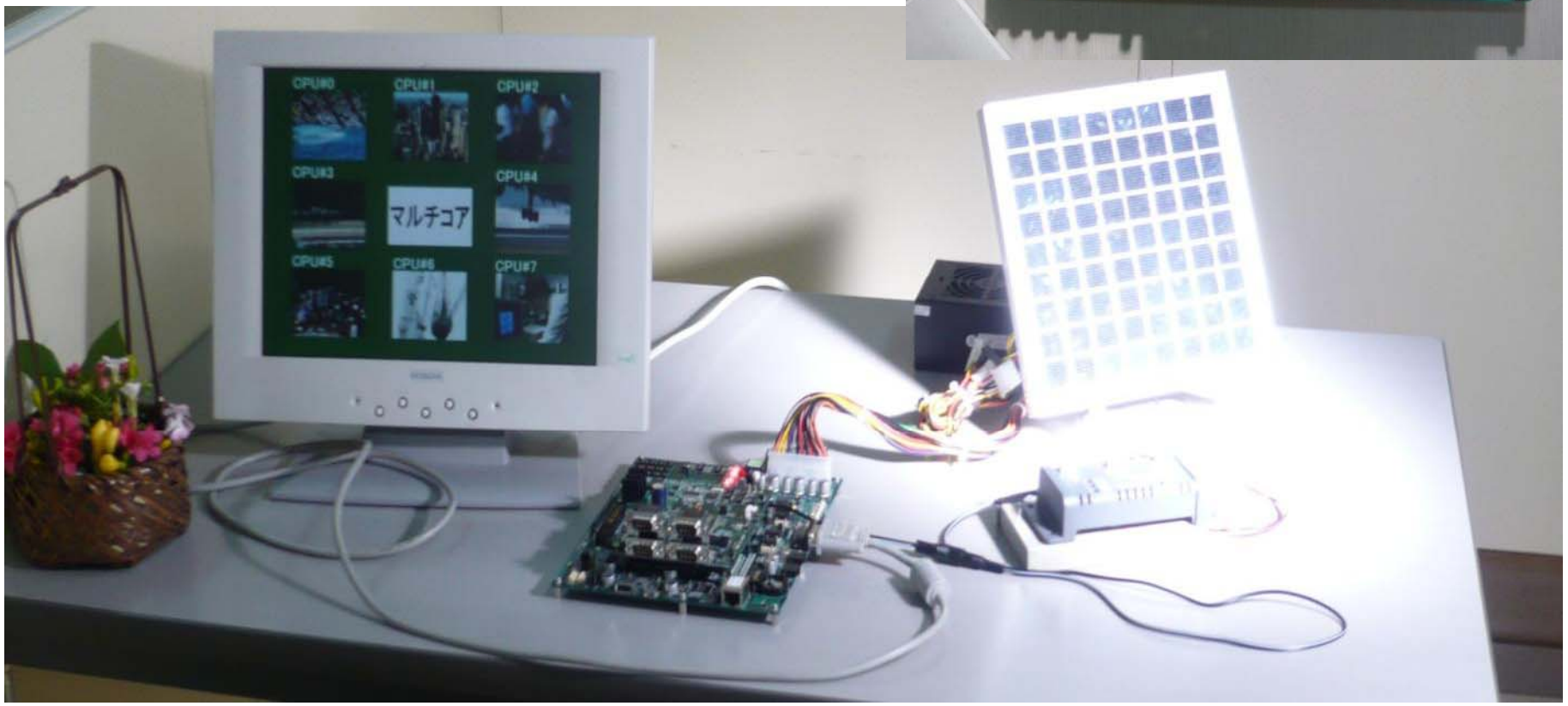
73.5% Power Reduction

Avg. Power 1.52 [W]

Low Power High Performance Multicore Computer with Solar Panel

- Clean Energy Autonomous
- Servers operational in deserts





Green Computing Systems R&D Center

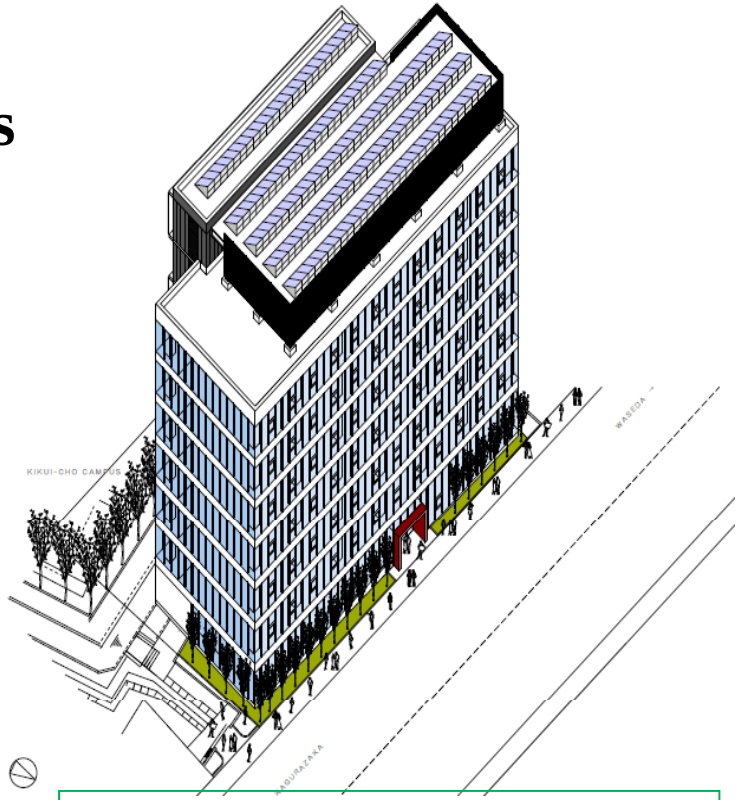
Waseda University

Supported by METI (Mar. 2011 Completion)

＜R & D Target＞

Hardware, Software, Application for Super Low-Power Manycore Processors

- **64-128 cores**
- **Natural air cooling(No cooling fun)**
  Cool, Compact, Clear, Quiet
- **Possibly operational by Solar Panel**



Beside Subway Waseda Station,
Near Waseda Univ. Main Campus

＜Industry, Government, Academia＞

Fujitsu, Hitachi, Renesas, Toshiba, NEC, etc

＜Ripple Effect＞

- **Low CO_2 (Carbon Dioxide) Emissions**
- **Creation Value Added Products**
  - **Consumer Electronics, Automobiles, Servers**