OSCAR Vector Multicore System
Platinum Vector Accelerator on FPGA

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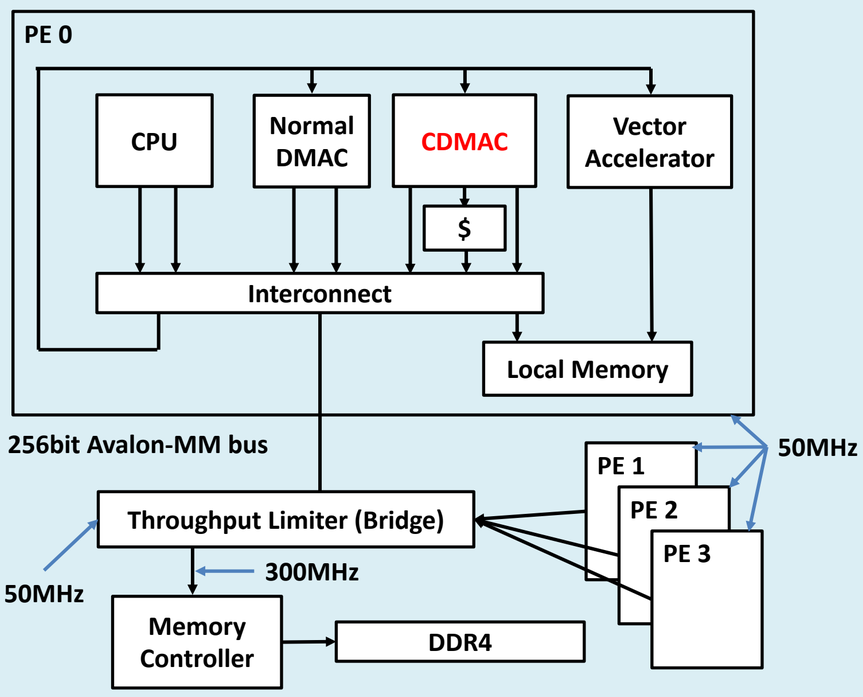
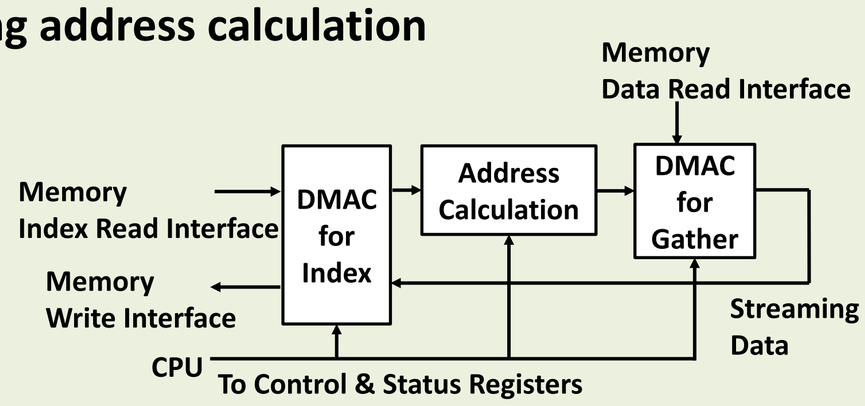
- OSCAR Compiler
- Vector Accelerator
- Clang/LLVM

Platinum Multicore Architecture



Cascaded DMA Controller (CDMAC)

- Our accelerator uses DMAC for data transfer with main memory
  - Separate data transfer and computation
- Enable vector processors to load data from continuous area even with indirect references
  - Handle sparse matrices efficiently
  - ➢ DMAC for indirect memory access
- Indirect memory access : out_arr[i] = data_arr[indices[i]]
  - ➢ We combined streaming address calculation and DMA components
- We also introduced cache to exploit memory locality of scattered data
  ex.) Structural calculation has high memory locality



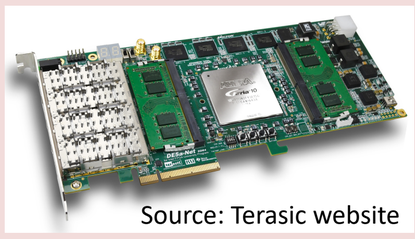
FPGA Implementation

Board: DE5a-Net-DDR4 (intelFPGA Arria10)
Accelerator Specification:

- 16 single precision ops/cycle
- Local Data Memory Bandwidth 32 byte/clock
- All data located on Local Data Memory
- Local Data Memory size: 32KB

CPU (NIOS II/f):

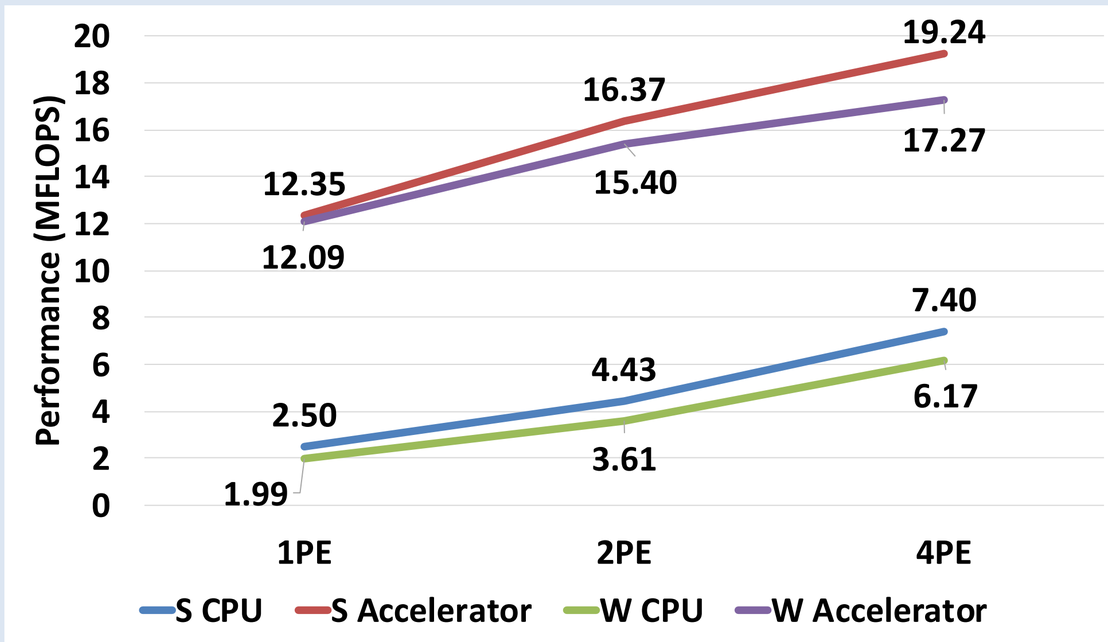
- Compiler: nios2-elf-gcc
- FPU: Floating Point Hardware 2
- Cache: 32KB


Source: Terasic website

NAS Parallel Benchmark CG

Applications

- NAS PARALLEL Benchmark CG
  - Size S, W
- Code Modification
  - Convert Fortran to C
  - Convert CSR format to SELL format
  - Parallelized using software coherent cache



Sparse Matrix Vector Multiplication

Applications

- Sparse matrices from SuiteSparse Matrix Collection (University of Florida Sparse Matrix Collection)
- We used SELL format
- Calculations are done by single precision floating point number and 32bit integer

Result

- CDMAC shows up to 17 times speedup compared to CPU execution.
- Band matrices show better performance than random matrices
  - Suitable for structural calculation