



OSCAR Automatic Parallelizing Compiler

Automatic Speedup and Power Reduction



Kasahara & Kimura Lab, Waseda University, TOKYO
<http://www.kasahara.cs.waseda.ac.jp>

OSCAR Automatic Parallelizing Compiler

To improve **effective performance**, **cost-performance** and **software productivity** and **reduce power**

Multigrain Parallelization

coarse-grain parallelism among loops and subroutines, **near fine grain parallelism** among statements in addition to **loop parallelism**

Data Localization

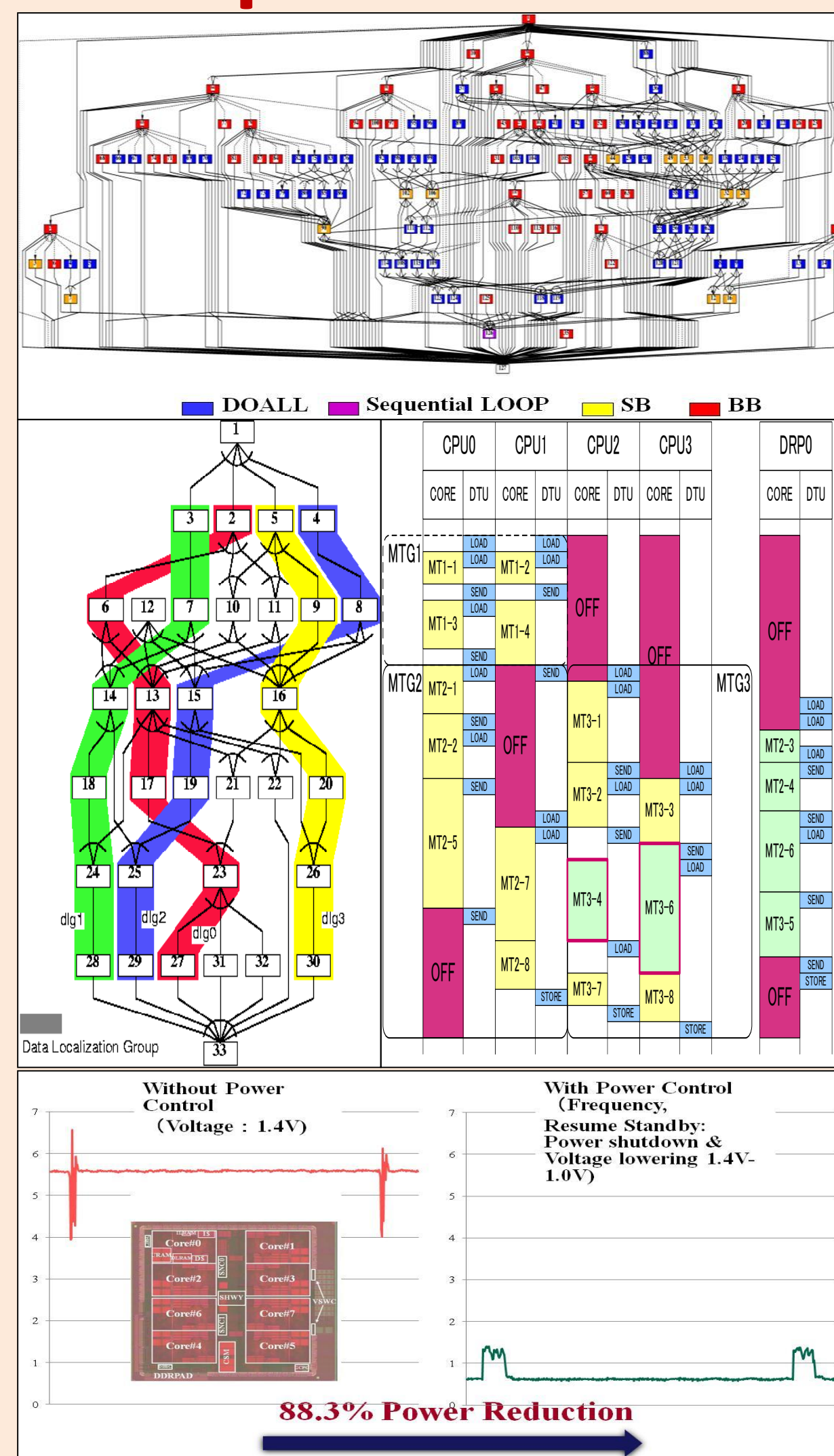
Automatic data management for **distributed shared memory**, **cache** and **local memory**

Data Transfer Overlapping

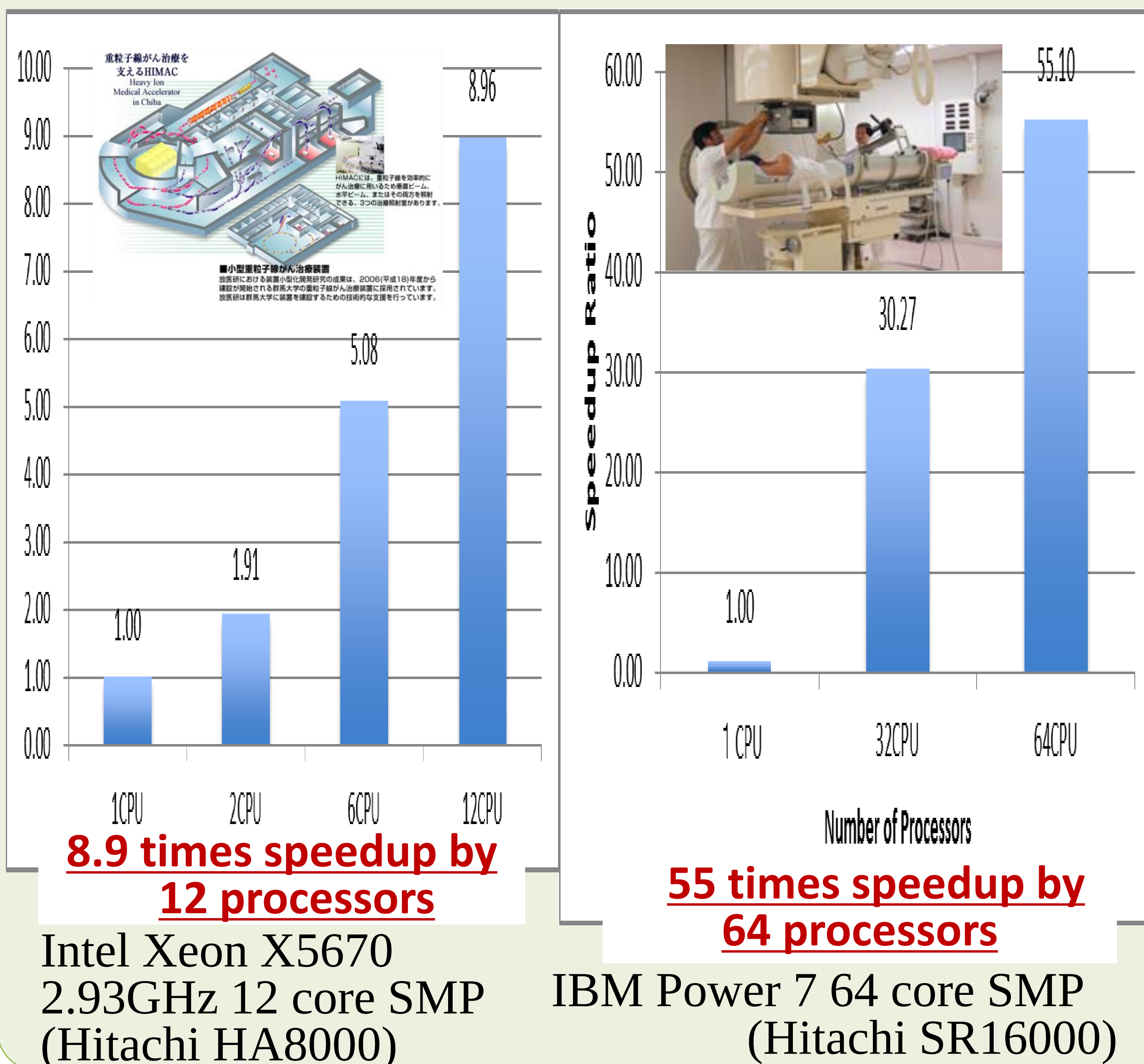
Data transfer overlapping using Data Transfer Controllers (DMAs)

Power Reduction

Reduction of consumed power by compiler control DVFS and Power gating with hardware supports.



Cancer Treatment Carbon Ion Radiotherapy



Software Coherent Cache

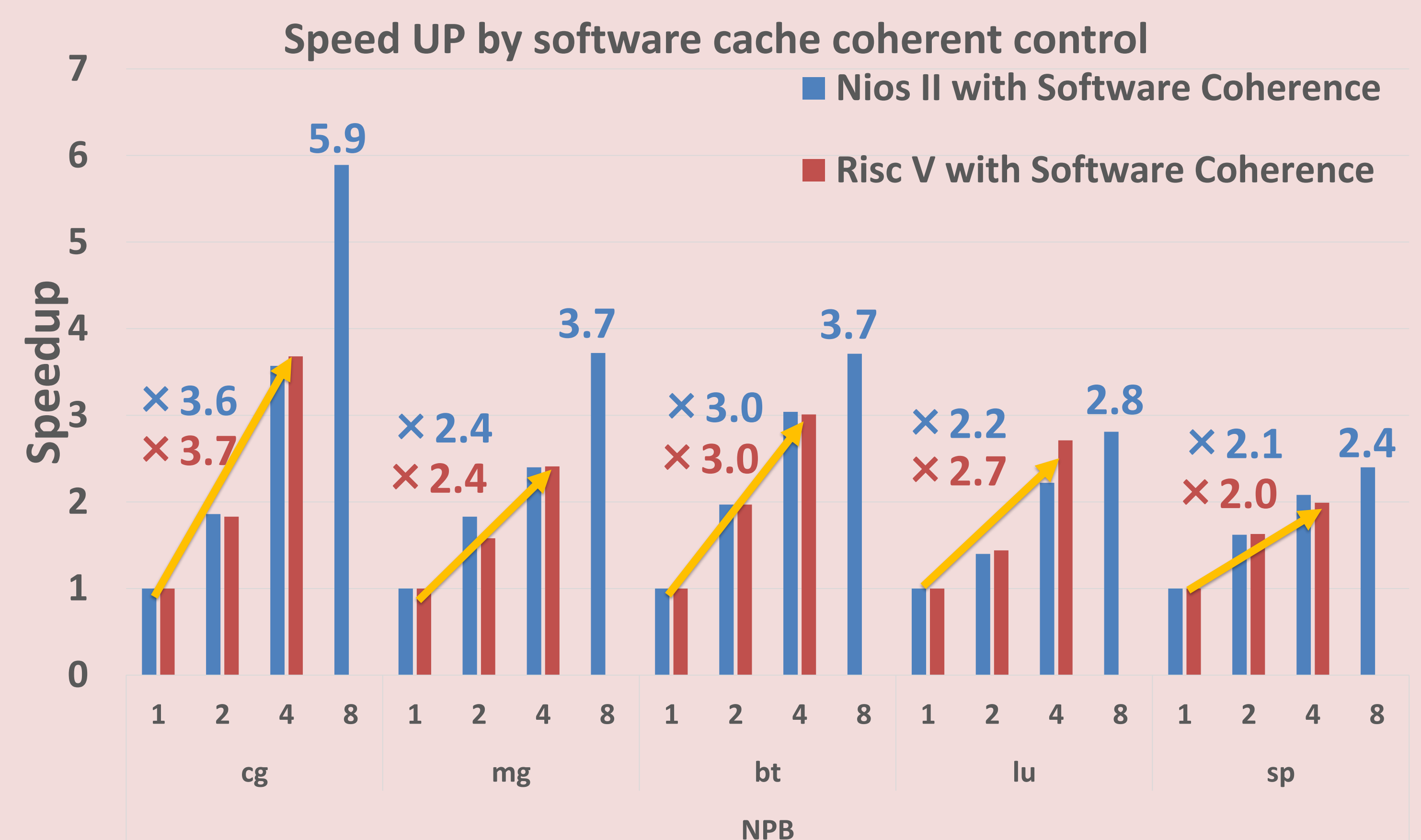
Parallelizing compiler directed software coherence technique for shared memory multicore systems without hardware cache coherence control

Advantages

- Smaller hardware and lower power consumption brought by removing expensive hardware cache coherence mechanism
- Higher performance by compiler's careful cache operation scheduling as well as memory optimization

Evaluation

- NIOS II / Risc V multicore system implemented in Arria10 SoC FPGA
 - I\$: 32KB / D\$:32KB (Each PE)
 - # of PE: 1PE, 2PE, 4PE, 8PE (only NIOS II)
- Application
 - NAS Parallel Benchmarks



Local Memory Management

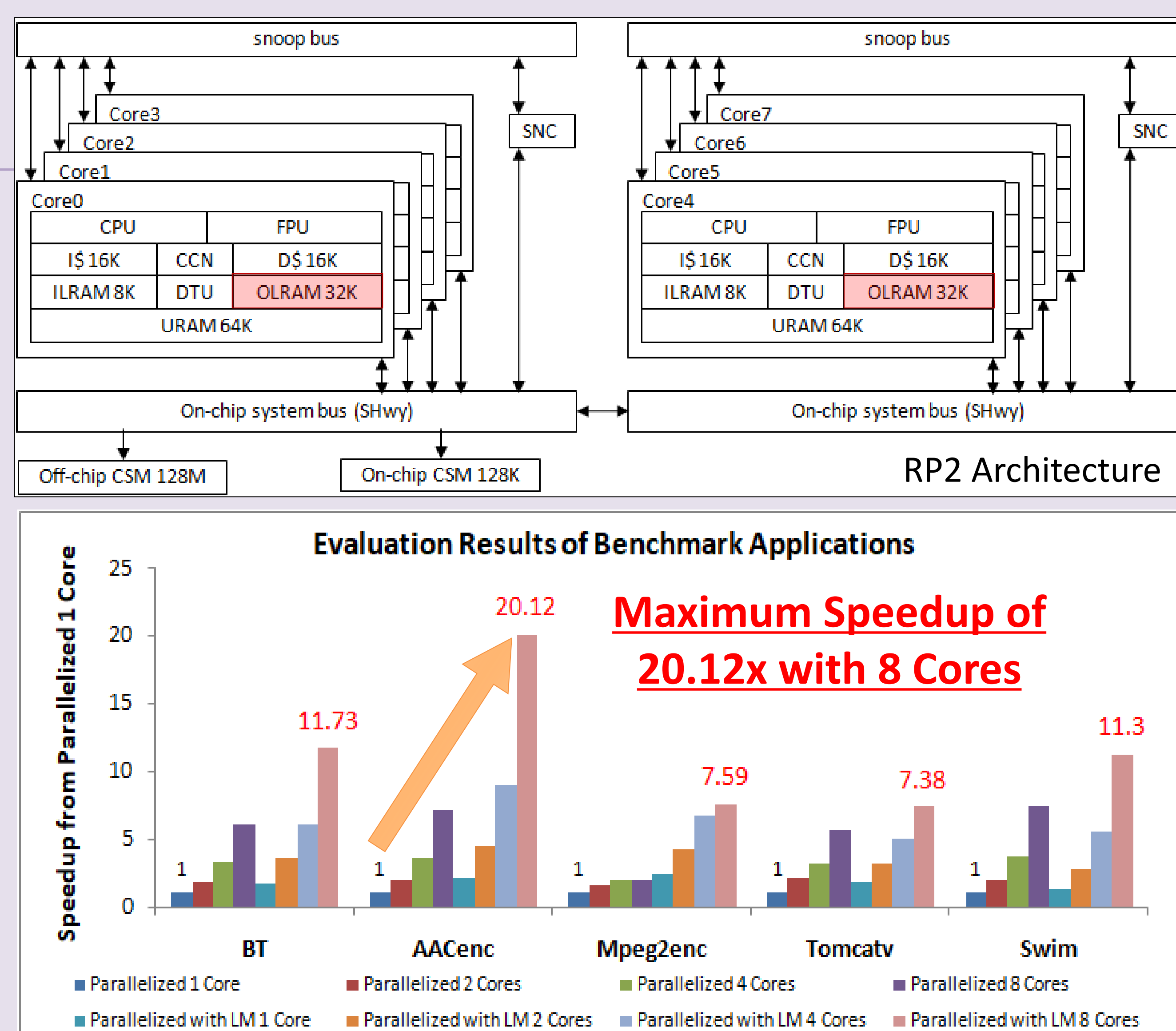
Local memory management technique for multicore processors by the OSCAR Compiler

Overview

- Decomposing data from multiple loops and mapping onto fast and small size local memory
- Block sizes of local memory determined by input application features

Evaluation

- RP2 PROCESSOR (Renesas Electronics, Hitachi, Waseda University)
 - 32KB Local Memory (LM) per core
- Benchmark Applications
 - From NAS Parallel Benchmark, SPEC, AAC Encoder, and MediaBench



SC19 members

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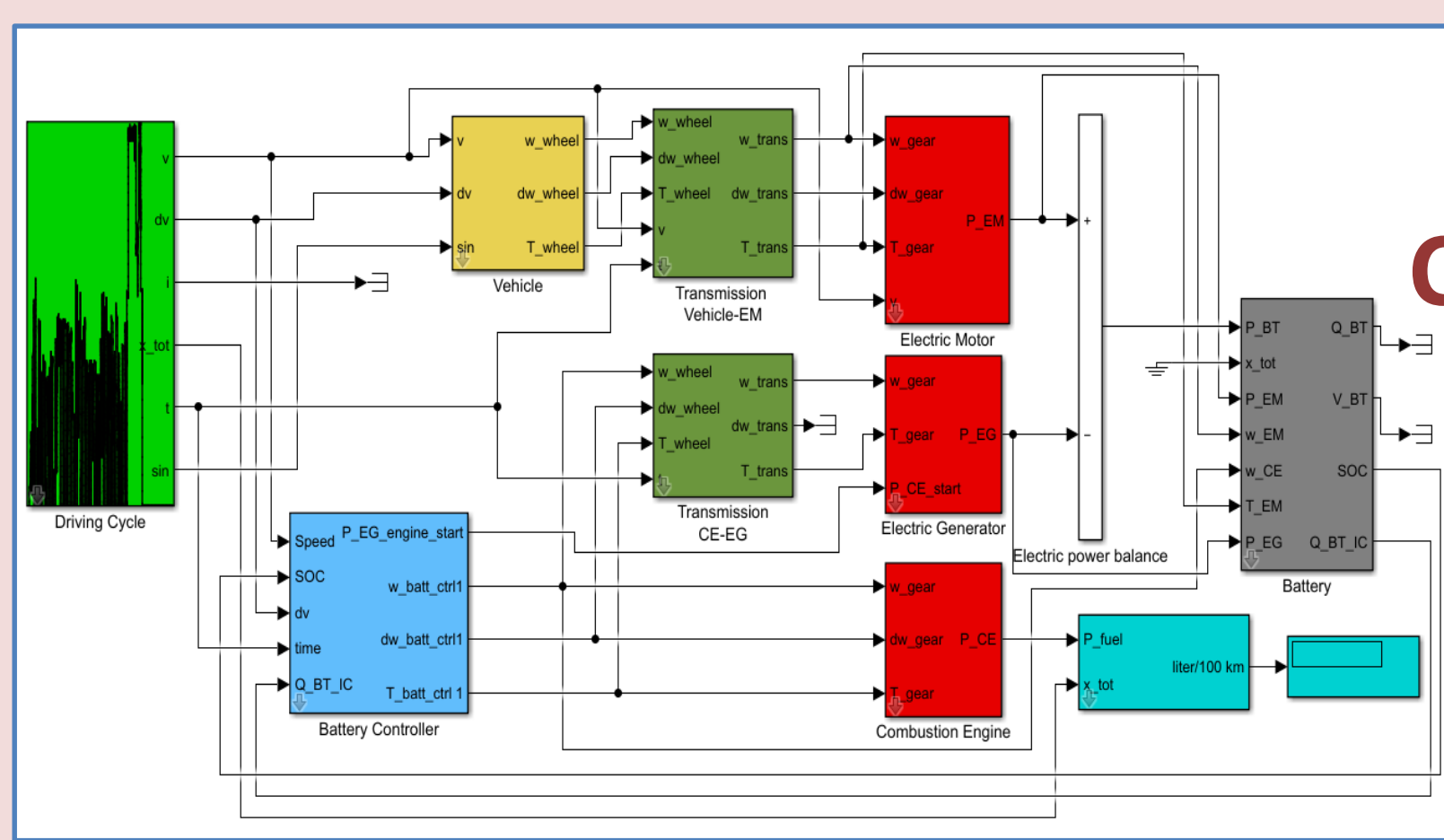
Parallel Processing of MATLAB/Simulink by OSCARator on Intel multi cores

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- OSCAR Compiler
- OSCARator
- MATLAB/Simulink
- Multi grain Parallelization

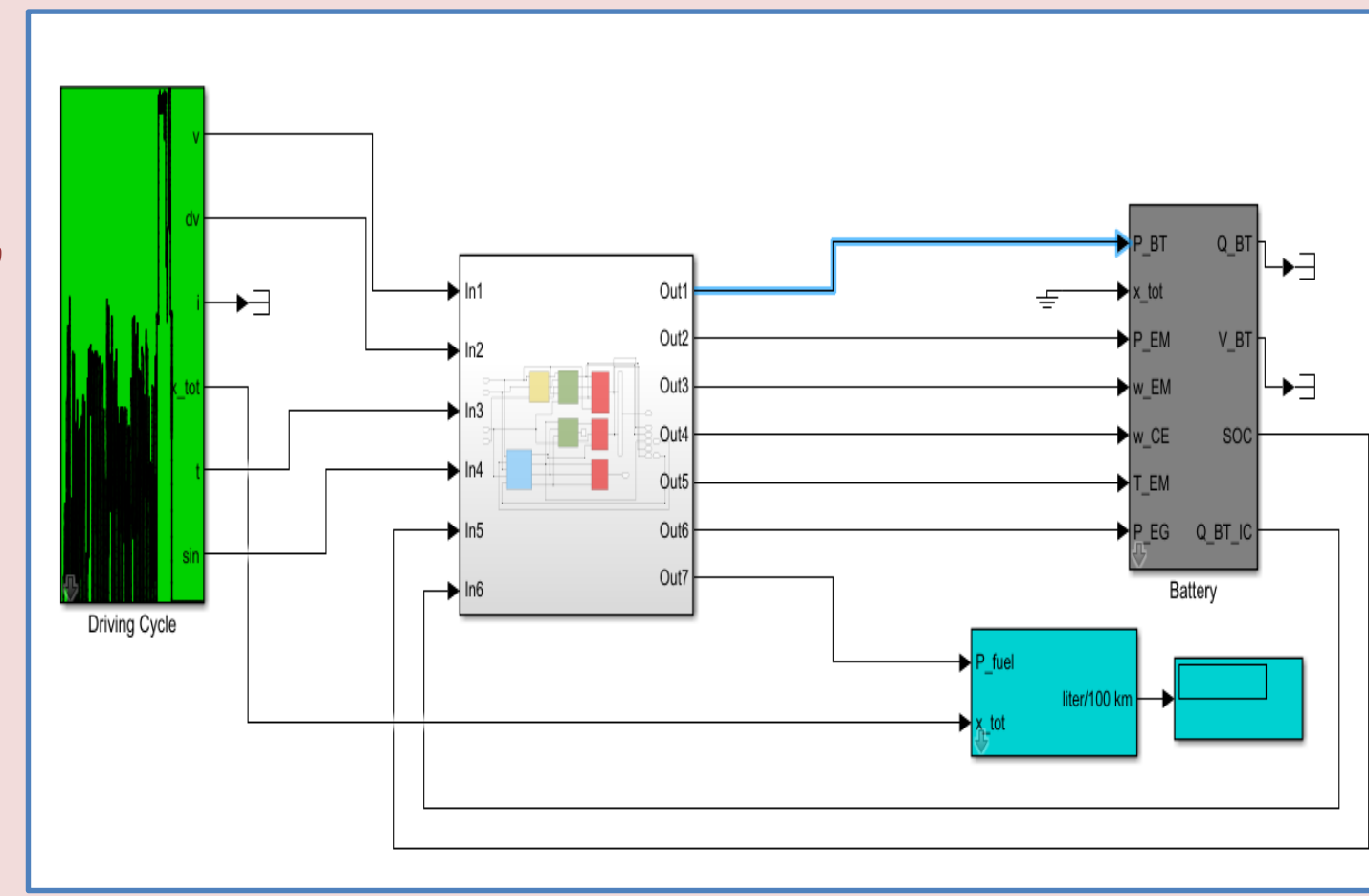
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OSCARator: Automatic Parallelization of MATLAB/Simulink powered by OSCAR Compiler

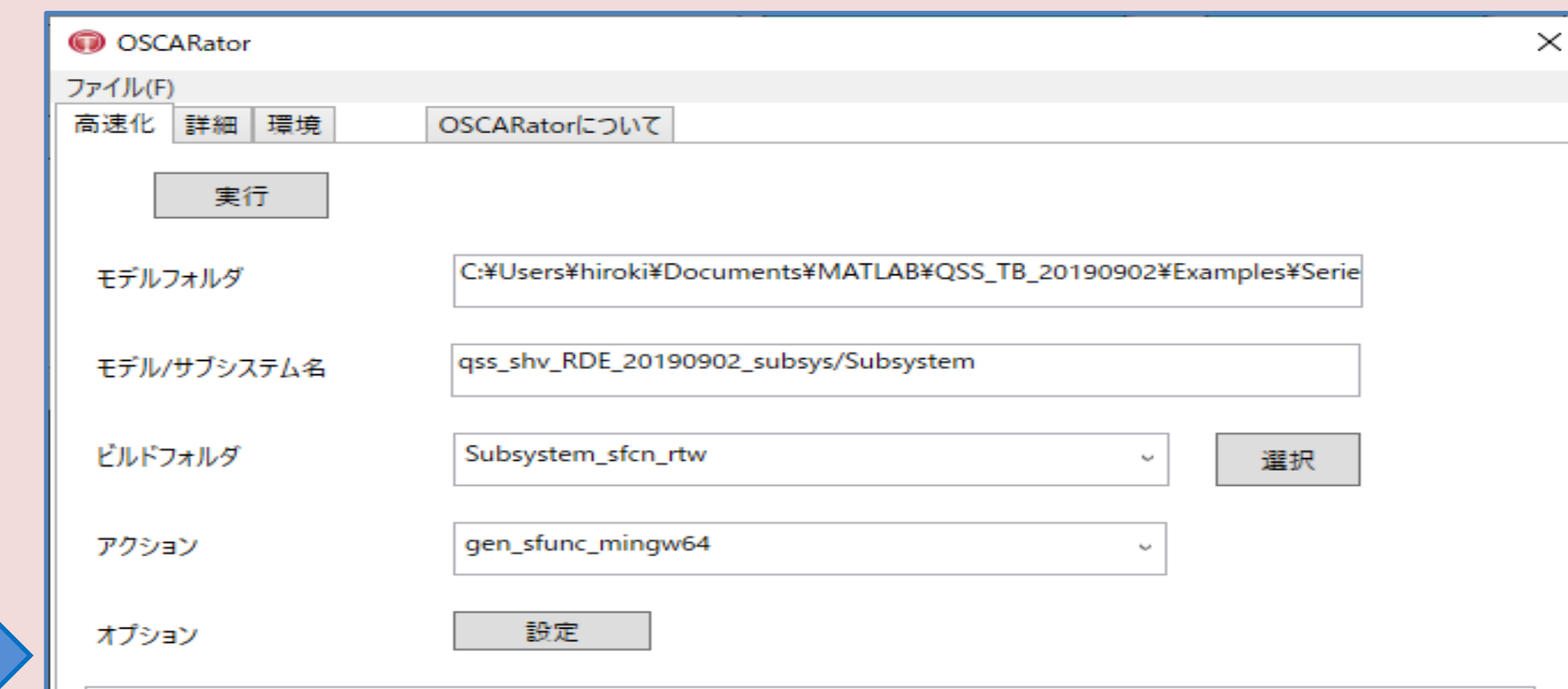


Original Simulink model

Create "Subsystem"
with blocks
to accelerate

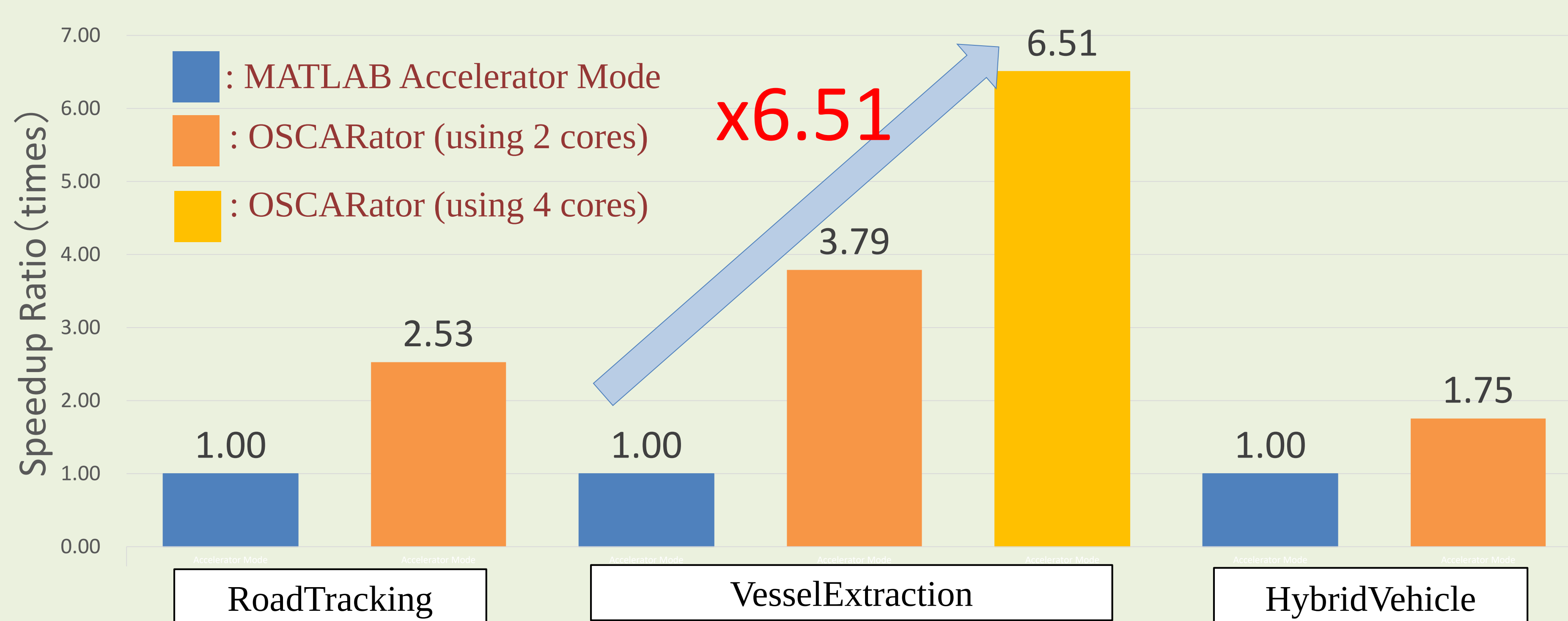


Simulink model with "Subsystem"



Simple Configuration Window

Speedup of Simulink Models by OSCARator on 4 cores Intel Core i5 Processor



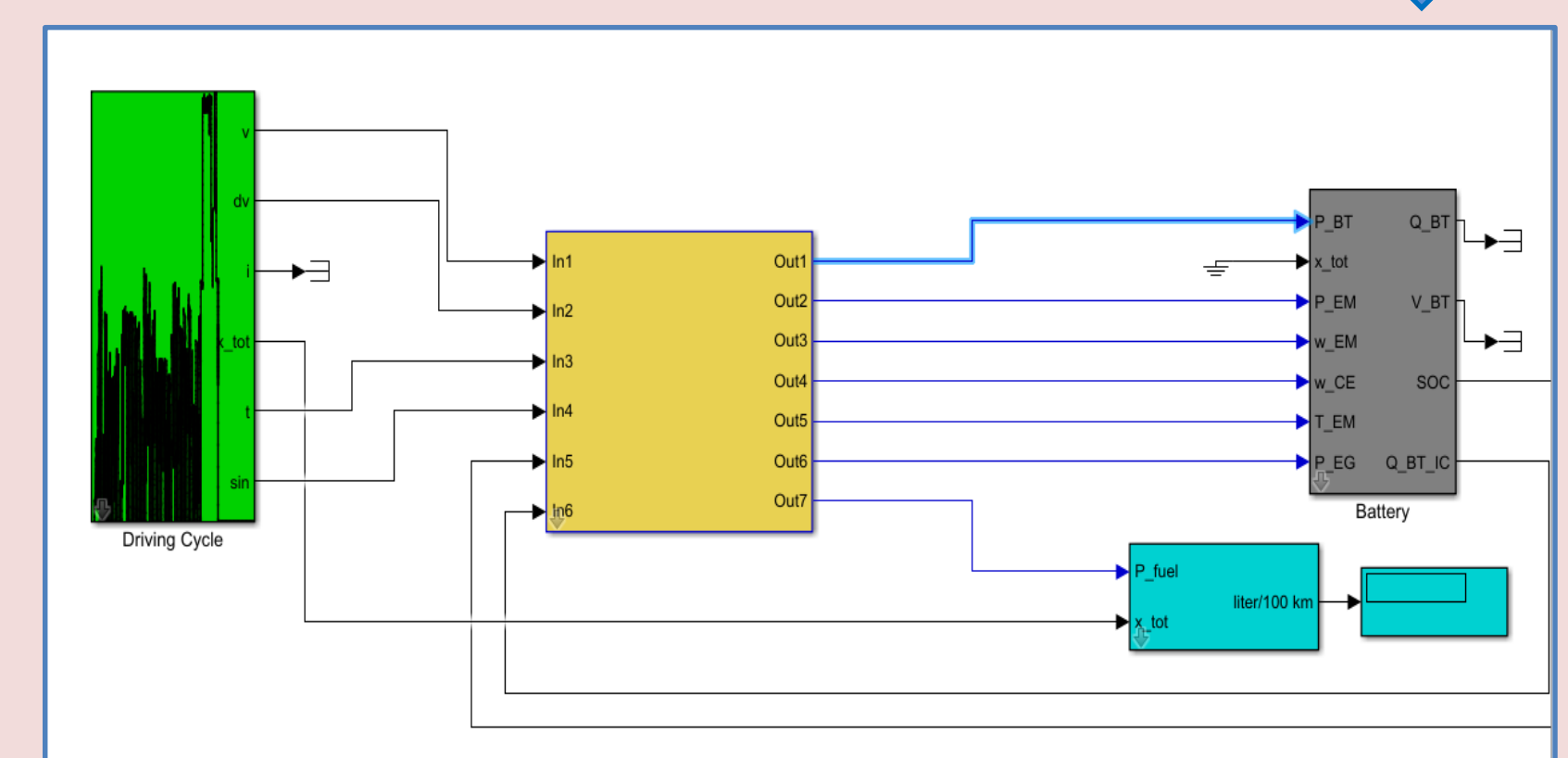
FULLY AUTOMATIC

Simulink Coder C-Code Generation

Automatic Parallelization

S-Function MEX Build

Replacing Subsystem with S-Function Block



New Accelerated Simulink model

Same Result

**Shorter Simulation Time
vs Original Simulink model**



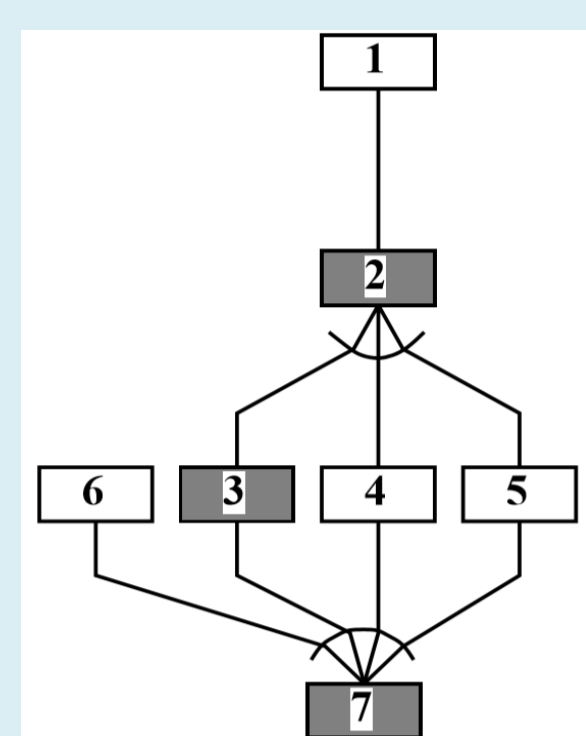
Parallelization and Cache Optimization by OSCAR Compiler on NEC SX-Aurora TSUBASA

Kasahara & Kimura Lab, Waseda University, TOKYO

- OSCAR Compiler
- NEC SX-Aurora TSUBASA

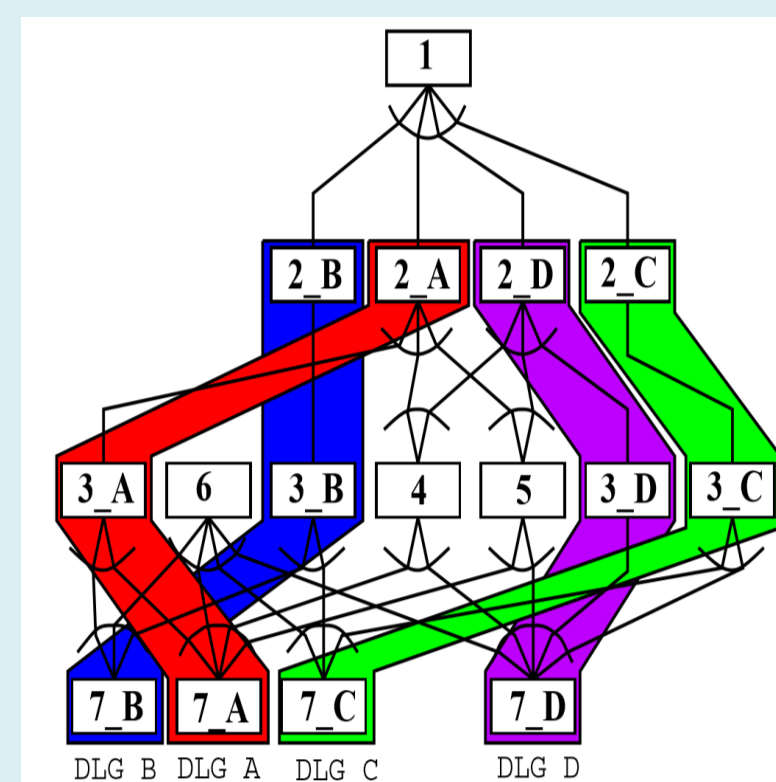
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Work Flow



OSCAR Compiler

Automatic
Parallelization
And Cache
Optimization



NEC Compiler

Automatic
Vectorization

Executable
File

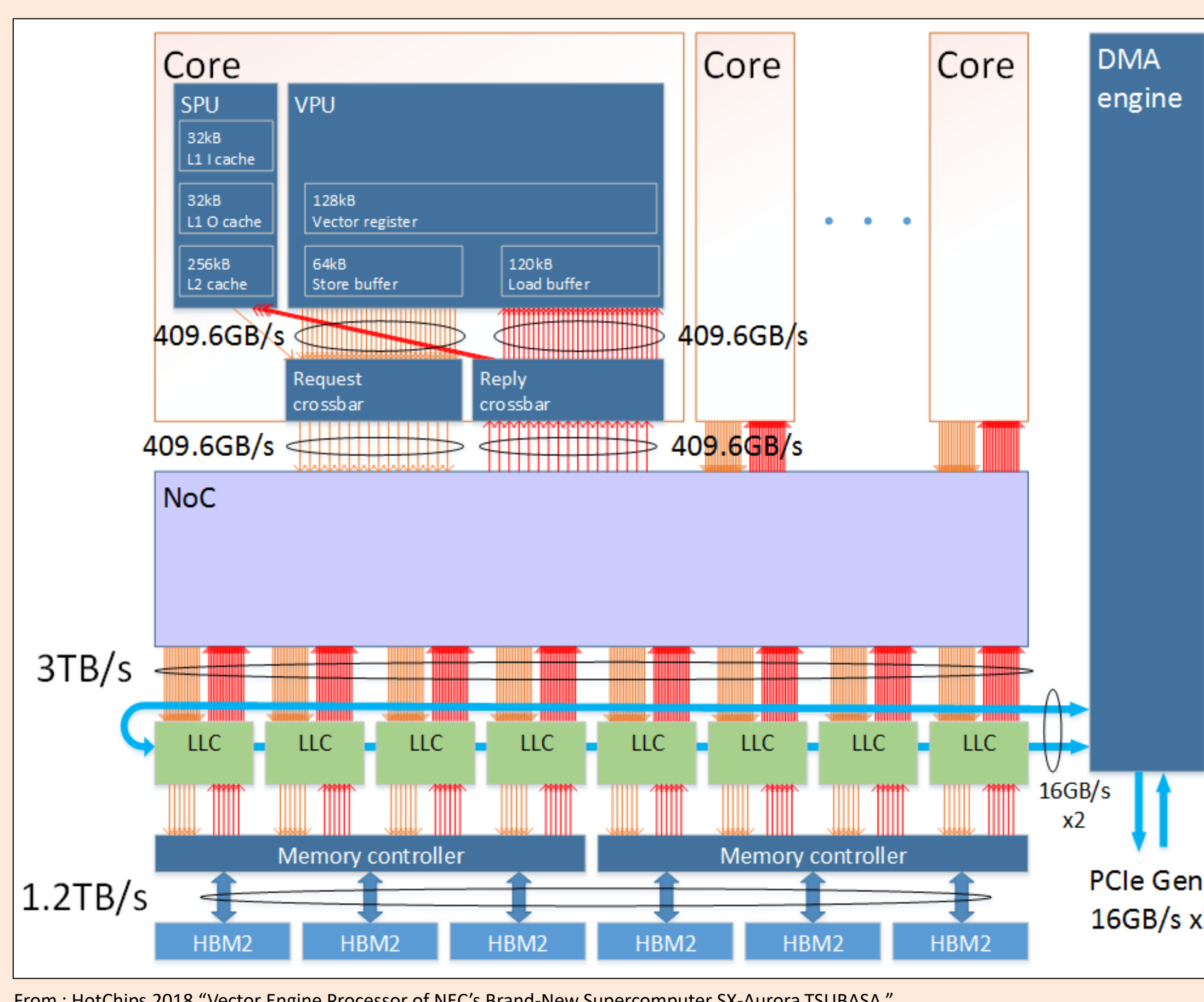
Parallelize &
Vectorize execution

Applications

- swim (SPEC 2000)
 - Size 8004x8004
- BT(NPB)
 - CLASS C

NEC SX-Aurora TSUBASA Architecture

8 Vector Core
16MB LLC
DMA Engine
6 HBM2 Controller



Speedups on SX-Aurora TSUBASA

