Automatic Parallelization by OSCAR Compiler for NEC SX-Aurora TSUBASA

Hironori Kasahara, Ph.D., IEEE Fellow, IPSJ Fellow

Senior Executive Vice President, Waseda University

IEEE Computer Society President 2018

URL: http://www.kasahara.cs.waseda.ac.jp/ （Booth 857 ITBL）

1980 BS, 82 MS, 85 Ph.D. , Dept. EE, Waseda Univ.
1985 Visiting Scholar: **U. of California, Berkeley,**
1986 Assistant Prof., 1988 Associate Prof., 1989-90
Research Scholar:**U. of Illinois, Urbana-Champaign,
Center for Supercomputing R&D, 1997 Prof.,** 2004
Director, Advanced Multicore Research Institute,
2017 member: **the Engineering Academy of Japan**
and **the Science Council of Japan**
2018 Nov. Senior Vice President, Waseda Univ.

1987 IFAC World Congress Young Author Prize
1997 IPSJ Sakai Special Research Award
2005 STARC Academia-Industry Research Award
2008 LSI of the Year Second Prize
2008 Intel AsiaAcademic Forum Best Research Award
2010 IEEE CS Golden Core Member Award
2014 Minister of Edu., Sci. & Tech. Research Prize
2015 IPSJ Fellow, 2017 IEEE Fellow, Eta Kappa Nu
2019 IEEE Spirit of Computer Society Award

Reviewed **Papers: 216, Invited Talks: 180, Granted Patents: 50** (Japan, US, GB, China), **Articles** in News Papers, Web News, Medias incl. TV etc.:

Committees in Societies and Government 260
IEEE Computer Society： President 2018, Executive Committee(2017-2019), BoG(2009-14), Strategic Planning Committee Chair 2018, Multicore STC Chair (2012-), Japan Chair(2005-07),
IPSJ Chair: HG for Magazine. & J. Edit, Sig. on ARC.
【METI/NEDO】 **Project Leaders: Multicore** for Consumer Electronics, Advanced **Parallelizing Compiler**, Chair: Computer Strategy Committee
【Cabinet Office】 CSTP Supercomputer Strategic ICT PT, **Japan Prize Selection Committees**, etc.
【MEXT】 **Info. Sci. & Tech. Committee,** Supercomputers (**Earth Simulator,** HPCI Promo., Next Gen. Supercomputer **K**) Committees, etc.

1

About WASEDA – 早稲田大学

Number of International Students

7,942* from **125*** countries and territories
(Undergraduate and Graduate)

Graduate Employability

#1 in private university of Japan
(#2 in Japan, #27 in the world)
QS Graduate Employability Rankings 2019

ENROLLMENT [学生数]	ALUMNI [卒業生]
49,436	630,000
World Business	FACULTY [教員]
5 Palmes in Eduniversal Business	5,468

PARTNER INSTITUTIONS [協定大学・機関]	NUMBER OF BOOKS [図書館蔵書]	GRADUATE STUDENTS [大学院生]	UNDERGRADUATE STUDENTS [学部生]
848 (93 countries)	5,800,000	8,385	41,051

Alumni CEOs in Japan

10,606

8 Prime Ministers

Founder Shigenobu OKUMA

Masaru IBUKA   Tadashi YANAI

Hiroshi YAMAUCHI

Prime Ministers

- 8th Shigenobu Okuma
- 17th Shigenobu Okuma
- 55th Tanzan Ishibashi
- 74th Noboru Takeshita
- 76th Toshiki Kaifu
- 84th Keizo Obuchi
- 85th Yoshiro Mori
- 91st Yasuo Fukuda
- 95th Yoshihiko Noda

Business Leaders
Founders of global companies

- Sony
- Samsung
- Casio
- LOTTE

Business Leaders
CEOs of global companies

- ANA (All Nippon Airways)
- HONDA
- Nintendo
- UNIQLO
- Shiseido
- Nomura Securities Co., Ltd.
- Tokio Marine & Nichido Fire Insurance Co., Ltd.
- Olympus Corporation

Aiji TANAKA
President
International Political Science Association (IPSA) President 2016

Hironori KASAHARA
Senior Executive Vice President
IEEE Computer Society President 2018. The first president from outside USA and Canada in 72 years CS history. CS has 84,000 members from, 168 countries.

Toshio FUKUDA
The University Professor Waseda, Waseda Alumnus, Prof. Emeritus Nagoya Univ., Prof. Meijo Univ. IEEE President 2020. The first from Asia in 135 years history. IEEE has 420,000 members.

mercari
HEROZ JAPAN
LINE

早稲田大学

Haruki MURAKAMI   Hirokazu KOREEDA   Yuzuru HANYU

S. ARAKAWA

Daiya SETO

IEEE Computer Society

Bjarne Stroustrup: Morgan Stanley & Columbia Univ.
2018 IEEE Computer Society Computer Pioneer Award
IEEE COMPSAC2018 Keynote & Award Ceremony

July 26, 2018, Keynote, Hitotsubashi Hall

July 25, 2018 Award Ceremony Rihga Royal Hotel Tokyo

Tencent–Waseda University Technical Tour

• 84,000+ members

• 480 chapters
• 168 countries
• 31 technical committees & councils

THE SEYMOUR CRAY AWARD

2018 IEEE COMPUTER SOCIETY SEYMOUR CRAY COMPUTER ENGINEERING AWARD
DR. DAVID E. SHAW
FOR THE DESIGN OF SPECIAL-PURPOSE SUPERCOMPUTERS FOR BIOMOLECULAR SIMULATIONS

IEEE CS Awards Ceremonies with CS President 2018

June BoG Award Dinner with CS Award Winners and their Families, Phoenix

Technical Achievement Award, in COMPSAC, Tokyo

Computer Pioneer Award to C++ Bjarne Stroustrup in COMPSAC, Tokyo

B. Ramakrishna Rau Award in MICRO, Fukuoka

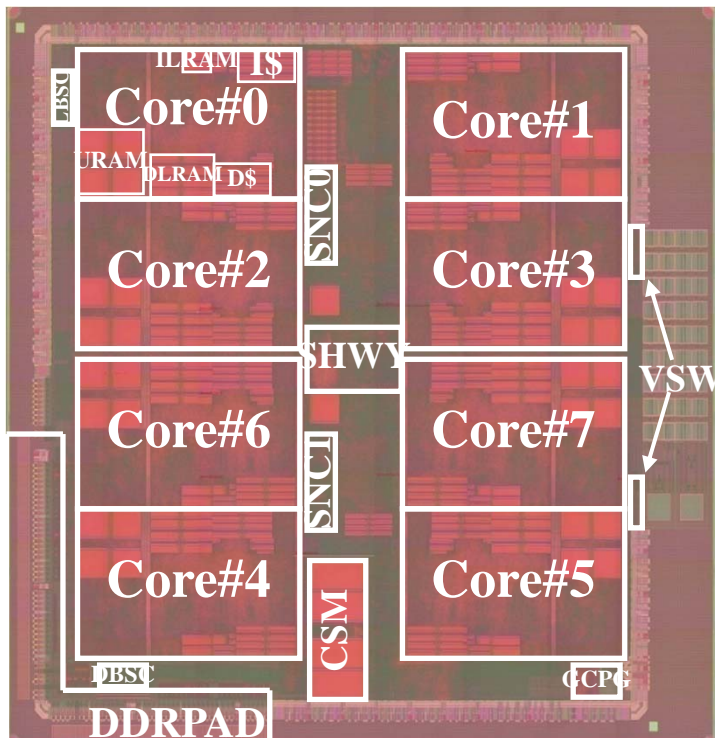Award Ceremony in SC (Super Computing 2018 with 13 thousands participants), Dallas

Cornel Univ. Prof. Steven Squyres火星探査、CalTech. Dr. Katie Boumanブラックホールの可視化等のる講演等

Multicores for Performance and Low Power

Power consumption is one of the biggest problems for performance scaling from smartphones to cloud servers and supercomputers ("K" more than 10MW) .

IEEE ISSCC08: Paper No. 4.5, M.ITO, … and H. Kasahara, "An 8640 MIPS SoC with Independent Power-off Control of 8 CPUs and 8 RAMs by an Automatic Parallelizing Compiler"

Power $\propto$ Frequency * Voltage^2
(Voltage $\propto$ Frequency)

➡ **Power $\propto$ Frequency^3**

If Frequency is reduced to 1/4 (Ex. 4GHz→1GHz), Power is reduced to 1/64 and Performance falls down to 1/4 .
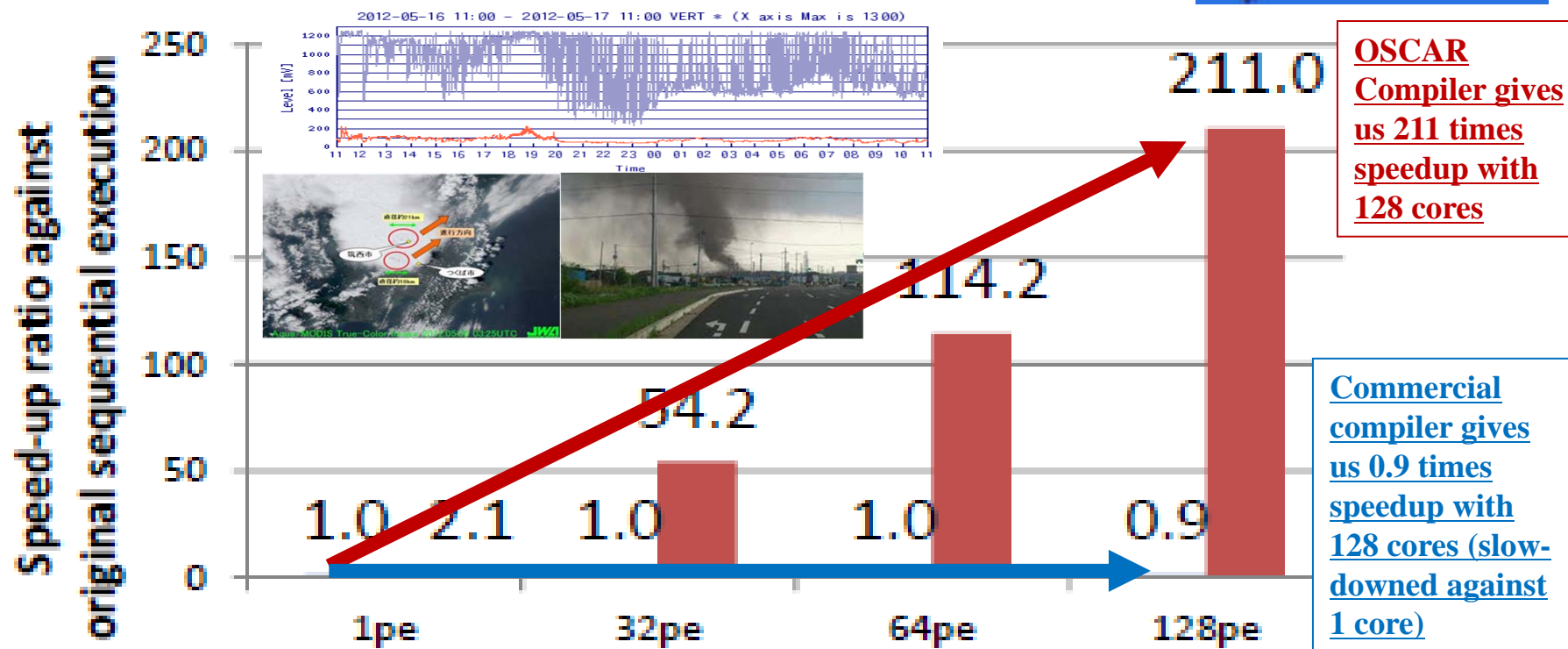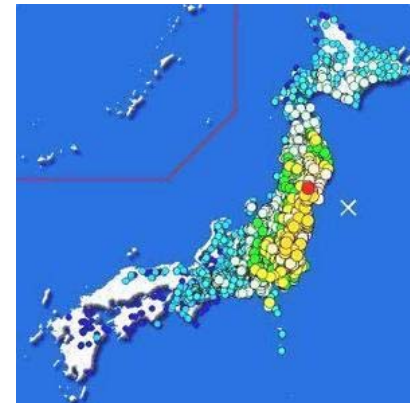
\<Multicores\>

If 8cores are integrated on a chip, Power is still 1/8 and Performance becomes 2 times.

Parallel Soft is important for scalable performance of multicore (LCPC2015)

- Just more cores don't give us speedup
- Development cost and period of parallel software are getting a bottleneck of development of embedded systems, eg. IoT, Automobile

Earthquake wave propagation simulation GMS developed by National Research Institute for Earth Science and Disaster Resilience (NIED)


OSCAR Compiler gives us 211 times speedup with 128 cores

Commercial compiler gives us 0.9 times speedup with 128 cores (slow-downed against 1 core)

- Automatic parallelizing compiler available on the market gave us no speedup against execution time on 1 core on 64 cores
  - Execution time with 128 cores was slower than 1 core (0.9 times speedup)
- Advanced OSCAR parallelizing compiler gave us 211 times speedup with 128cores against execution time with 1 core using commercial compiler
  - OSCAR compiler gave us 2.1 times speedup on 1 core against commercial compiler by global cache optimization

7

Power Reduction of MPEG2 Decoding to 1/4 on 8 Core Homogeneous Multicore RP-2 by OSCAR Parallelizing Compiler

MPEG2 Decoding with 8 CPU cores
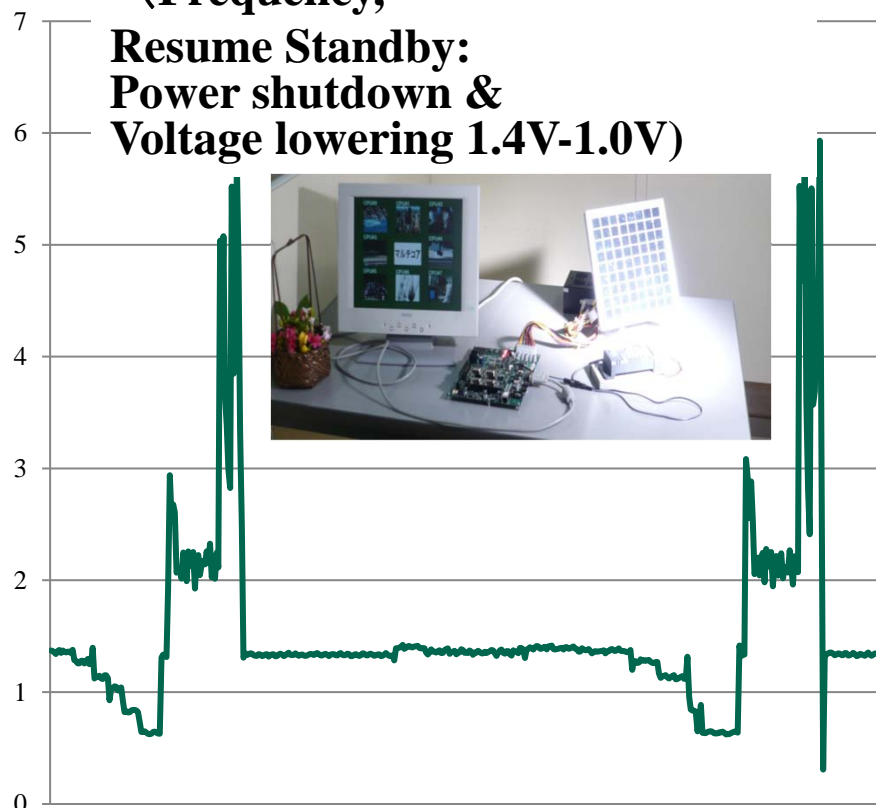
Without Power Control （Voltage：1.4V)
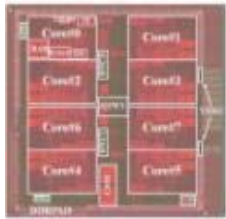
With Power Control （Frequency, Resume Standby: Power shutdown & Voltage lowering 1.4V-1.0V)
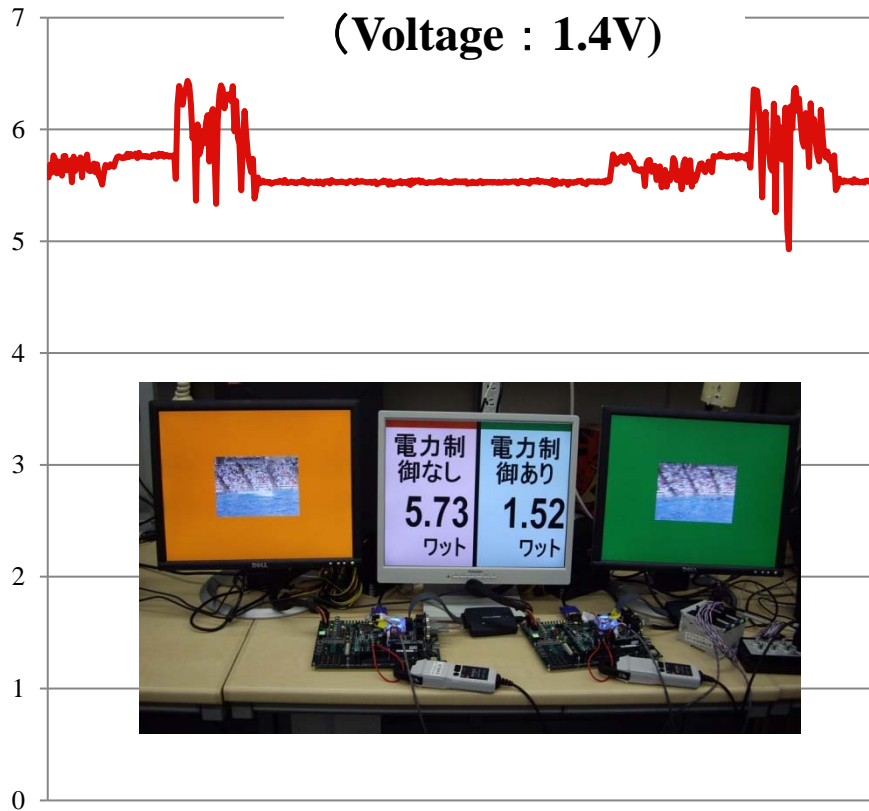
Avg. Power 5.73 [W]

73.5% Power Reduction

Avg. Power 1.52 [W]

8

OSCAR Parallelizing Compiler

To improve effective performance, cost-performance and software productivity and reduce power

Multigrain Parallelization(LCPC1991,2001,04)

coarse-grain parallelism among loops and subroutines (2000 on SMP), near fine grain parallelism among statements (1992) in addition to loop parallelism

Data Localization

Automatic data management for distributed shared memory, cache and local memory (Local Memory 1995, 2016 on RP2,Cache2001,03) Software Coherent Control (2017)

Data Transfer Overlapping(2016 partially)

Data transfer overlapping using Data Transfer Controllers (DMAs)

Power Reduction

(2005 for Multicore, 2011 Multi-processes, 2013 on ARM)

Reduction of consumed power by compiler control DVFS and Power gating with hardware supports.

DOALL   Sequential LOOP   SB   BB

Data Localization Group

Without Power Control (Voltage : 1.4V)

With Power Control (Frequency, Resume Standby: Power shutdown & Voltage lowering 1.4V-1.0V)

88.3% Power Reduction
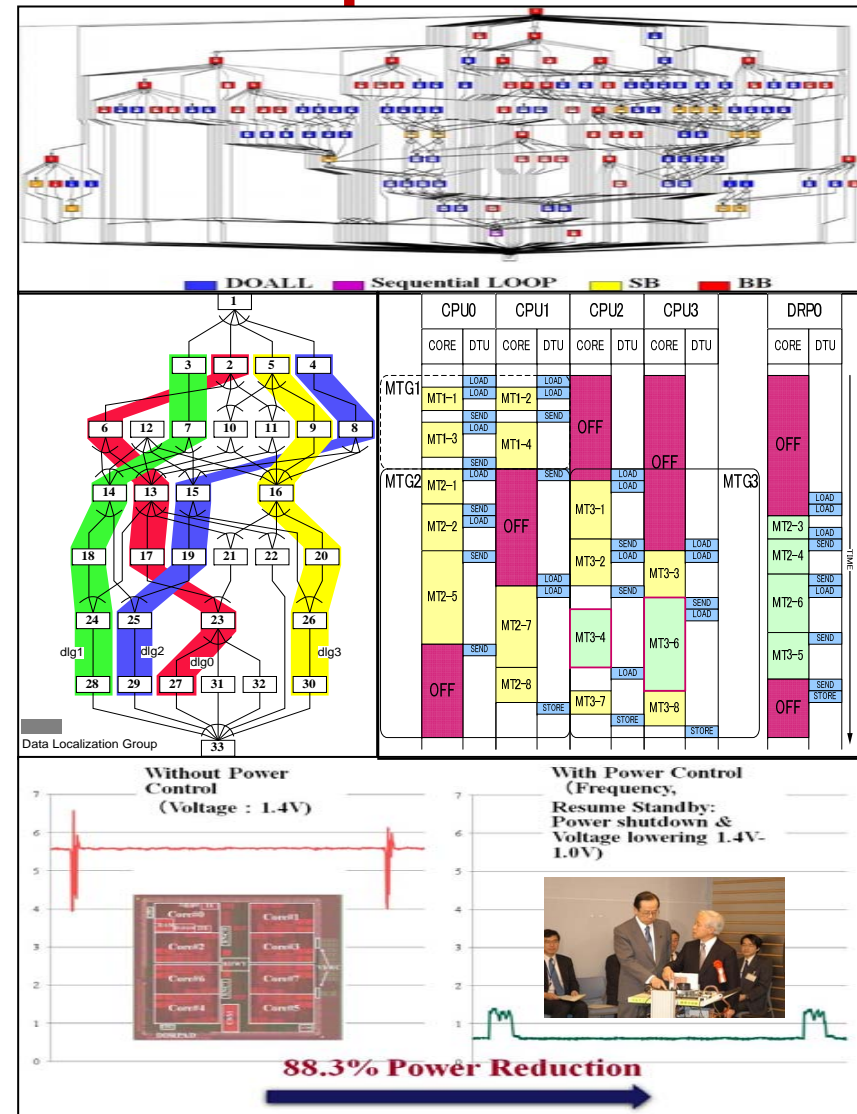
Multicore Program Development Using OSCAR API V2.0

Sequential Application Program in Fortran or C
(Consumer Electronics, Automobiles, Medical, Scientific computation, etc.)

OSCAR API for Homogeneous and/or Heterogeneous Multicores and manycores
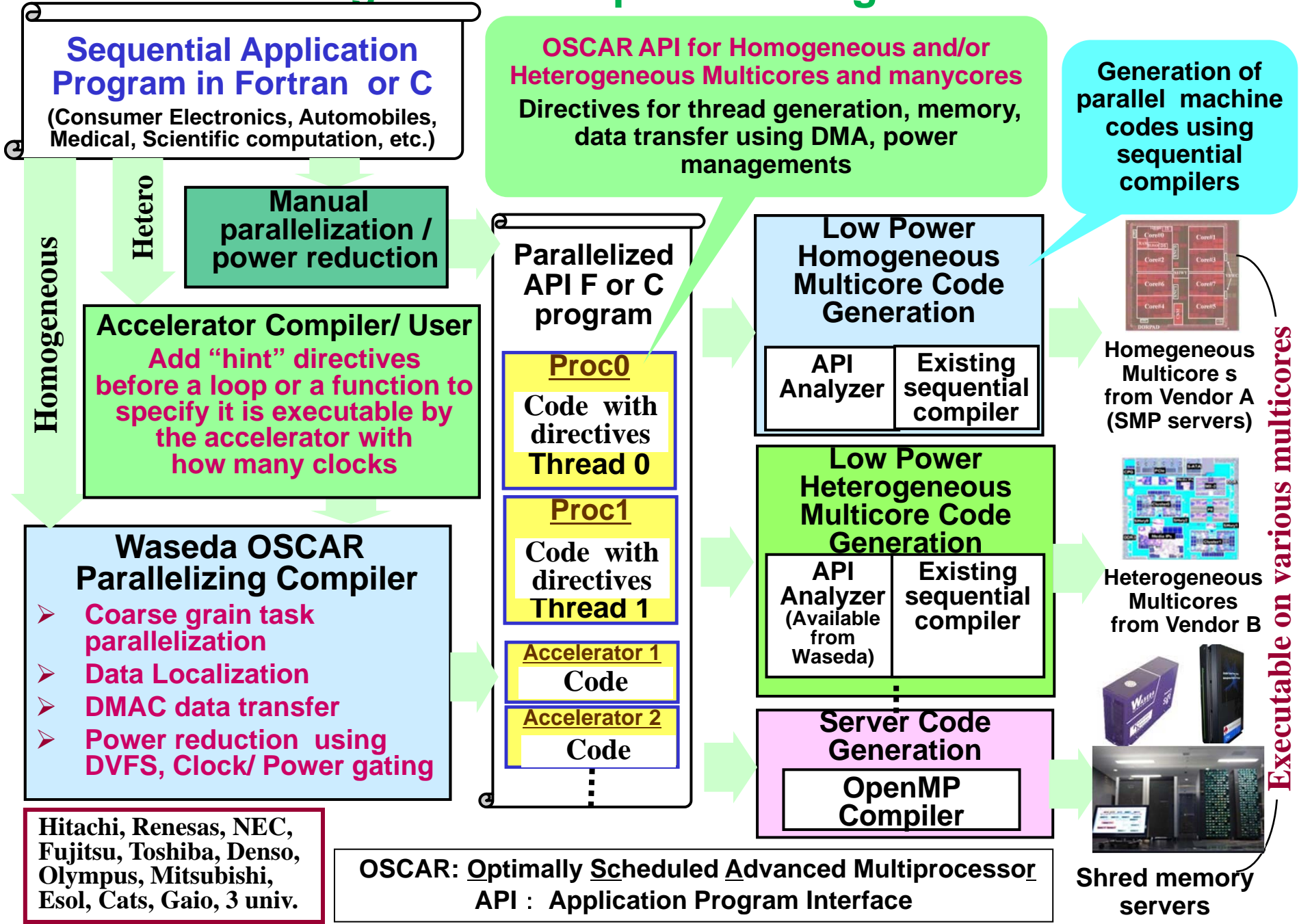Directives for thread generation, memory, data transfer using DMA, power managements

Generation of parallel machine codes using sequential compilers

Hetero

Homogeneous

Manual parallelization / power reduction

Accelerator Compiler/ User
Add "hint" directives before a loop or a function to specify it is executable by the accelerator with how many clocks

Parallelized API F or C program

Proc0
Code with directives
Thread 0

Proc1
Code with directives
Thread 1

Accelerator 1
Code

Accelerator 2
Code

Waseda OSCAR Parallelizing Compiler
- Coarse grain task parallelization
- Data Localization
- DMAC data transfer
- Power reduction using DVFS, Clock/ Power gating

Low Power Homogeneous Multicore Code Generation

| API Analyzer | Existing sequential compiler |

Low Power Heterogeneous Multicore Code Generation

| API Analyzer (Available from Waseda) | Existing sequential compiler |

Server Code Generation

| OpenMP Compiler |

Homegeneous Multicore s from Vendor A (SMP servers)

Heterogeneous Multicores from Vendor B

Shred memory servers

Executable on various multicores

Hitachi, Renesas, NEC, Fujitsu, Toshiba, Denso, Olympus, Mitsubishi, Esol, Cats, Gaio, 3 univ.

OSCAR: Optimally Scheduled Advanced Multiprocessor
API : Application Program Interface

Automatic Pallalelization Tool of MATLAB/Simulink:
OSCAR Tech "OSCARator" https://www.oscartech.jp/en/

- **OSCARator is a simulation accelerator of MATLAB/Simulink on multicore processor**
  - based on "OSCAR Compiler" Automatic Parallelization Technology developed by Kasahara and Kimura Lab. Waseda University
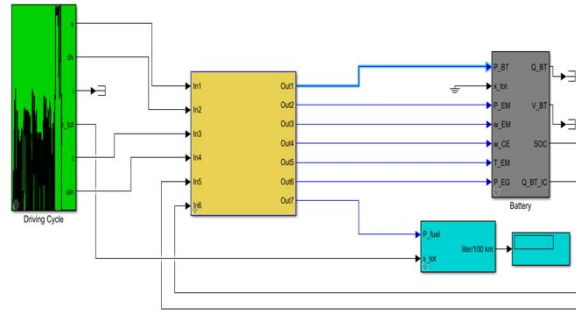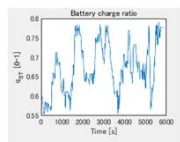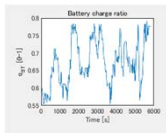
Original Simulink Model

make a "Subsystem" with blocks which you want to accelerate
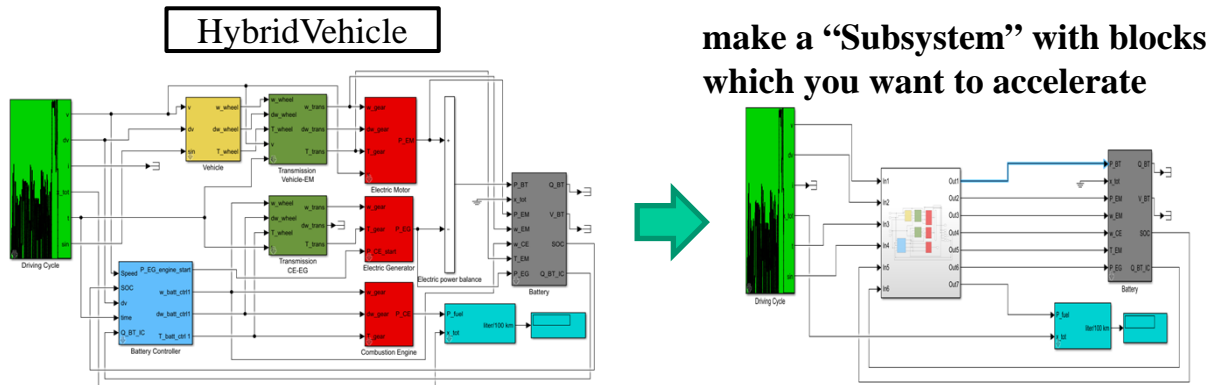
Start OSCARator from right click menu, OSCARator will automatically configure settings.
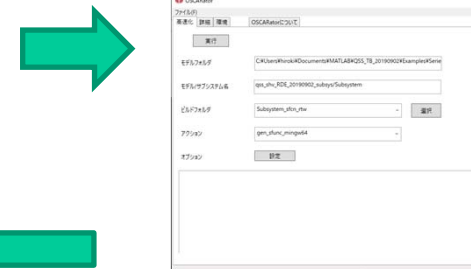
New Accelerated Simulink Model

Same Result and
Shorter Simulation Time

<FULLY AUTOMATIC>
- Simulink Coder C-Code Generation
- Automatic Parallelization
- S-Function MEX Build
- Replacing Subsystem with S-Function Block

MEX: Dynamically linked subroutine executed in the MATLAB environment.

Speedup of Simulink Models by OSCARator on 4 cores Intel Core i5 Processor

https://www.oscartech.jp/en/

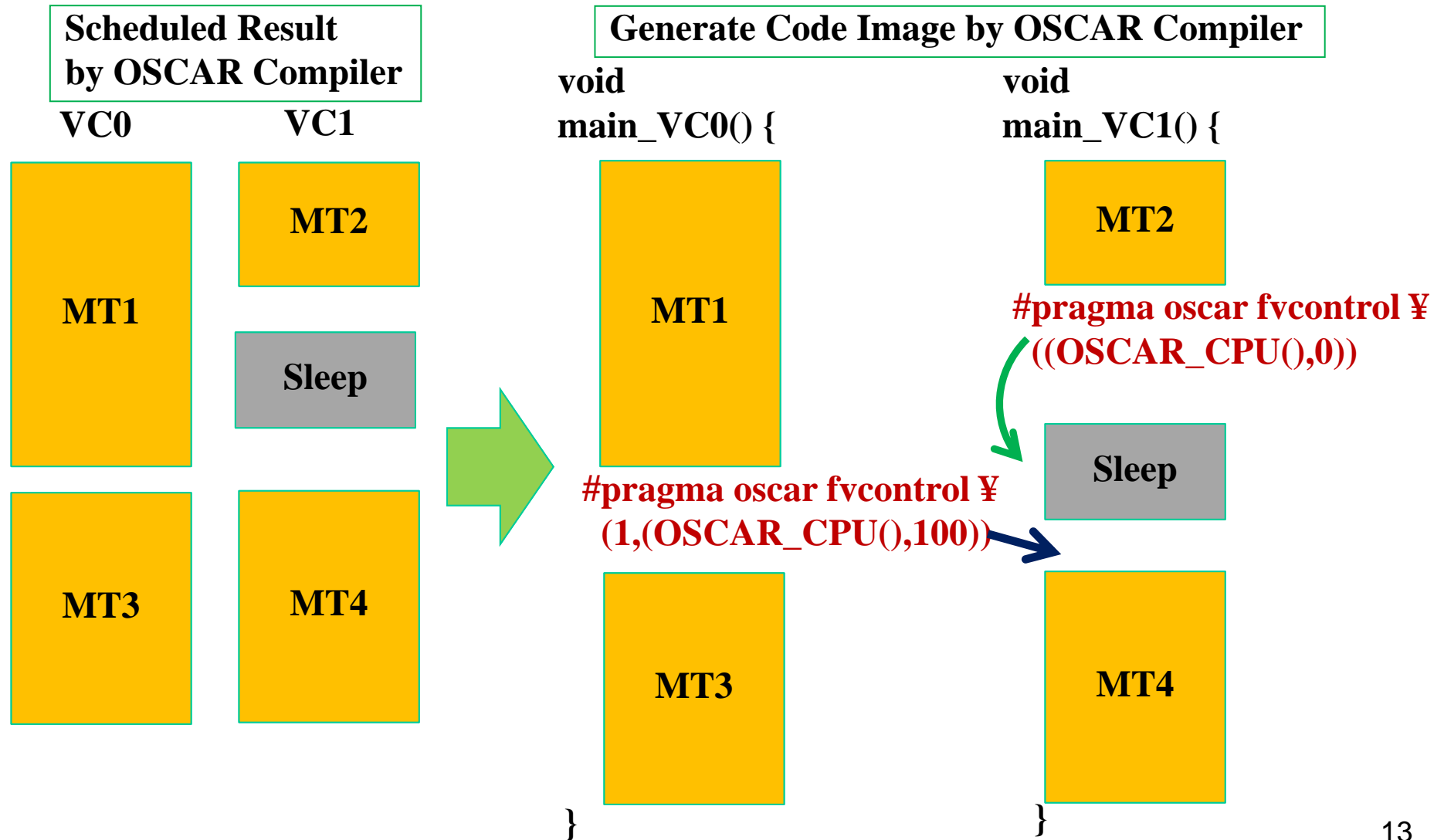**6.51 times** speed up on 4 cores against 1 core MATLAB Accerelator Mode for VesselExtraction
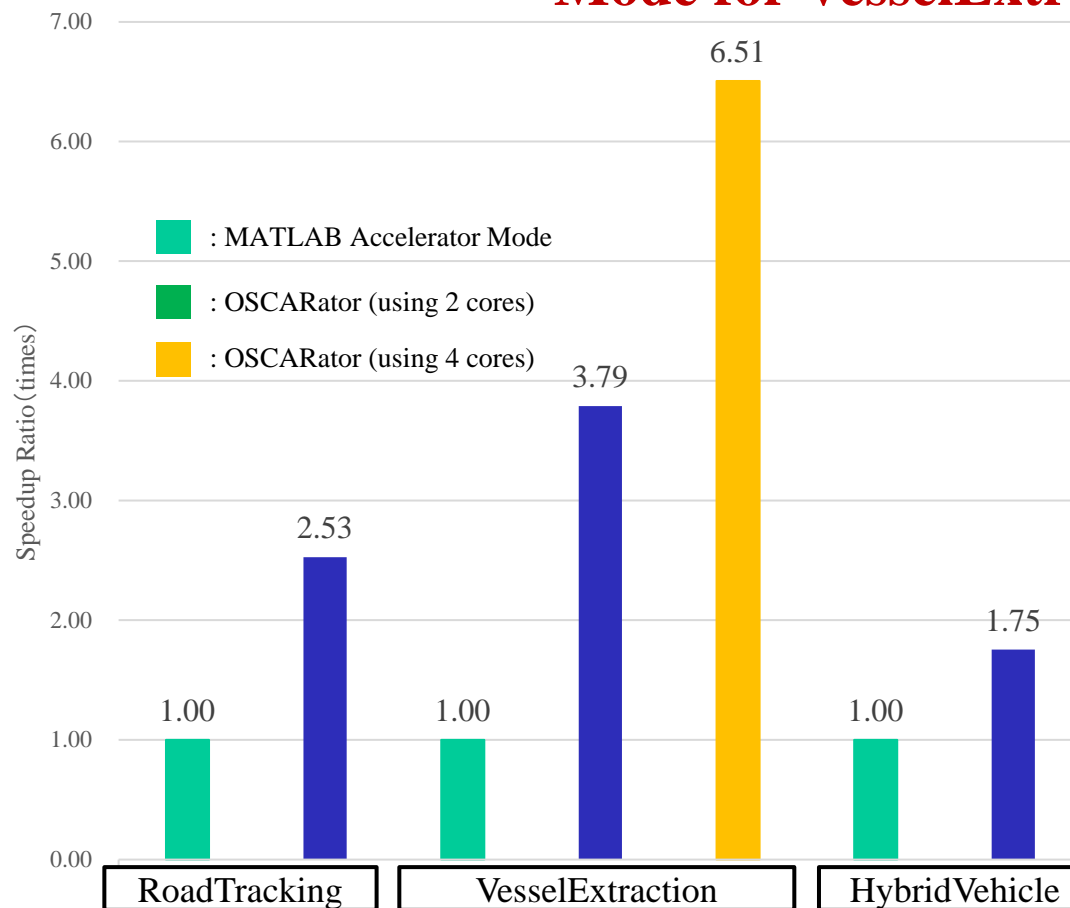
Intel Core i5 7400T 2.4GHz (4 cores)
16GB (SODIMM 2400MHz)
Windows 10 Pro (1903)
MATLAB R2019a Update 5
MinGW GCC 6.3

Legend:
- : MATLAB Accelerator Mode
- : OSCARator (using 2 cores)
- : OSCARator (using 4 cores)

Y-axis: Speedup Ratio (times), 0.00 to 7.00

RoadTracking: 1.00, 2.53
VesselExtraction: 1.00, 3.79, 6.51
HybridVehicle: 1.00, 1.75

- RoadTracking
  - from Computer Vision Toolbox
  - https://jp.mathworks.com/help/vision/examples/color-based-road-tracking.html
- VesselExtraction
  - from MATLAB Central
  - modified for Simulink Model
  - https://www.mathworks.com/matlabcentral/fileexchange/24990-retinal-blood-vessel-extraction
- HybridVehicle
  - Hybrid Vehicle Powertrain
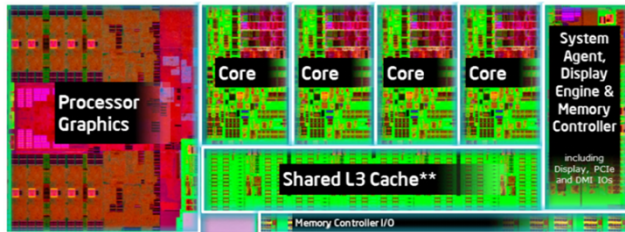 - developed by Kusaka Lab. Waseda University
  - http://www.f.waseda.jp/jin.kusaka/

(Compared with MATLAB Accelerator Mode Simulation)

Low-Power Optimization with OSCAR API

Scheduled Result by OSCAR Compiler

VC0   VC1

MT1

MT2

Sleep

MT3   MT4

Generate Code Image by OSCAR Compiler

void
main_VC0() {

MT1

#pragma oscar fvcontrol ¥
(1,(OSCAR_CPU(),100))

MT3

}

void
main_VC1() {

MT2

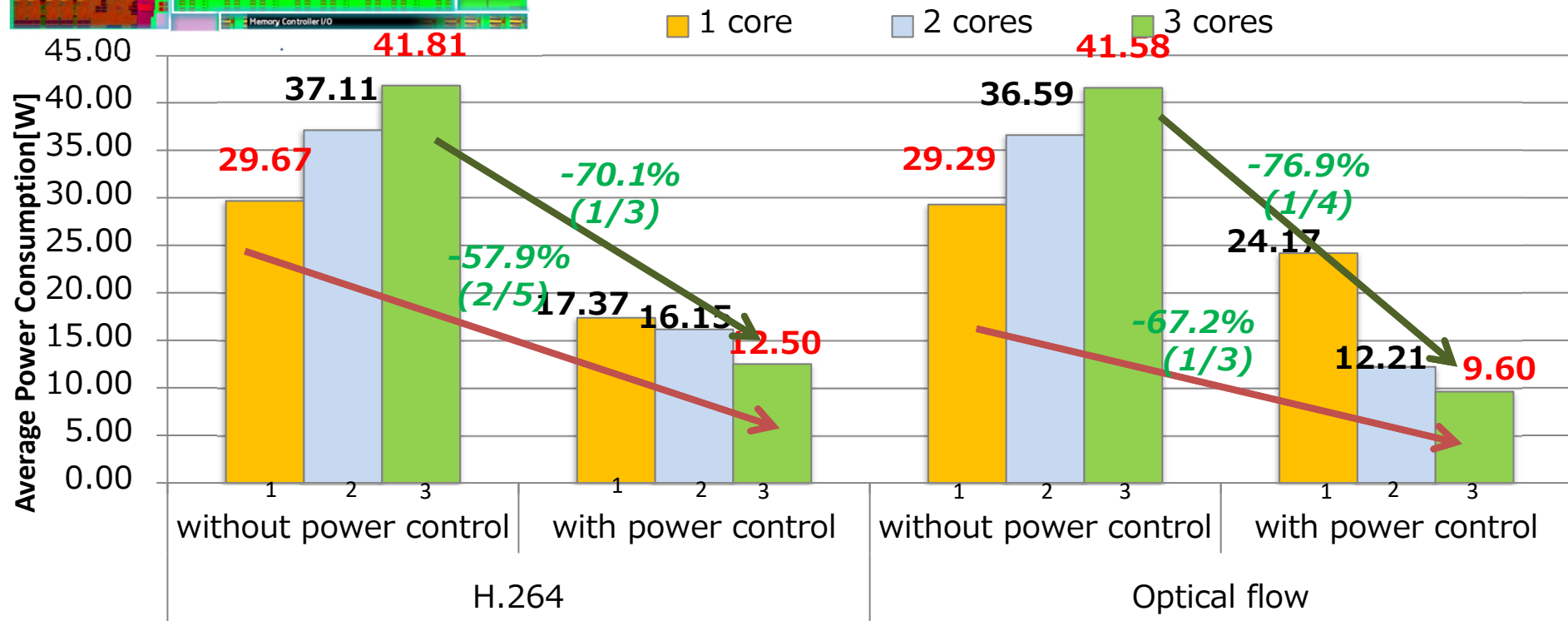#pragma oscar fvcontrol ¥
((OSCAR_CPU(),0))

Sleep

MT4

}

13

Automatic Power Reuction on Intel Haswell
H.264 decoder & Optical Flow　(3cores)

H81M-A,　Intel Core i7 4770k

Quad core,　3.5GHz～0.8GHz

Legend: ■ 1 core　■ 2 cores　■ 3 cores

Average Power Consumption[W]

H.264:
- without power control: 29.67, 37.11, 41.81
- with power control: 17.37, 16.15, 12.50
- -70.1% (1/3)
- -57.9% (2/5)

Optical flow:
- without power control: 29.29, 36.59, 41.58
- with power control: 24.17, 12.21, 9.60
- -76.9% (1/4)
- -67.2% (1/3)

Power for 3cores was reduced to 1/3～1/4 against without software power control

Power for 3cores was reduced to 2/5～1/3 against ordinary 1core execution

14

OSCAR Heterogeneous Multicore

DTU
- Data Transfer Unit

LPM
- Local Program Memory

LDM
- Local Data Memory

DSM
- Distributed Shared Memory

CSM
- Centralized Shared Memory
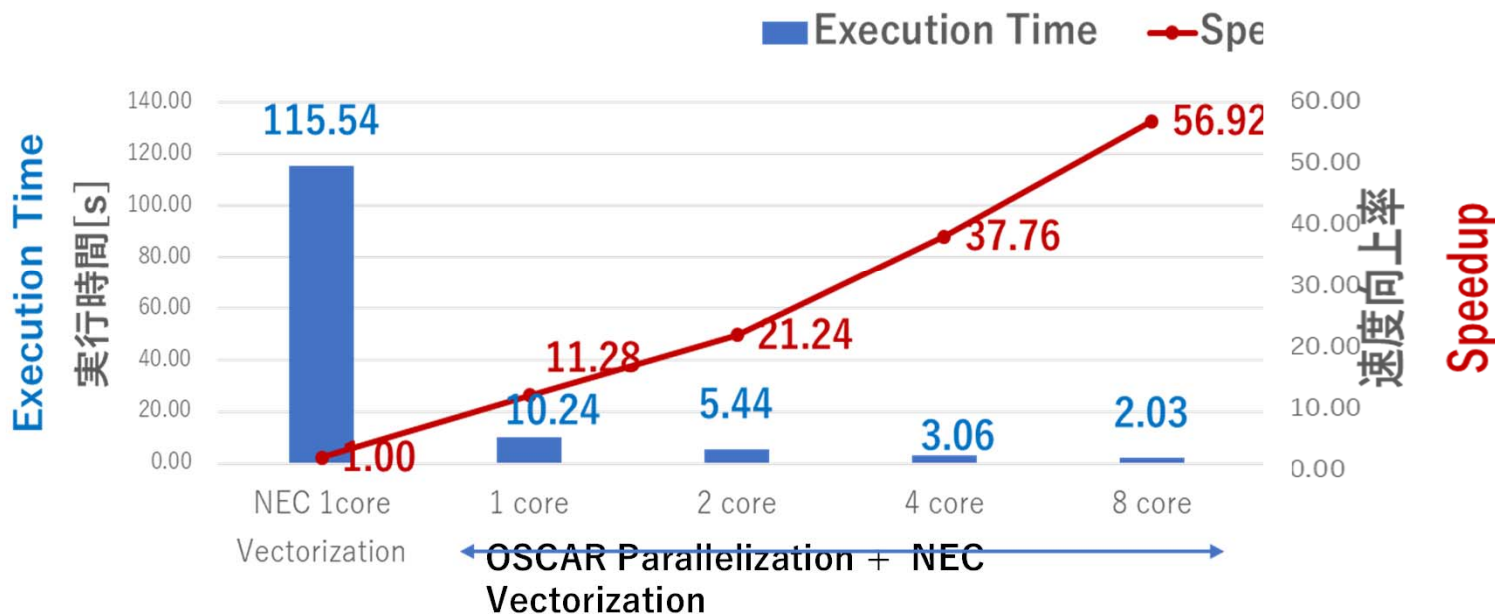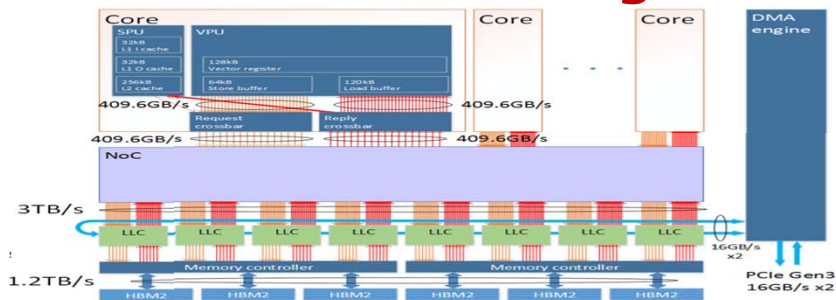
FVR
- Frequency/Voltage Control Register

15
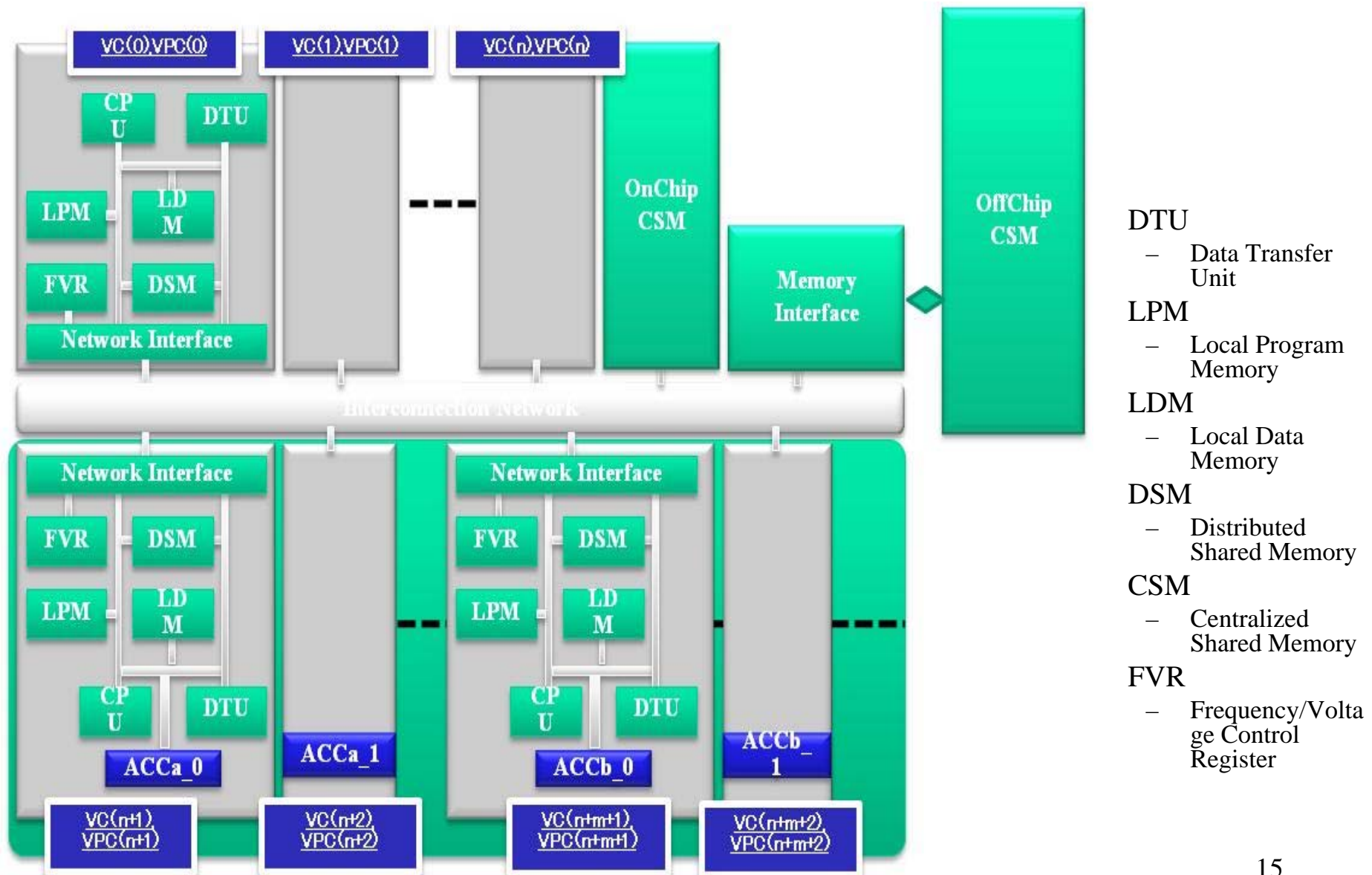
An Image of Static Schedule for Heterogeneous Multi-core with Data Transfer Overlapping and Power Control
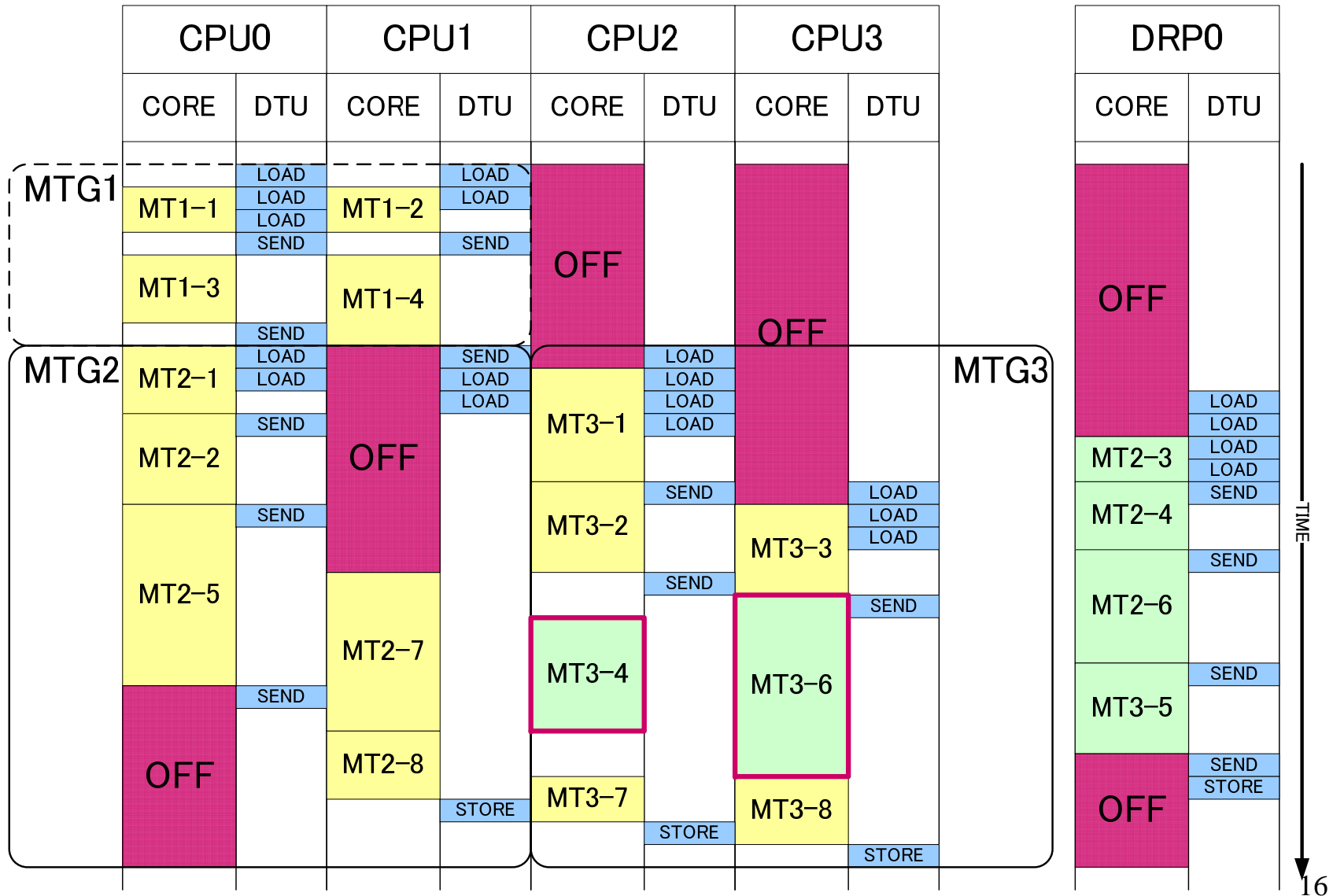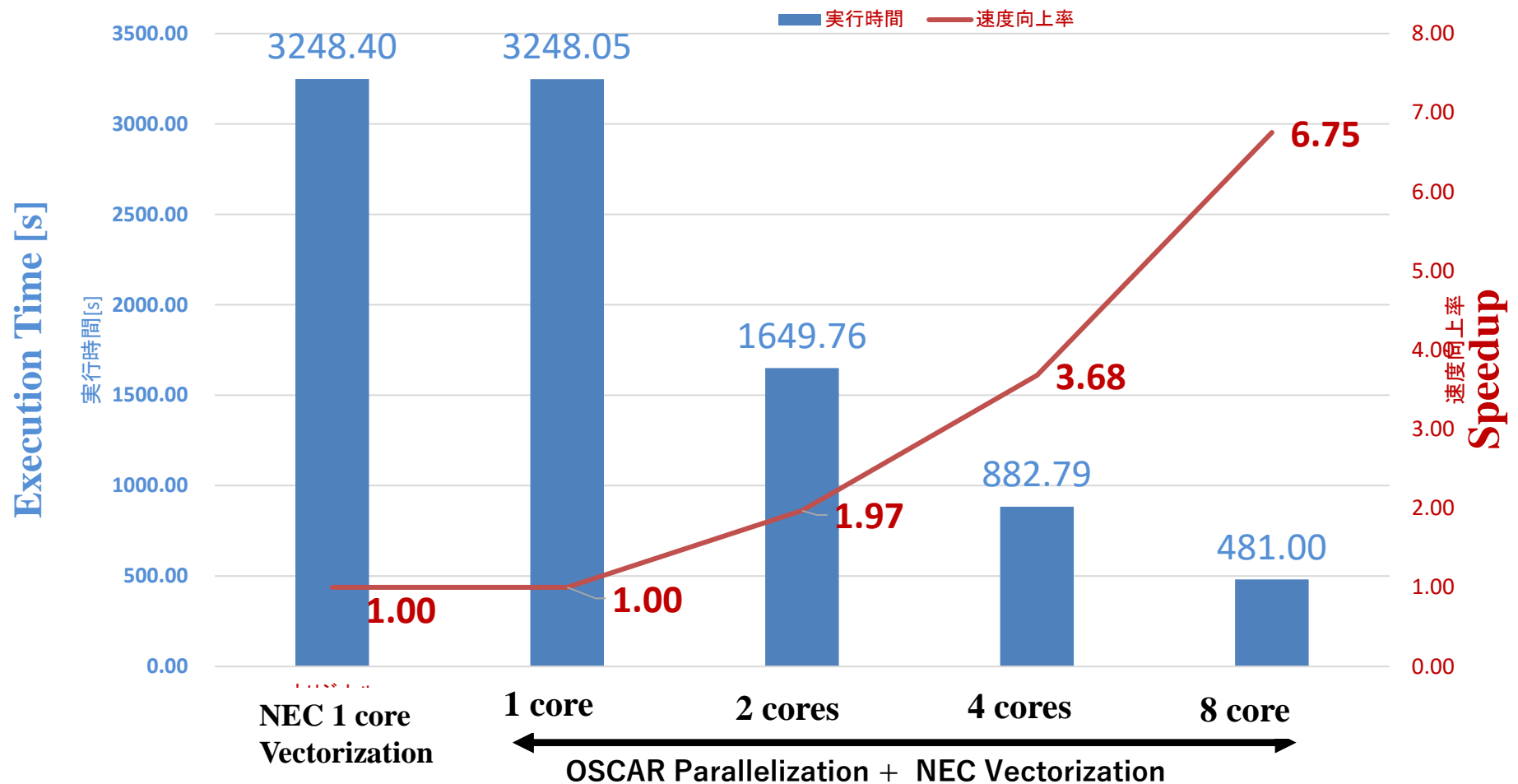
Speedup of NPB/CG by OSCAR Compiler on NEC SX-Aurora TSUBASA A100-1 8 cores 10C VE
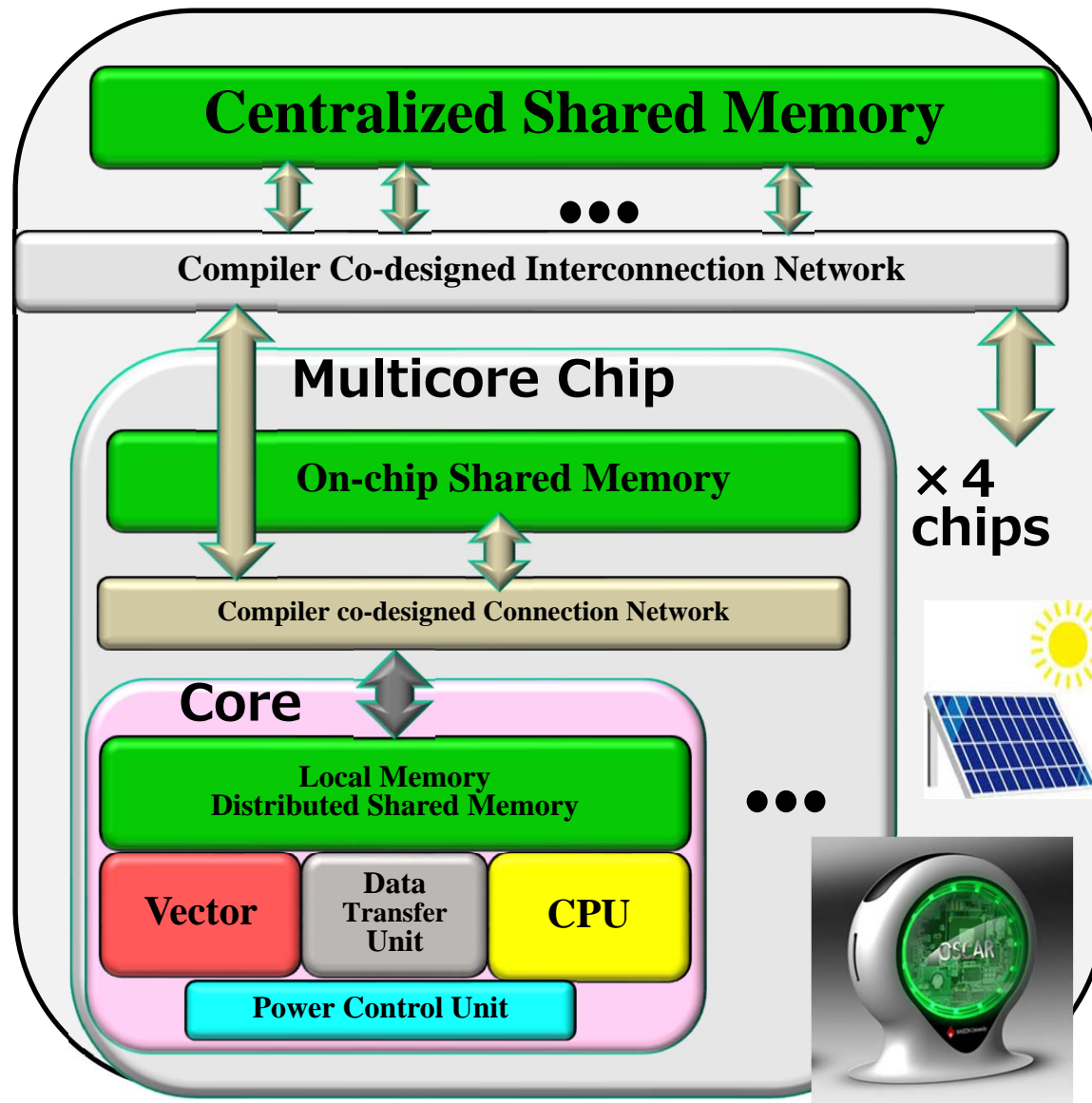
57 times speed up for 8 core Parallelization by OSCAR Compiler & NEC Vectorization against NEC 1 core Vectorization

Speedup of **NPB/BT** by OSCAR Compiler on NEC SX-Aurora TSUBASA A100-1 8 cores 10C VE

OSCAR Vector Multicore and Compiler for Embedded to Severs with OSCAR Technology

Centralized Shared Memory

Compiler Co-designed Interconnection Network

Multicore Chip

On-chip Shared Memory

× 4 chips

Compiler co-designed Connection Network

Core

Local Memory
Distributed Shared Memory

| Vector | Data Transfer Unit | CPU |

Power Control Unit

Target:

➢ **Solar Powered**

➢ **Compiler power reduction.**

➢ Fully automatic parallelization and vectorization including local memory management and data transfer.

Vector Accelerator

Features
- Attachable for any CPUs (Intel, ARM, IBM)
- Data driven initiation by sync flags
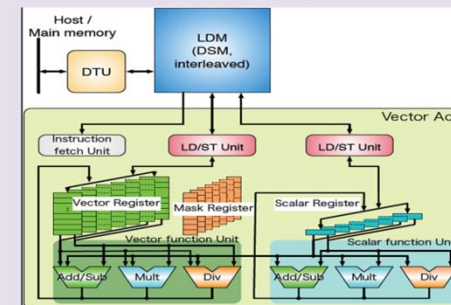
Function Units [tentative]
- **Vector Function Unit**
  - 8 double precision ops/clock
  - 64 characters ops/clock
  - Variable vector register length
  - Chaining LD/ST & Vector pipes
- Scalar Function Unit

Registers[tentative]
- Vector Register 256Bytes/entry, 32entry
- Scalar Register 8Bytes/entry
- Floating Point Register 8Bytes/entry
- Mask Register 32Bytes/entry
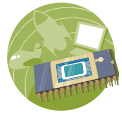
Future Multicore Products with Automatic Parallelizing Compiler

Next Generation Automobiles

- Safer, more comfortable, energy efficient, environment friendly
- Cameras, radar, car2car communication, internet information integrated brake, steering, engine, moter control

Smart phones

-From everyday recharging to less than once a week
- Solar powered operation in emergency condition
- Keep health

Advanced medical systems

Cancer treatment,
Drinkable inner camera
- Emergency solar powered
- No cooling fun, No dust , clean usable inside OP room

Personal / Regional Supercomputers

Solar powered with more than 100 times power efficient : FLOPS/W
- Regional Disaster Simulators saving lives from tornadoes, localized heavy rain, fires with earth quakes