Hironori Kasahara

IEEE Computer Society President Elect 2017, President 2018
Professor, Dept. of Computer Science & Engineering
Director, Advanced Multicore Processor Research Institute
Waseda University, Tokyo, Japan
URL: http://www.kasahara.cs.waseda.ac.jp/

1980 BS, 82 MS, 85 Ph.D. , Dept. EE, Waseda Univ.
1985 Visiting Scholar: U. of California, Berkeley
1986 Assistant Prof., 1988 Associate Prof., 1997 Prof., Dept. of EECE, Waseda Univ. Now Dept. of Computer Sci. & Eng.

1989-90 Research Scholar: U. of Illinois, Urbana-Champaign, Center for Supercomputing R&D

1987 IFAC World Congress Young Author Prize
1997 IPSJ Sakai Special Research Award
2005 STARC Academia-Industry Research Award
2008 LSI of the Year Second Prize
2008 Intel AsiaAcademic Forum Best Research Award
2010 IEEE CS Golden Core Member Award
2014 Minister of Edu., Sci. & Tech. Research Prize, 2015 IPSJ Fellow
2017 IEEE Fellow, Member of The Engineering Academy of Japan,
    Science Council of Japan, IEEE Eta-Kappa-Nu

Reviewed Papers: 214, Invited Talks: 145, Published Unexamined Patent Application:59 (Japan, US, GB, China Granted Patents: 30), Articles in News Papers, Web News, Medias incl. TV etc.: 572

Committees in Societies and Government   245
IEEE Computer Society President 2018, BoG(2009-14), Multicore STC Chair (2012-), Japan Chair (2005-07), IPSJ Chair: HG for Mag. & J. Edit, Sig. on ARC.
【METI/NEDO】 Project Leaders: Multicore for Consumer Electronics, Advanced Parallelizing Compiler, Chair: Computer Strategy Committee【Cabinet Office】 CSTP Supercomputer Strategic ICT PT, Japan Prize Selection Committees, etc.
【MEXT】Info. Sci. & Tech. Committee, Supercomputers (Earth Simulator, HPCI Promo., Next Gen. Supercomputer K) Committees, etc.

Hironori Kasahara Voted 2017 IEEE Computer Society President-Elect

LOS ALAMITOS, Calif., 30 September 2016 — **Hironori Kasahara**, a Professor of Computer Science at Waseda University in Tokyo, and Director of the Advanced Multicore Research Institute, has been voted **IEEE Computer Society 2017 President-Elect.**

Kasahara is a former member of the IEEE-CS Board of Governors, has served as chair of the IEEE-CS Multicore STC and CS Japan Chapter, and board member of the IEEE Tokyo Section. Kasahara will serve as the 2018 IEEE CS President for a one-year term beginning 1 January 2018. Kasahara garnered 3,278 votes, compared with 2,804 votes cast for Hausi A. Müller, a Professor of Computer Science and Associate Dean of Research, Faculty of Engineering at University of Victoria, Canada, and a member of IEEE-CS Board of Governors.

The President oversees IEEE-CS programs and operations and is a nonvoting member of most IEEE-CS program boards and committees. The 2016 election had a 12.69% turnout, with 6,357 ballots cast. The turnout was higher than the 2015 election with and 12.68% turnout (6,239 ballots cast) and the 2014 election with a 12.66% turnout (6,728 ballots cast).

2016 IEEE Computer Society Election Results

Press Release | Ballot counts

Posted 29 September 2016

Hironori Kasahara selected 2017 President-Elect (2018 President)

Hironori Kasahara has served as a chair or member of 225 society and government committees, including a member of the CS Board of Governors; chair of CS Multicore STC and CS Japan chapter; associate editor of IEEE Transactions on Computers; vice PC chair of the 1996 ENIAC 50th Anniversary International Conference on Supercomputing; general chair of LCPC; PC member of SC, PACT, PPoPP, and ASPLOS; board member of IEEE Tokyo section; and member of the Earth Simulator committee.

He received a PhD in 1985 from Waseda University, Tokyo, joined its faculty in 1986, and has been a professor of computer science since 1997 and a director of the Advanced Multicore Research Institute since 2004. He was a visiting scholar at University of California, Berkeley, and the University of Illinois at Urbana–Champaign's Center for Supercomputing R&D.

Kasahara received the CS Golden Core Member Award, IFAC World Congress Young Author Prize, IPSJ Fellow and Sakai Special Research Award, and the Japanese Minister's Science and Technology Prize. He led Japanese national projects on parallelizing compilers and embedded multicores, and has presented 210 papers, 132 invited talks, and 27 patents. His research has appeared in 520 newspaper and Web articles.
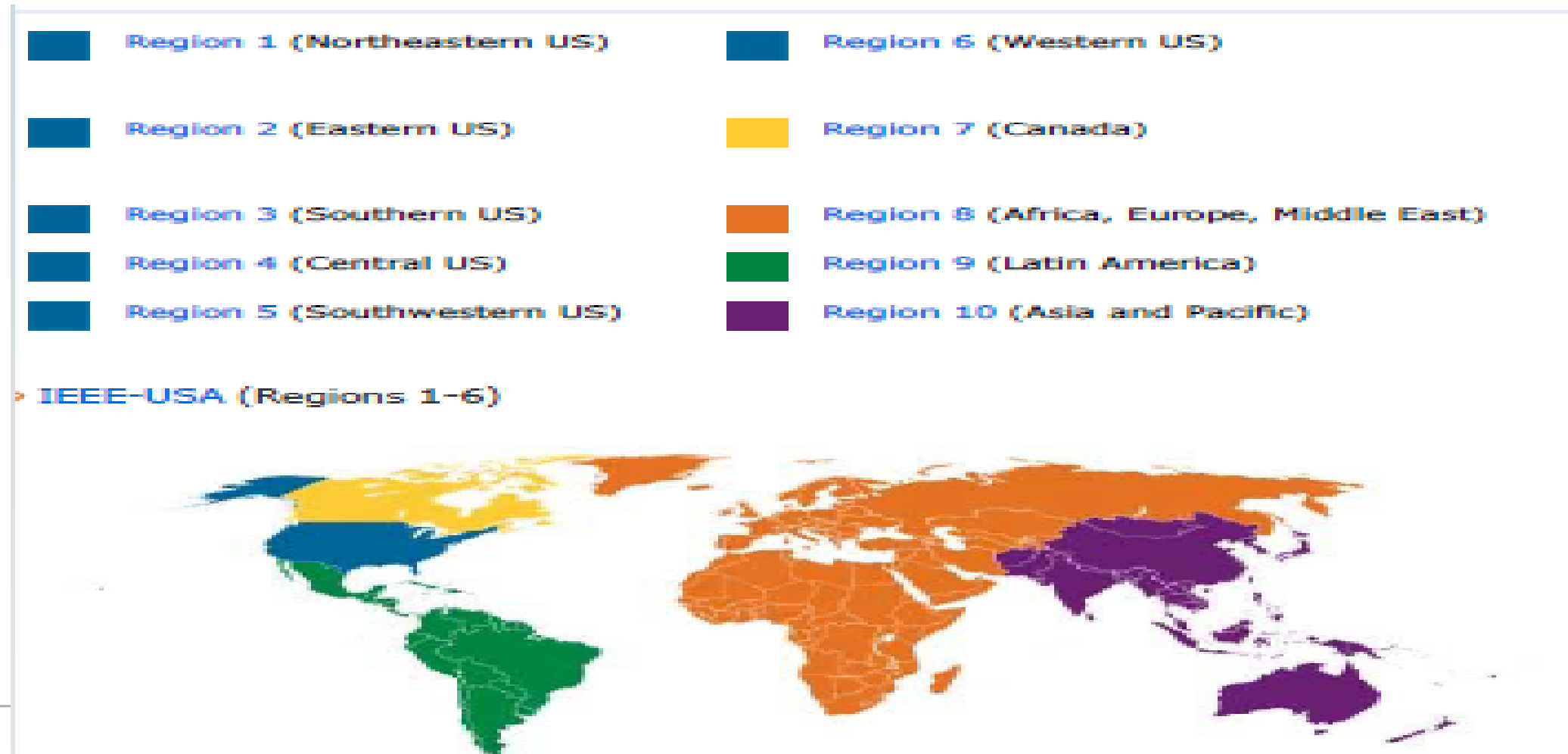
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IEEE Computer Society BoG
(Board of Governors) Feb.1, 2017

IEEE Computer Society

60,000+ members, **volunteer-led organization,**
200 technical conferences, industry-oriented "**Rock Stars**" ,
17 scholarly journals and **13 magazines, awards program,**
Digital Library with more than 550,000 articles and papers ,
400 local and regional chapters, 40 technical committees,

■ Region 1 (Northeastern US)	■ Region 6 (Western US)	
■ Region 2 (Eastern US)	■ Region 7 (Canada)	
■ Region 3 (Southern US)	■ Region 8 (Africa, Europe, Middle East)	
■ Region 4 (Central US)	■ Region 9 (Latin America)	
■ Region 5 (Southwestern US)	■ Region 10 (Asia and Pacific)	

> IEEE-USA (Regions 1-6)

Collaboration of SEMICON and IEEE COMPSAC: 2019 Collocation in San Francisco

IEEE computer society

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COMPSAC 2018
Tokyo, Japan
July 23-27
Staying Smarter in a Smartening World

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Report on COMPSAC 2017 by Sorel Reisman, COMPSAC Standing Committee Chair

COMPSAC 2018: Staying Smarter in a Smartening World
Tokyo, Japan - July 23-27

CFP (pdf)

Computer technologies are producing profound changes in society. Emerging developments in areas such as Deep Learning, supported by increasingly powerful and increasingly miniaturized hardware, are beginning to be deployed in architectures, systems, and applications that are redefining the relationships between humans and technology. As this happens, humans are relinquishing their roles as masters of technology to partnerships wherein autonomous, computer-driven devices become our assistants. What are the technologies enabling these changes? How far can these partnerships go? What will be our future as we deploy more and more "things" on the Internet of Things – to create smart cities, smart vehicles, smart hospitals, smart homes, smart clothes, etc.? Will humans simply become IoT devices in these scenarios and if so, what will be the social, cultural, and economic challenges arising from these developments? What are the technical challenges to making this all happen – for example, in terms of technologies such as Big Data, Cloud, Fog, Edge Computing, mobile computing, and pervasive computing in general? What will be the role of the 'user' as the 21st Century moves along?

COMPSAC 2018 is organized as a tightly integrated union of symposia, each of which will focus on technical aspects related to the "smart" theme of the conference. The technical program will include keynote addresses, research papers, industrial case studies, fast abstracts, a doctoral symposium, poster sessions, and workshops and tutorials on emerging and important topics related to the conference theme. A highlight of the conference will be plenary and specialized panels that will address the technical challenges facing technologists who are developing and deploying these smart systems and applications. Panels will also address cultural and societal challenges for a society whose members must continue to learn to live, work, and play in the environments the technologies produce. Authors are invited to submit original, unpublished research work, as well as industrial practice reports. Simultaneous submission to other publication venues is not permitted. All submissions must adhere to IEEE Publishing Policies, and all will be vetted through the IEEE CrossCheck Portal.

Conference venue: Hitotsubashi Hall and National Institute of Informatics, National Center of Sciences
Accomodation: KKR Hotel Tokyo
Conference reception - July 24: Gakushikaikan
Conference banquet - July 25: RIHGA Royal Hotel Tokyo (TBD)

Local Chairs
Hironori Washizaki, WasedaUniv.

Nobukazu Yoshioka, NII

COMPSAC Organizers
Standing Committee Chair
IEEE CS President 2011
Sorel Reisman,
California State Univ.

Steering Committee Chair
Sheikh Iqbal Ahamed,
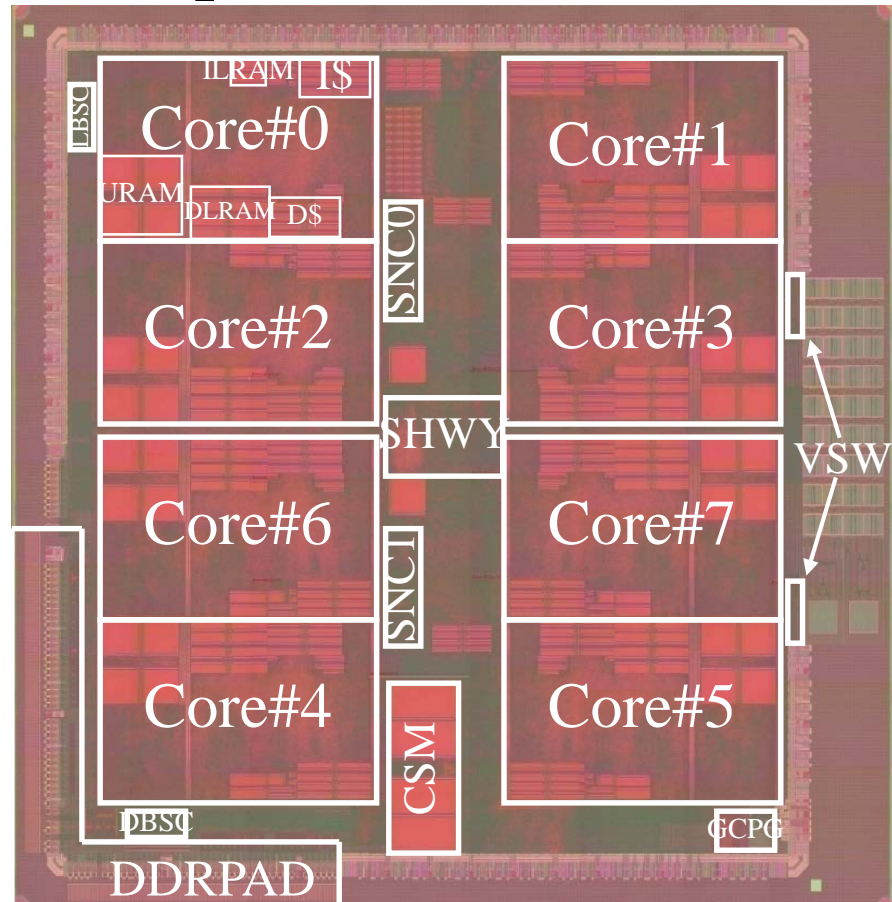Marquette Univ.

General Chairs
Shinichi Honiden,
NII, Japan

Roger U. Fujii,
IEEE CS President 2016

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Multicores for Performance and Low Power

Power consumption is one of the biggest problems for performance scaling from smartphones to cloud servers and supercomputers ("K" more than 10MW).

IEEE ISSCC08: Paper No. 4.5, M.ITO, … H. Kasahara, "An 8640 MIPS SoC with Independent Power-off Control of 8 CPUs and 8 RAMs by an Automatic Parallelizing Compiler"

Power $\propto$ Frequency * Voltage^2
(Voltage $\propto$ Frequency)
$\Rightarrow$ Power $\propto$ Frequency^3

If Frequency is reduced to 1/4 (4GHz$\rightarrow$1GHz),
Power is reduced to 1/64 and
Performance falls down to 1/4 .
<Multicores>
If 8cores are integrated on a chip,
Power is still 1/8 and
Performance becomes 2 times.

Parallel Soft is important for scalable performance

Just more cores don't give us speedup

➢ **Development cost & period of parallel software are getting a bottleneck of development of embedded systems, eg. IoT, Automobile**

Fujitsu M9000 SPARC Multicore Server

Earthquake wave propagation simulation GMS developed by National Research Institute for Earth Science and Disaster Resilience (NIED)

legend: ■ original (sun studio) ■ proposed method

Y-axis: Speed-up ratio against original sequential execution

X-axis: 1pe, 32pe, 64pe, 128pe

Values: 1.0 / 1.0 (1pe); 1.0 / 54.2 (32pe); 1.0 / 114.2 (64pe); 0.9 / 211.0 (128pe)
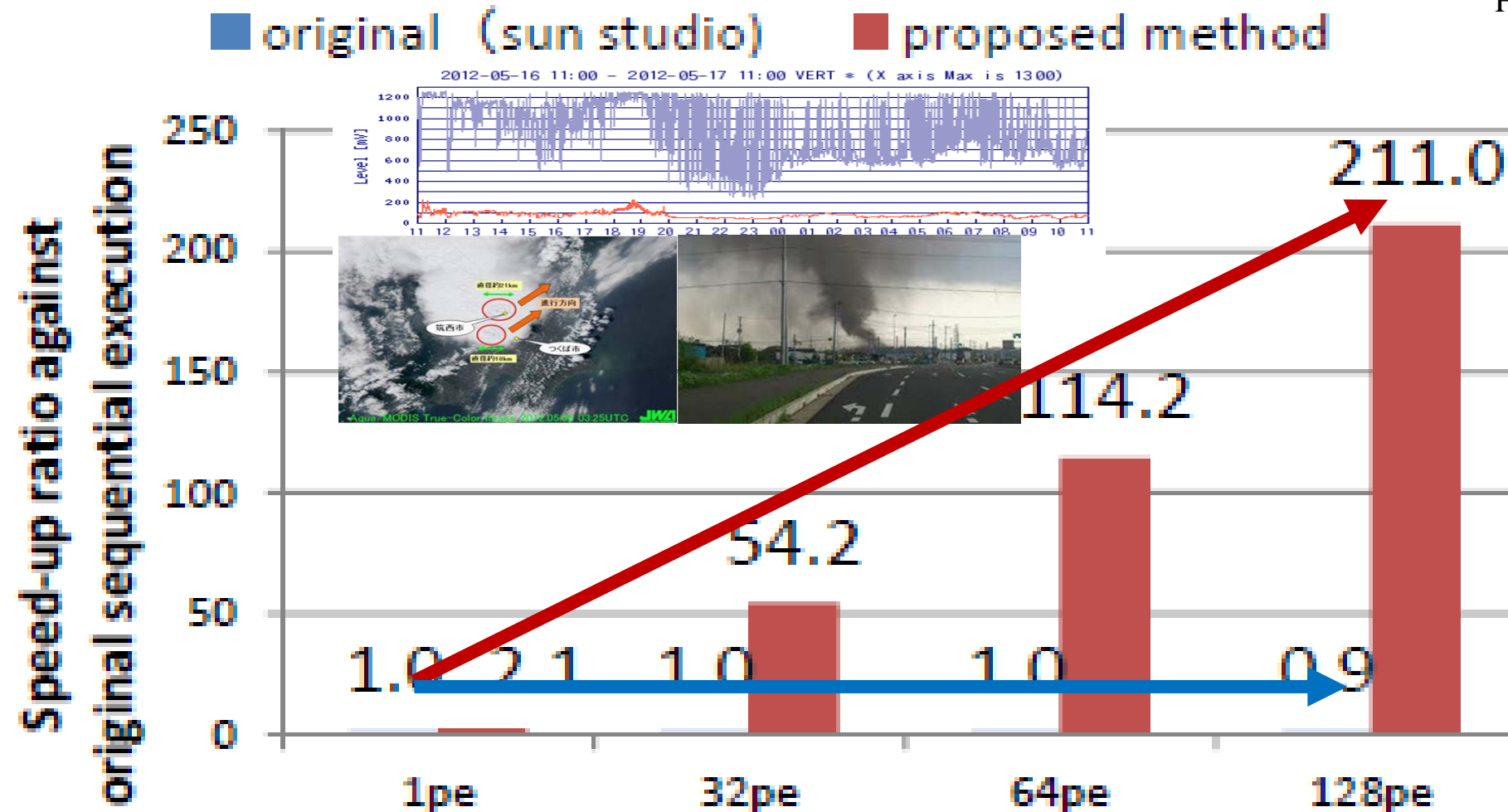
OSCAR Compiler gives us 211 times speedup with 128 cores

Commercial compiler gives us 0.9 times speedup with 128 cores (slow-downed against 1 core)

➢ **Parallelizing compiler available on the market gave us no speedup against execution time on 1 core on 64 cores**

➢ **OSCAR parallelizing compiler gave us 211 times speedup with 128cores against execution time with 1 core using commercial compiler**

Power Reduction of MPEG2 Decoding to 1/4 on 8 Core Homogeneous Multicore RP-2 by OSCAR Compiler
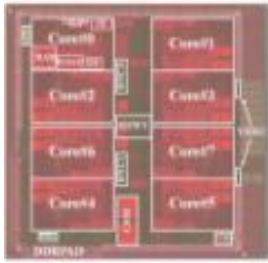
MPEG2 Decoding with 8 CPU cores

Without Power Control
（Voltage：1.4V)
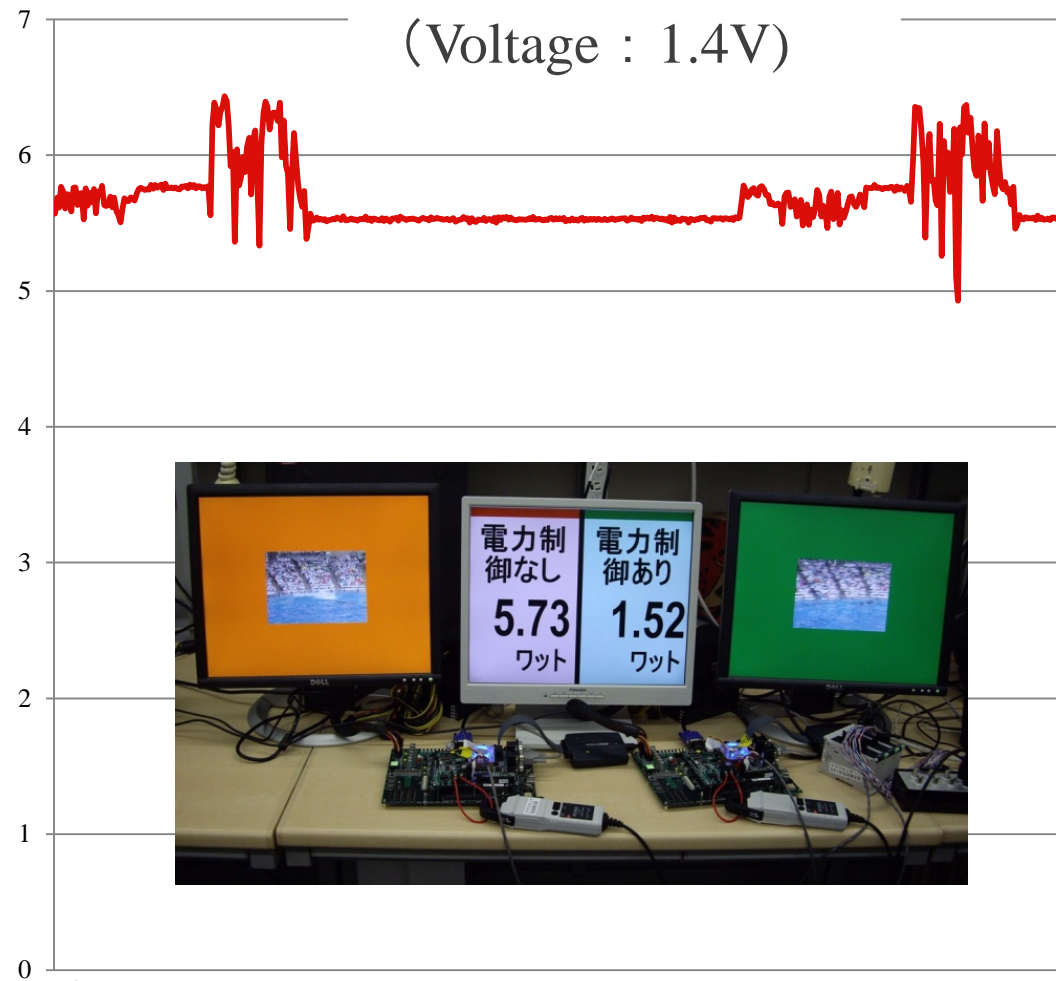
With Power Control
（Frequency,
Resume Standby:
Power shutdown &
Voltage lowering 1.4V-1.0V)
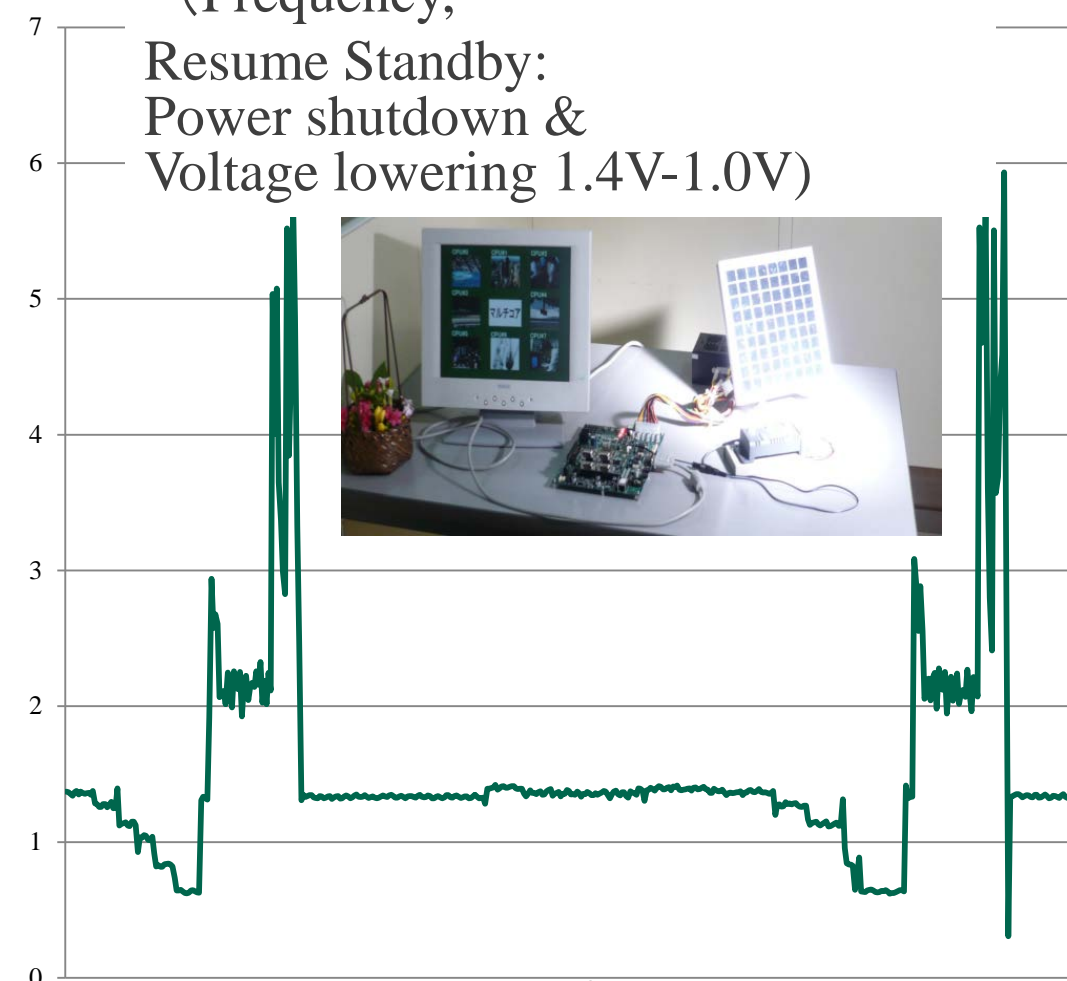
Avg. Power

73.5% Power Reduction

Avg. Power

5.73 [W]

1.52 [W]

Demo of NEDO Multicore for Real Time Consumer Electronics at the Council of Science and Engineering Policy on April 10, 2008

第74回総合科学技術会議 【平成20年4月10日】

第74回総合科学技術会議の様子(1)
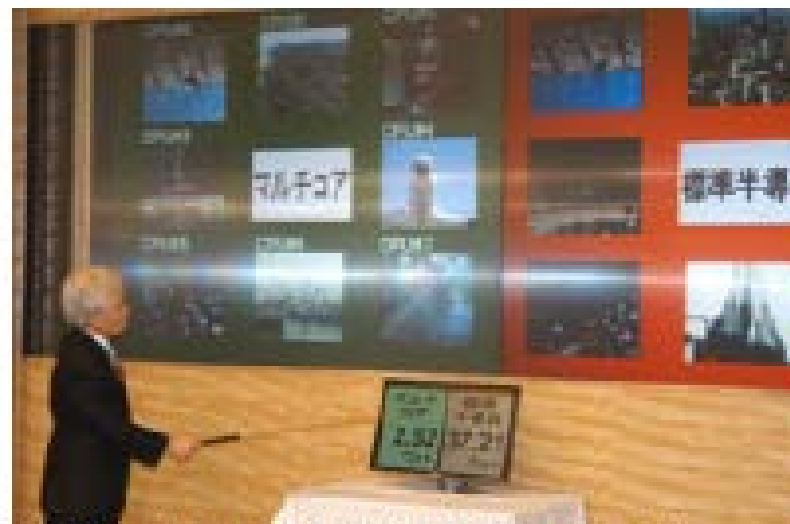
第74回総合科学技術会議の様子(2)

第74回総合科学技術会議の様子(3)

第74回総合科学技術会議の様子(4)

CSTP Members
Prime Minister:
Mr. Y. FUKUDA

Minister of State for Science, Technology and Innovation Policy:
Mr. F. KISHIDA

Chief Cabinet Secretary:
Mr. N. MACHIMURA

Minister of Internal Affairs and Communications :
Mr. H. MASUDA

Minister of Finance :
Mr. F. NUKAGA

Minister of Education, Culture, Sports, Science and Technology:
Mr. K. TOKAI

Minister of Economy,Trade and Industry:
Mr. A. AMARI

Waseda Univ. Green Computing Systems R&D Center
Supported by METI (Mar. 2011 Completion)

＜R & D Target＞

Hardware, Software, Application for Super Low-Power Manycore

➢More than 64 cores

➢Natural air cooling (No fan)
  Cool, Compact, Clear, Quiet

➢Operational by Solar Panel

<Industry, Government, Academia>

Hitachi, Fujitsu, NEC, Renesas, Olympus, Toyota, Denso, Mitsubishi, Toshiba, OSCAR Technology, etc

＜Ripple Effect＞

➢Low CO_2 (Carbon Dioxide) Emissions

➢Creation Value Added Products

➢ Automobiles, Medical, IoT, Servers

Hitachi SR16000:
  Power7 128coreSMP
Fujitsu M9000
  SPARC VII 256 core SMP

Beside Subway Waseda Station,
Near Waseda Univ. Main Campus

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OSCAR Parallelizing Compiler

To improve effective performance, cost-performance and software productivity and reduce power

Multigrain Parallelization (1991,2001,04)

coarse-grain parallelism among loops and subroutines (2000 on SMP), near fine grain parallelism among statements (1992) in addition to loop parallelism

Data Localization

Automatic data management for distributed shared memory, cache and local memory (Local Memory 1995, 2016 on RP2,Cache2001,03) Software Coherent Control (2017)

Data Transfer Overlapping (2016 partially)

Data transfer overlapping using Data Transfer Controllers (DMAs)

Power Reduction

(2005 for Multicore, 2011 Multi-processes, 2013 on ARM)

Reduction of consumed power by compiler control DVFS and Power gating with hardware supports.

88.3% Power Reduction
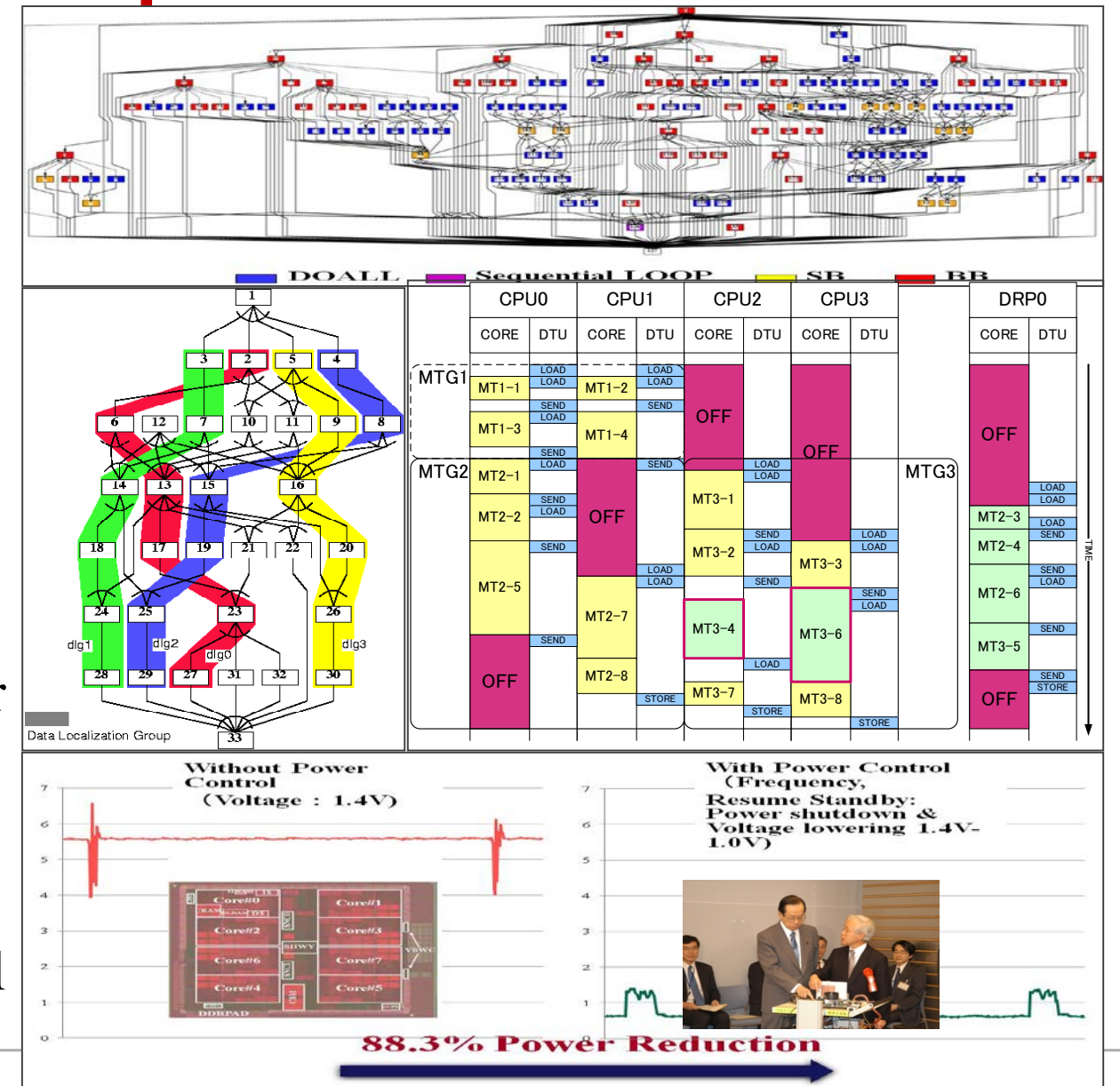
Multicore Program Development Using OSCAR API V2.0

Sequential Application   Program in Fortran or C

(IoT, Automobiles, Medical, Scientific computation, etc.)

Homogeneous

Hetero

Manual parallelization / power reduction

Accelerator Compiler/ User
Add "hint" directives
before a loop or a function to specify it is executable by the accelerator with
how many clocks

Waseda OSCAR Parallelizing Compiler

- ➤ Coarse grain task parallelization
- ➤ Data Localization
- ➤ DMAC data transfer
- ➤ Power reduction using DVFS, Clock/ Power gating

OSCAR API for Homogeneous and/or Heterogeneous Multicores and manycores
Directives for thread generation, memory, data transfer using DMA, power managements

Generation of parallel machine codes using sequential compilers

Parallelized API F or C program

Proc0
Code with directives
Thread 0

Proc1
Code with directives
Thread 1

Accelerator 1
Code

Accelerator 2
Code

Low Power Homogeneous Multicore Code Generation

API Analyzer	Existing sequential compiler

Low Power Heterogeneous Multicore Code Generation

API Analyzer (Available from Waseda)	Existing sequential compiler

Server Code Generation

OpenMP Compiler

Homegeneous Multicore s from Vendor A (SMP servers)

Heterogeneous Multicores from Vendor B

Executable on various multicores

Shred memory servers

OSCAR: Optimally Scheduled Advanced Multiprocessor
API : Application Program Interface

semi

Speedup for H.264 and Optical Flow on ARM Cortex-A9 Android 3 cores by OSCAR Compiler
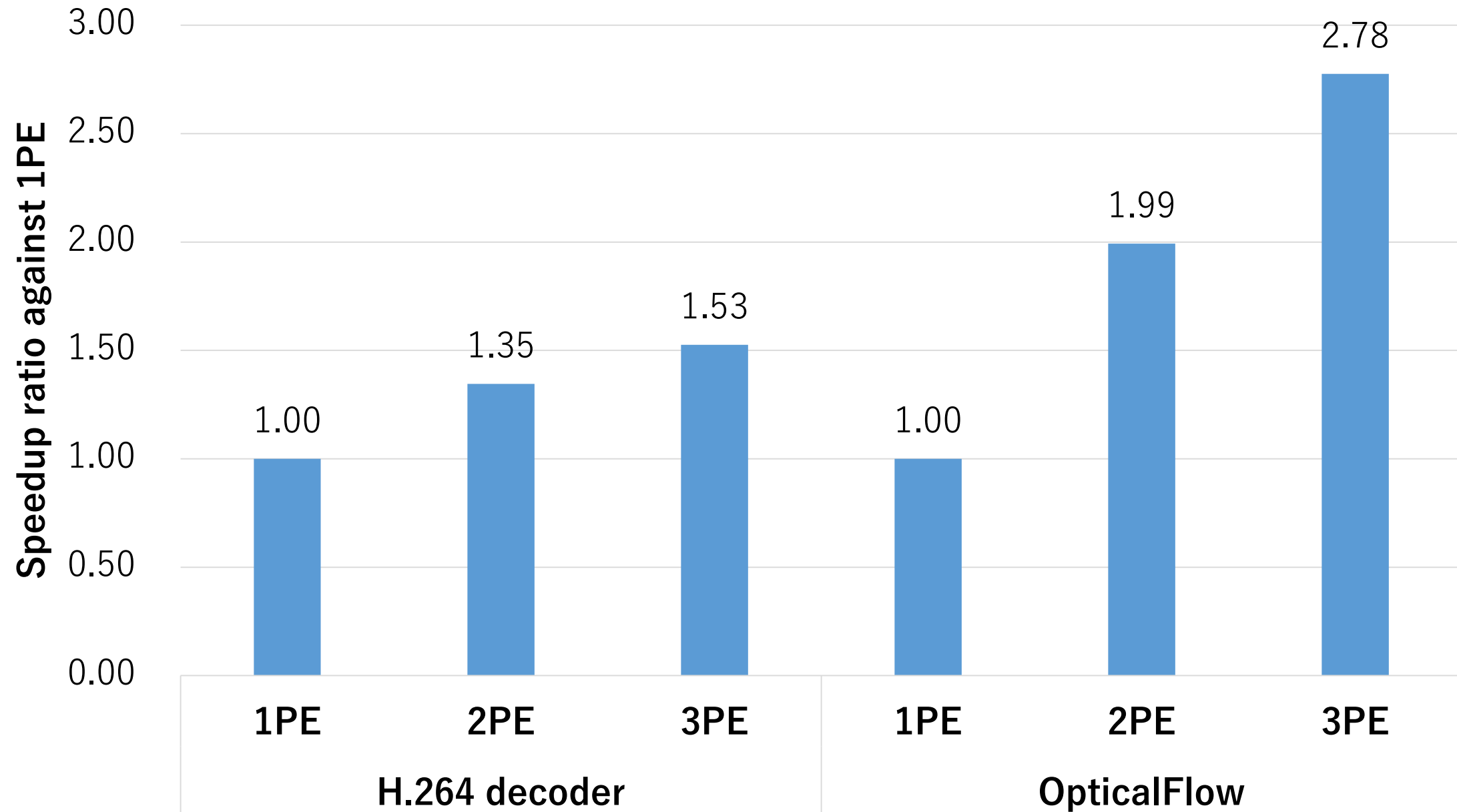
Automatic Power Reduction on ARM CortexA9 with Android

http://www.youtube.com/channel/UCS43lNYEIkC8i_KIgFZYQBQ
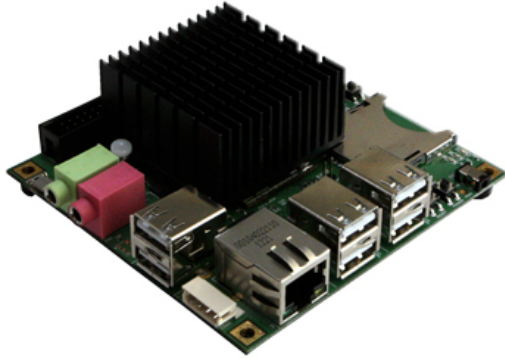
ODROID X2

Samsung Exynos4412 Prime, ARM Cortex-A9 Quad core
1.7GHz〜0.2GHz, used by Samsung's Galaxy S3

■ 1 core   ■ 2 cores   ■ 3 cores

H.264 decoder & Optical Flow   (on 3 cores)

Average Power Consumption[W]

H.264 without power control: 1 core 1.07, 2 cores 1.69, 3 cores 2.45
H.264 with power control: 1 core 0.79, 2 cores 0.57, 3 cores 0.51
-79.2%（1／5）
-52.3% (1/2)

Optical flow without power control: 1 core 0.95, 2 cores 1.50, 3 cores 2.23
Optical flow with power control: 1 core 0.72, 2 cores 0.36, 3 cores 0.30
- 86.5% (1/7)
- 68.4% (1/3)

without power control   with power control   without power control   with power control

H.264   Optical flow

Power for 3cores was reduced to 1/5〜1/7 against without software power control
Power for 3cores was reduced to 1/2〜1/3 against ordinary 1core execution

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Automatic Power Reduction of OpenCV Face Detection on big.LITTLE ARM Processor
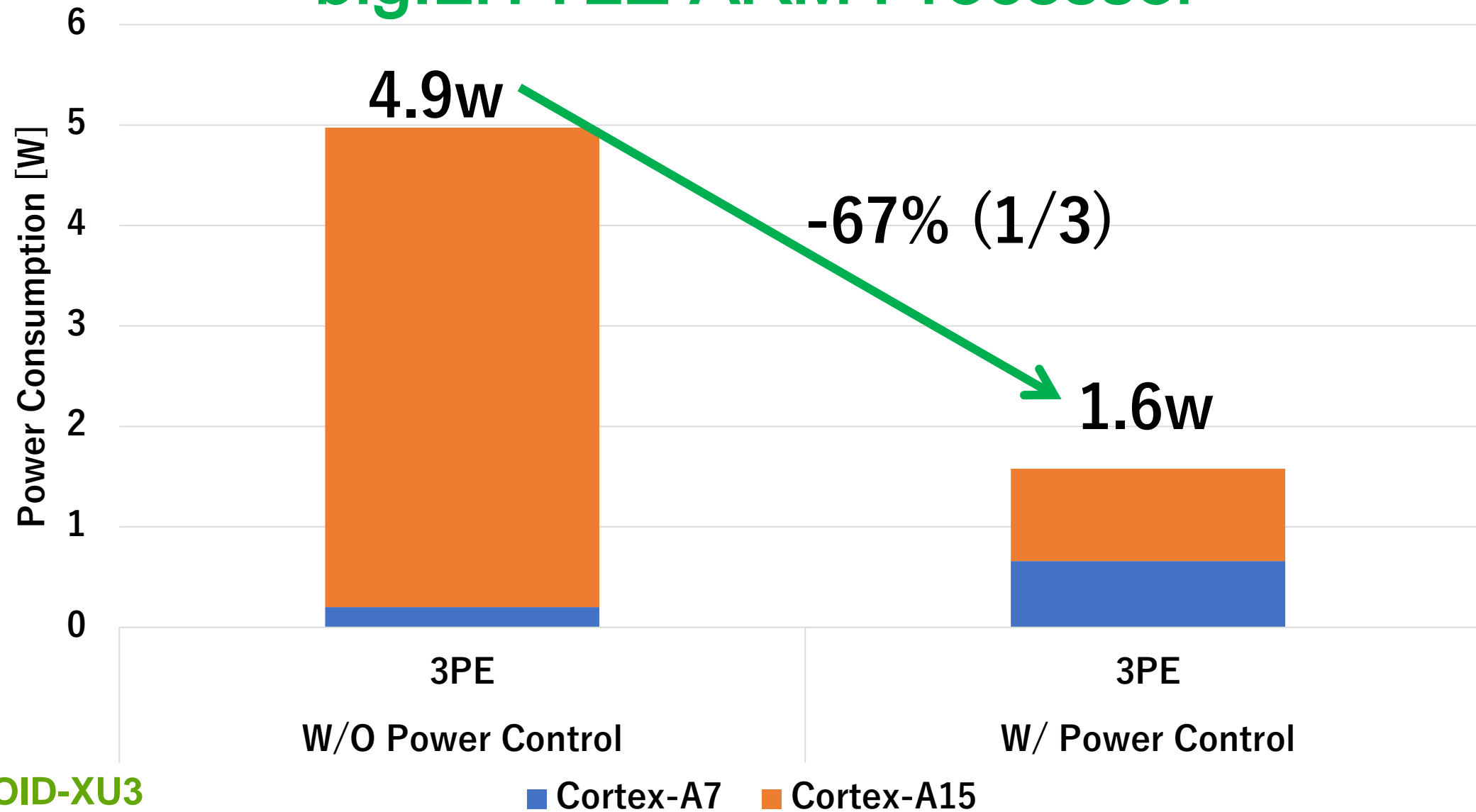
- **ODROID-XU3**
  - Samsung Exynos 5422 Processor
    - 4x Cortex-A15 2.0GHz, 4x Cortex-A7 1.4GHz big.LITTLE Architecture
    - 2GB LPDDR3 RAM Frequency can be changed by each cluster unit

Automatic Power Reduction on Intel Haswell
H.264 decoder & Optical Flow (3cores)

H81M-A, Intel Core i7 4770k
Quad core, 3.5GHz～0.8GHz
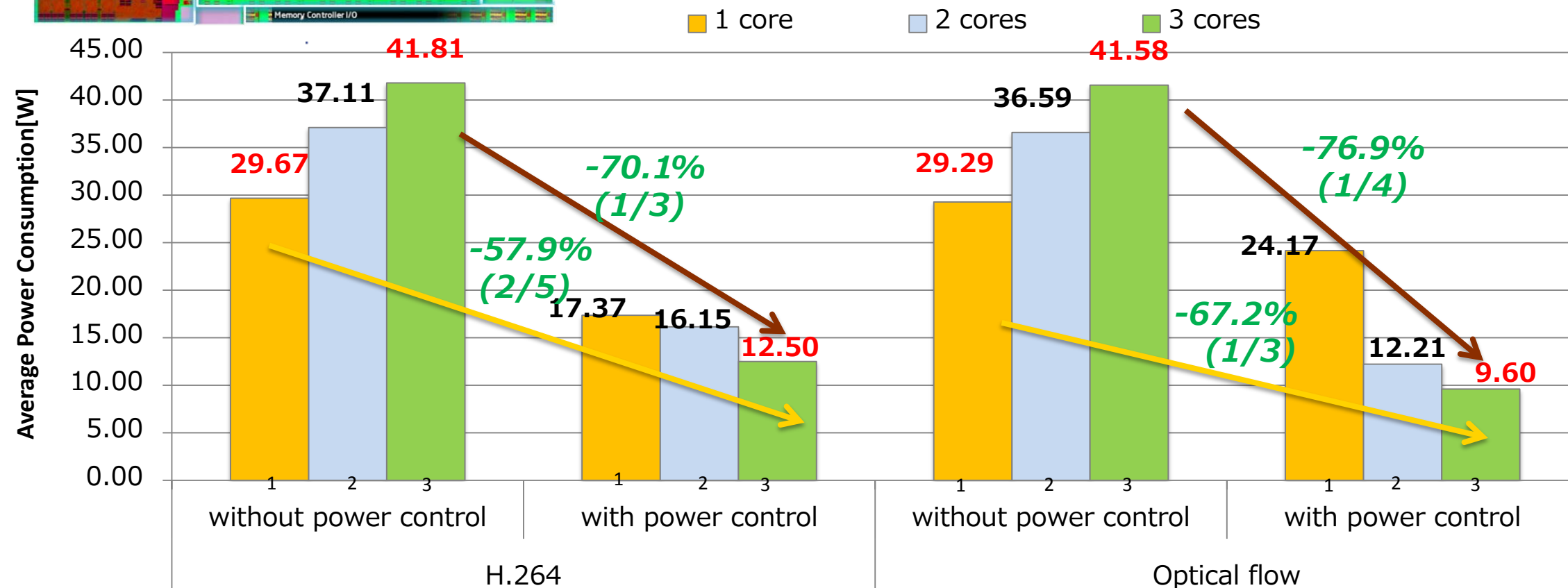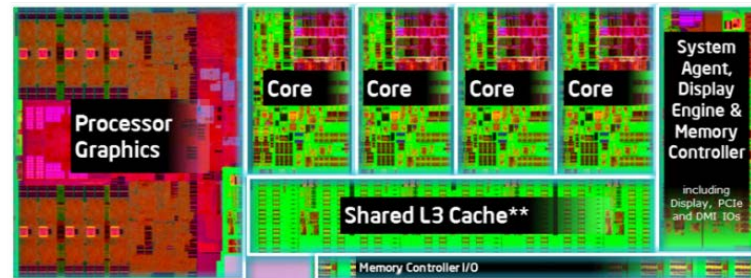
Power for 3cores was reduced to 1/3～1/4 against without software power control

Power for 3cores was reduced to 2/5～1/3 against ordinary 1core execution

110 Times Speedup against the Sequential Processing for GMS Earthquake Wave Propagation Simulation on Hitachi SR16000
（Power7 Based 128 Core Linux SMP）
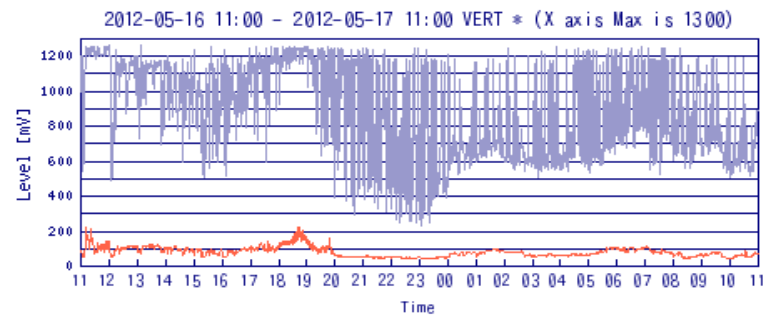
First touch for distributed shared memory and cache optimization over loops are important for scalable speedup

Fortran:15 thousand lines
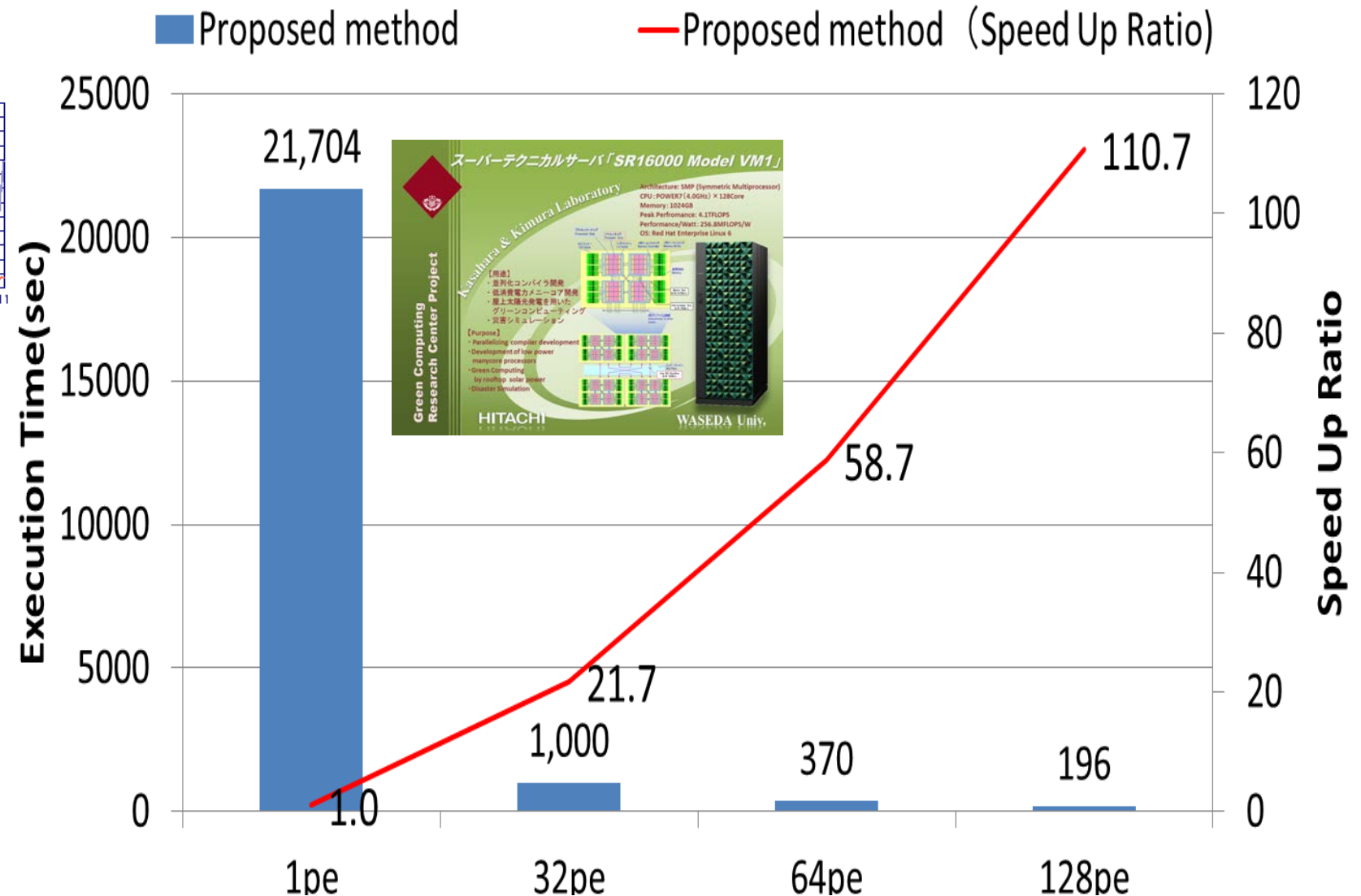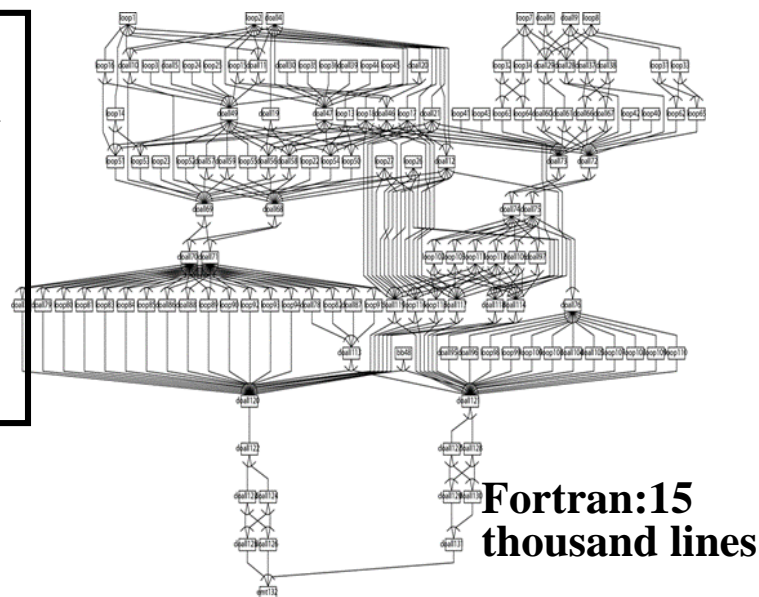
Cancer TreatmentCarbon Ion Radiotherapy

(Previous best was 2.5 times speedup on 16 processors with hand optimization)

National Institute of Radiological Sciences (NIRS)
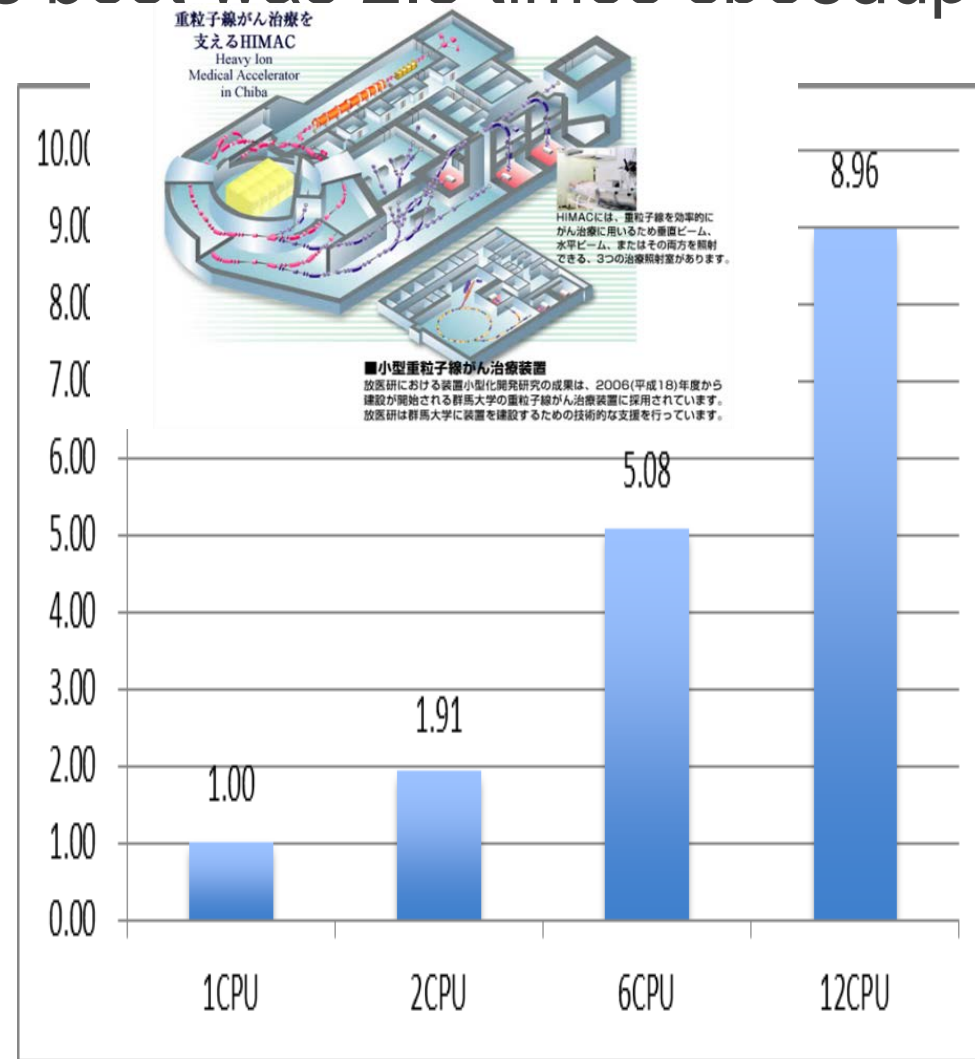
8.9times speedup by 12 processors

Intel Xeon X5670 2.93GHz 12 core SMP (Hitachi HA8000)
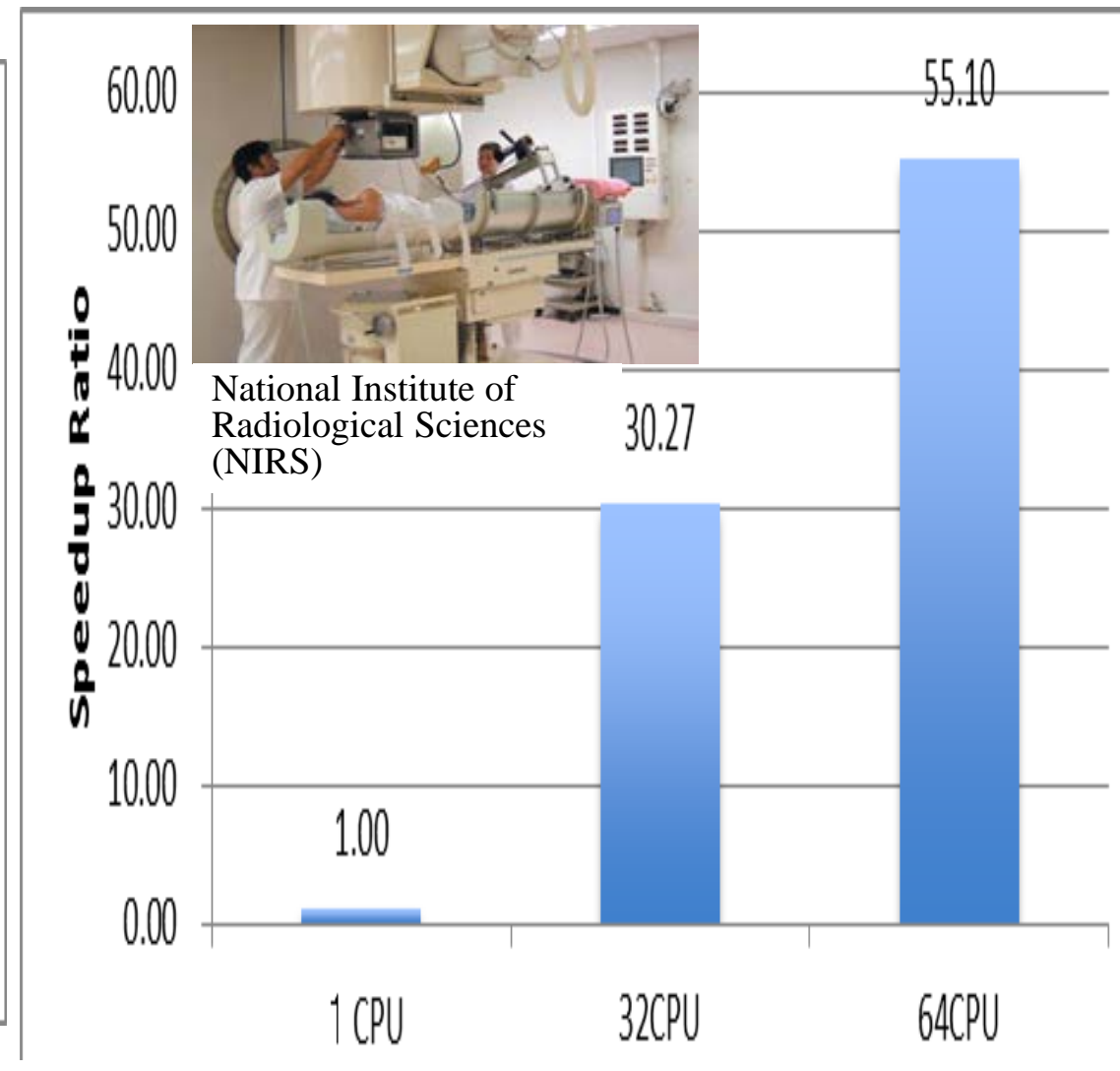
55 times speedup by 64 processors

IBM Power 7   64 core SMP (Hitachi SR16000)

Performance on Multicore Server for Latest Cancer Treatment Using Heavy Particle (Proton, Carbon Ion)

327 times speedup on 144 cores
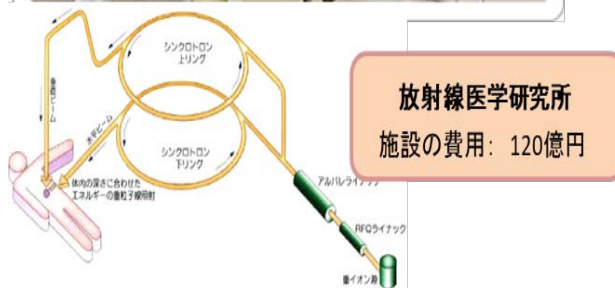
Hitachi 144cores SMP Blade Server BS500:
Xeon E7-8890 V3(2.5GHz　18core/chip) x8 chip

放射線医学研究所
施設の費用: 120億円

327.6 times speed up with 144 cores

- GCC
- OSCAR

	1PE	32pe	64pe	144pe
GCC	1.00			
OSCAR	5.00	109.20	196.50	327.60
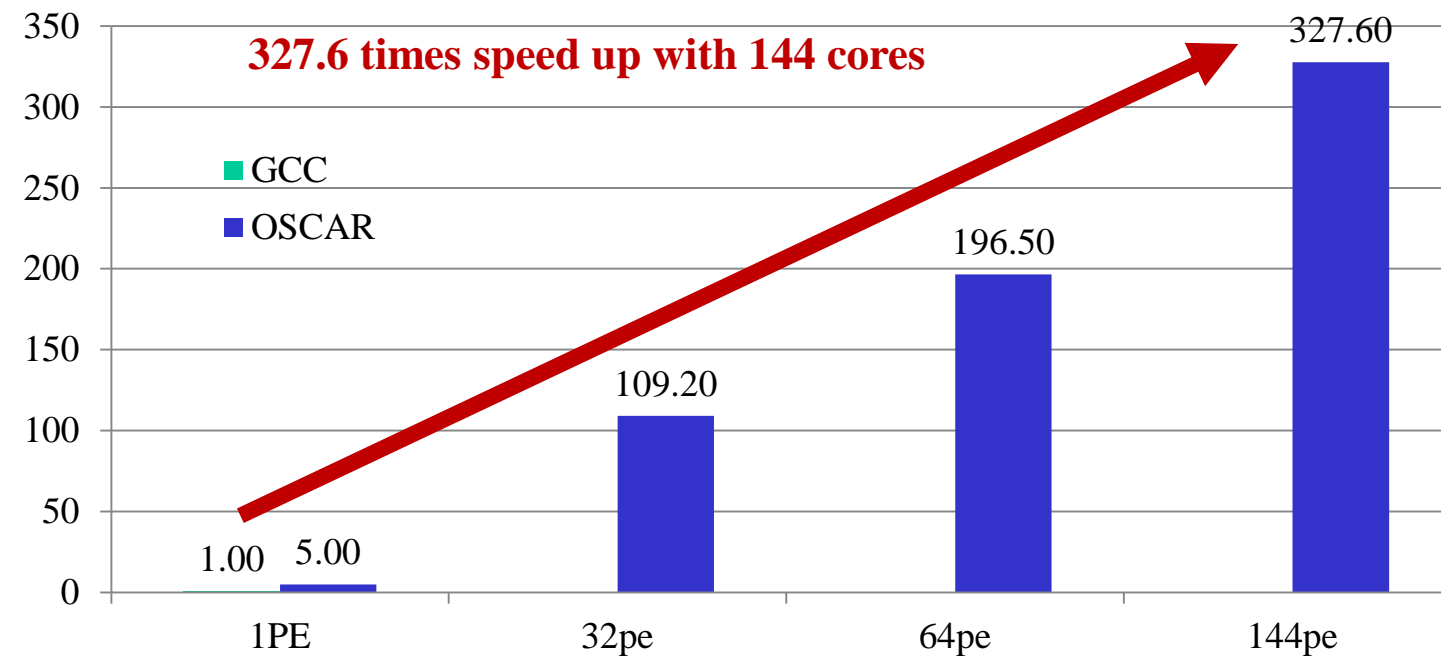
➢ **Original sequential execution time 2948 sec（50 minutes）using GCC was reduced to 9 sec with 144 cores（327.6 times speedup）**

➢ **Reduction of treatment cost and reservation waiting period is expected**

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Engine Control by multicore with Denso

Though so far parallel processing of the engine control on multicore has been very difficult, Denso and Waseda succeeded 1.95 times speedup on 2core V850 multicore processor.

➤ Hard real-time automobile engine control by multicore using local memories

➤ Millions of lines C codes consisting conditional branches and basic blocks

1 core
逐次

2 cores
並列化
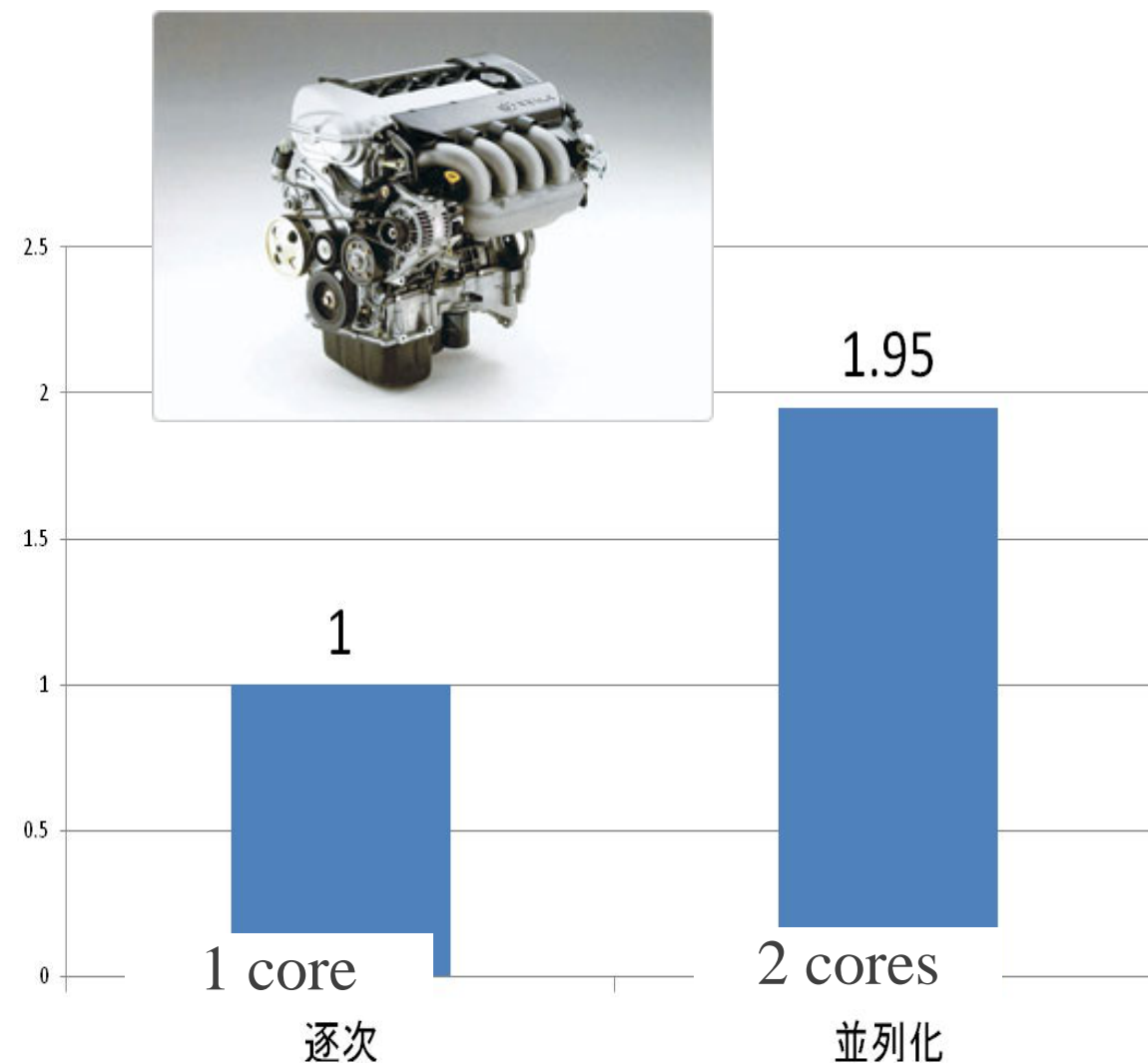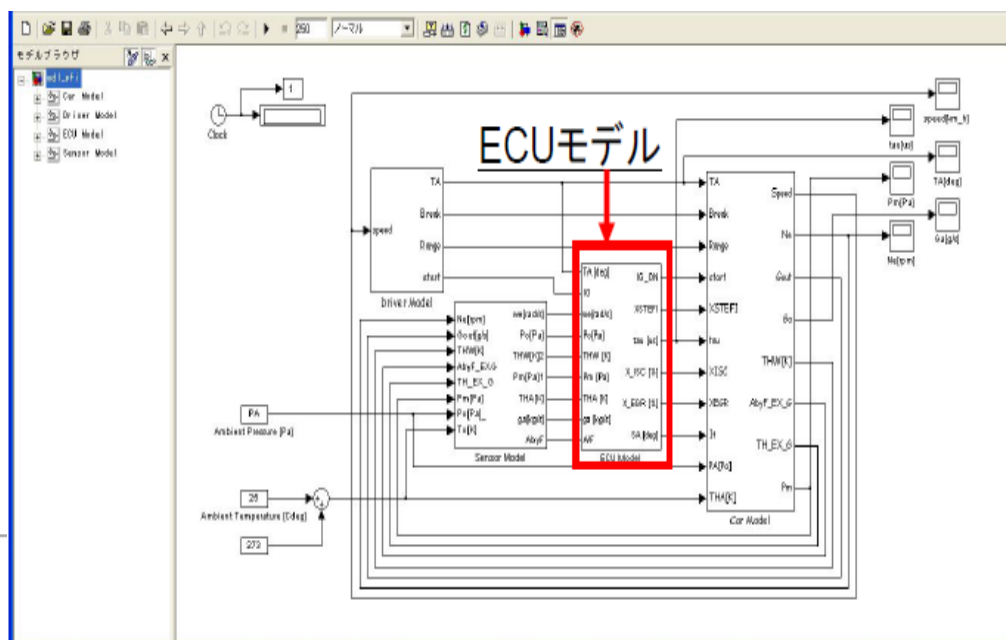
Macro Task Fusion for Static Task Scheduling

: Data Dependency
: Control Flow
○ : Conditional Branch

Fuse branches and succeeded tasks

Merged block

Only data dependency

MFG of sample program before maro task fusion

MFG of sample program after macro task fusion

MTG of sample program after macro task fusion
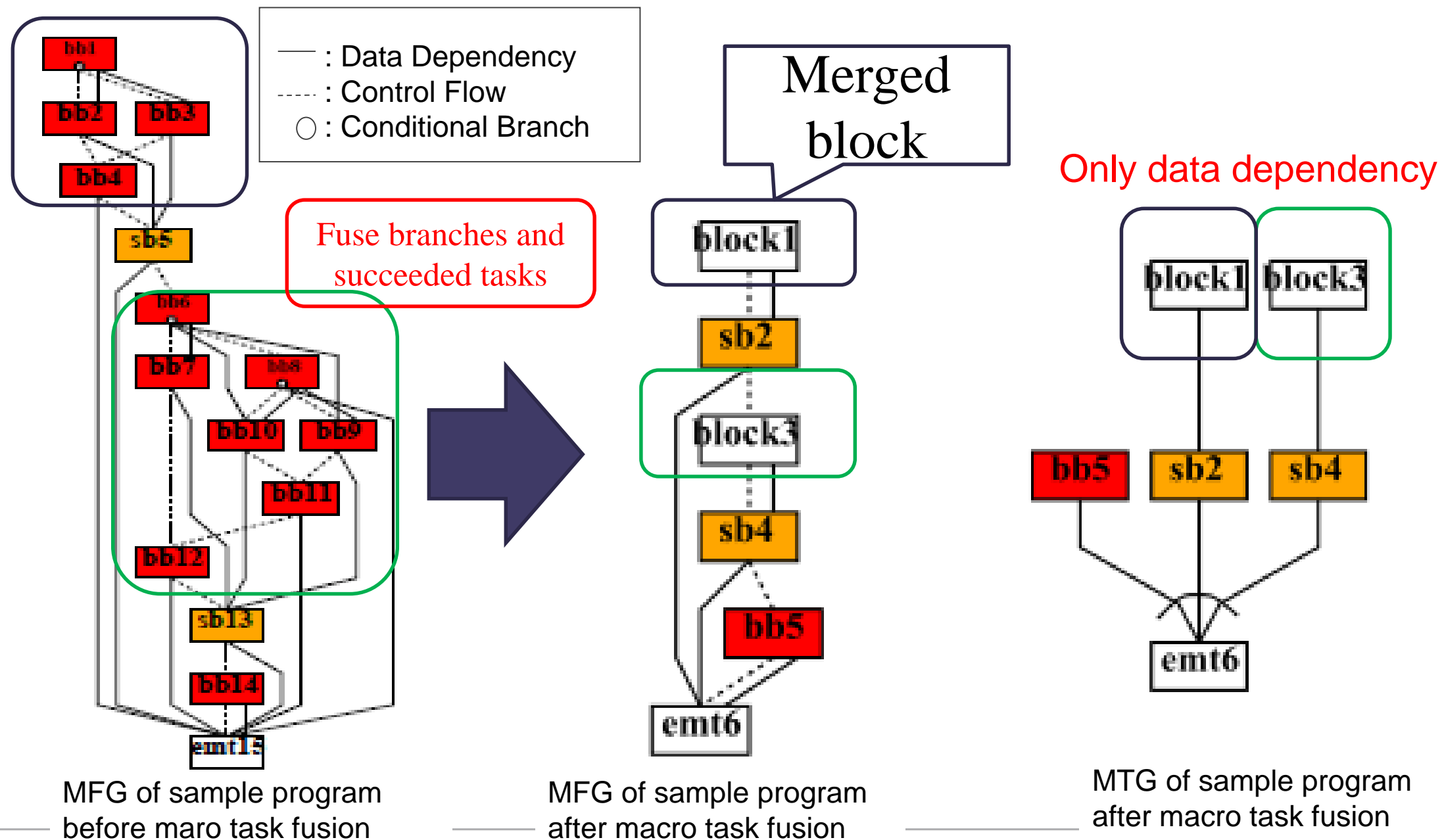
OSCAR Compile Flow for Simulink Applications
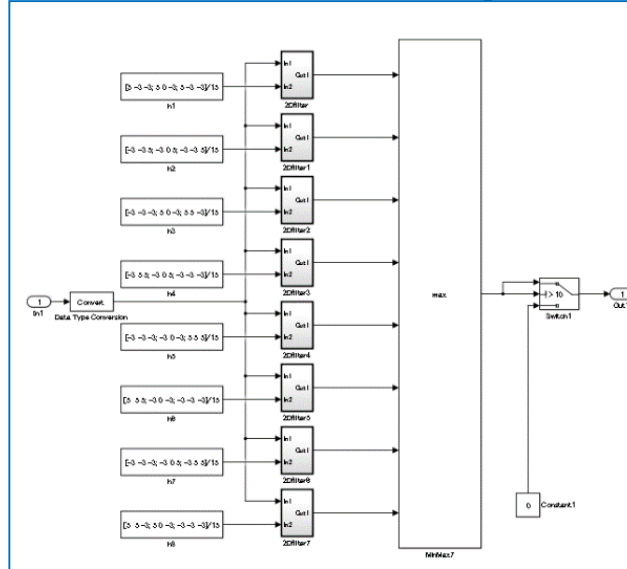
Simulink model

Generate C code using Embedded Coder

C code

OSCAR Compiler

(1) Generate MTG
→ Parallelism

(2) Generate gantt chart
→ Scheduling in a multicore
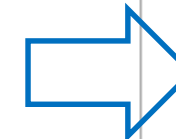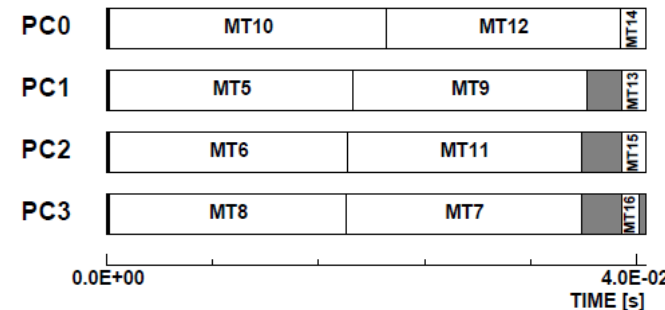
(3) Generate parallelized C code using the OSCAR API
→ Multiplatform execution
(Intel, ARM and SH etc)

Speedups of MATLAB/Simulink Image Processing on Various 4core Multicores (Intel Xeon, ARM Cortex A15 and Renesas SH4A)
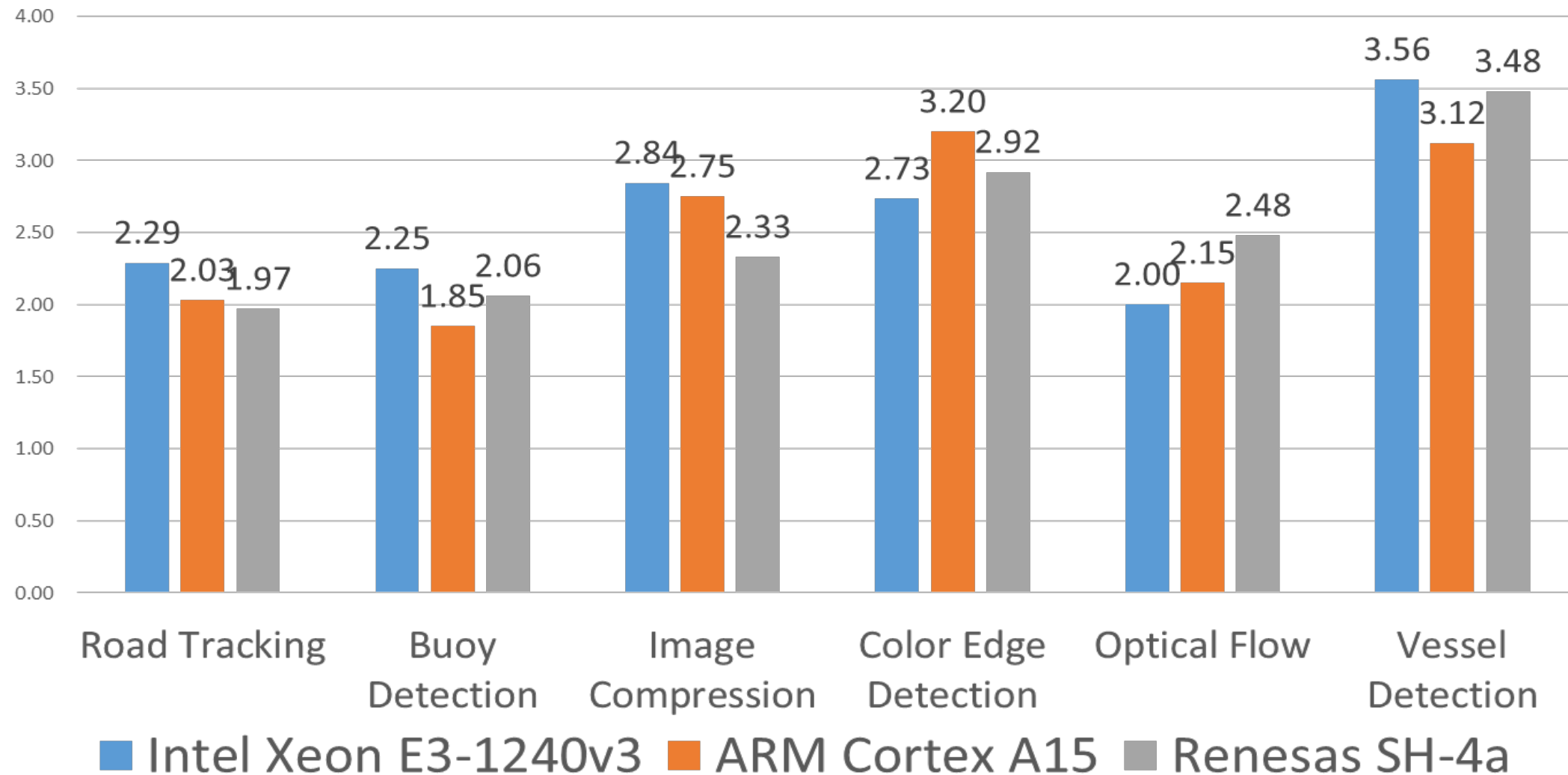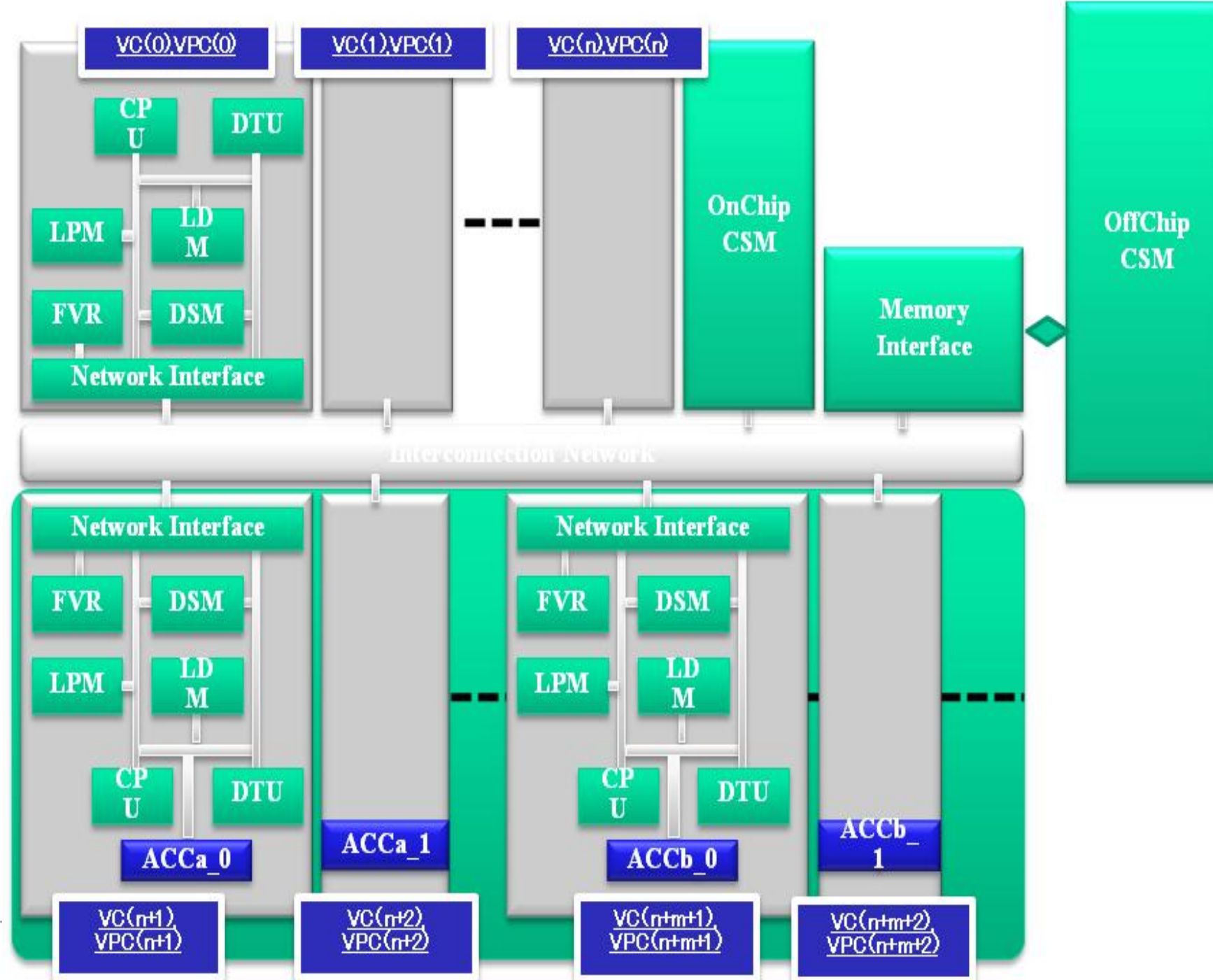

Road Tracking, Image Compression : http://www.mathworks.co.jp/jp/help/vision/examples
Buoy Detection : http://www.mathworks.co.jp/matlabcentral/fileexchange/44706-buoy-detection-using-simulink
Color Edge Detection : http://www.mathworks.co.jp/matlabcentral/fileexchange/28114-fast-edges-of-a-color-image--actual-color--not-converting-to-grayscale-/
Vessel Detection : http://www.mathworks.co.jp/matlabcentral/fileexchange/24990-retinal-blood-vessel-extraction/

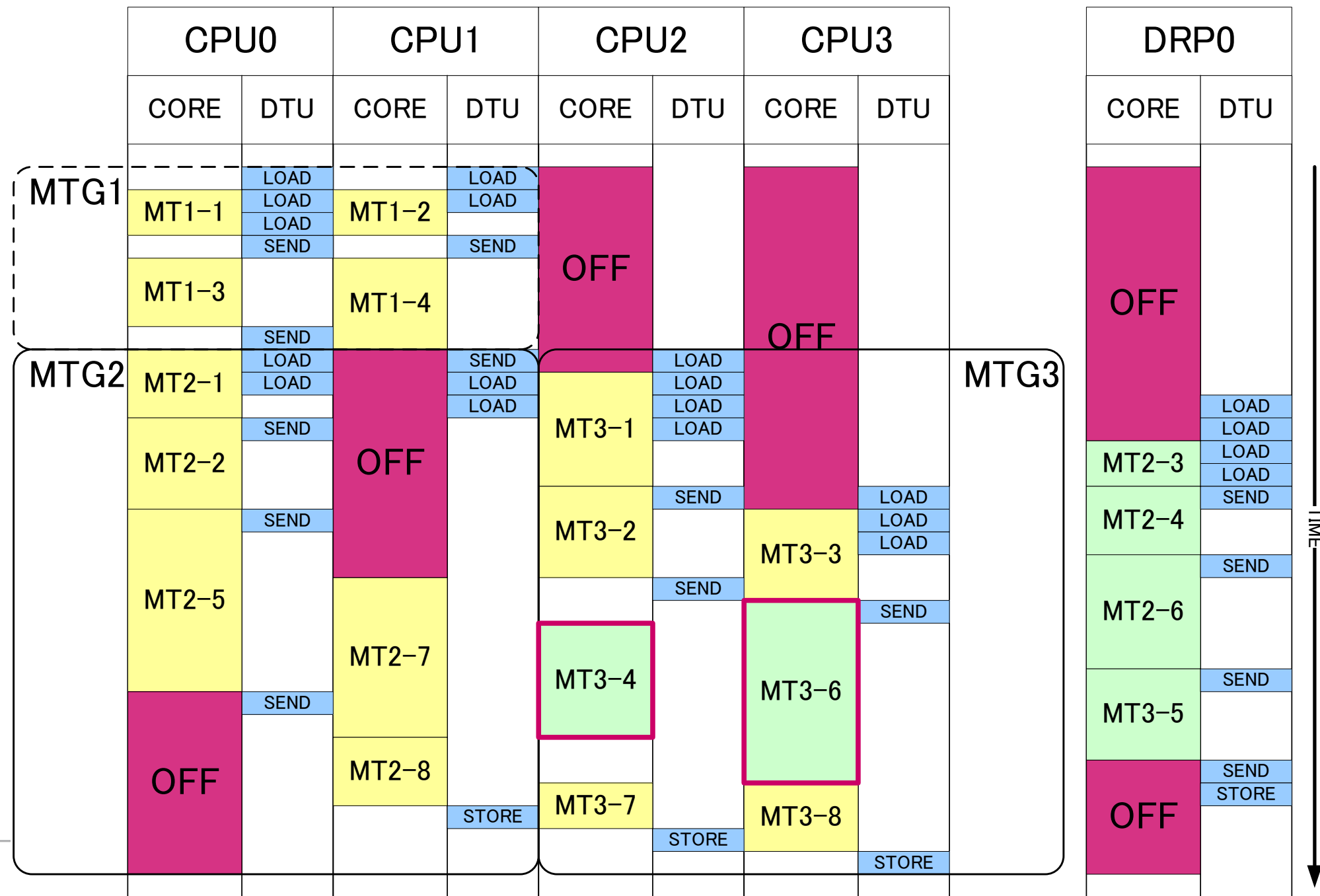SEMICON JAPAN

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OSCAR Heterogeneous Multicore

- **DTU**
  - **Data Transfer Unit**
- **LPM**
  - **Local Program Memory**
- **LDM**
  - **Local Data Memory**
- **DSM**
  - **Distributed Shared Memory**
- **CSM**
  - **Centralized Shared Memory**
- **FVR**
  - **Frequency/Voltage Control Register**

An Image of Static Schedule for Heterogeneous Multi-core with Data Transfer Overlapping and Power Control

OSCAR API Ver. 2.0 for Homogeneous/Heterogeneous Multicores and Manycores

List of Directives (22 directives)

- **Parallel Execution API**
  - parallel sections (*)
  - flush (*)
  - critical (*)
  - execution
- **Memoay Mapping API**
  - threadprivate (*)
  - distributedshared
  - onchipshared
- **Synchronization API**
  - groupbarrier
- **Data Transfer API**
  - dma_transfer
  - dma_contiguous_parameter
  - dma_stride_parameter
  - dma_flag_check
  - dma_flag_send

(* from OpenMP)

- **Power Control API**
  - fvcontrol
  - get_fvstatus
- **Timer API**
  - get_current_time
- **Accelerator**
  - accelerator_task_entry
- **Cache Control**
  - cache_writeback
  - cache_selfinvalidate
  - complete_memop
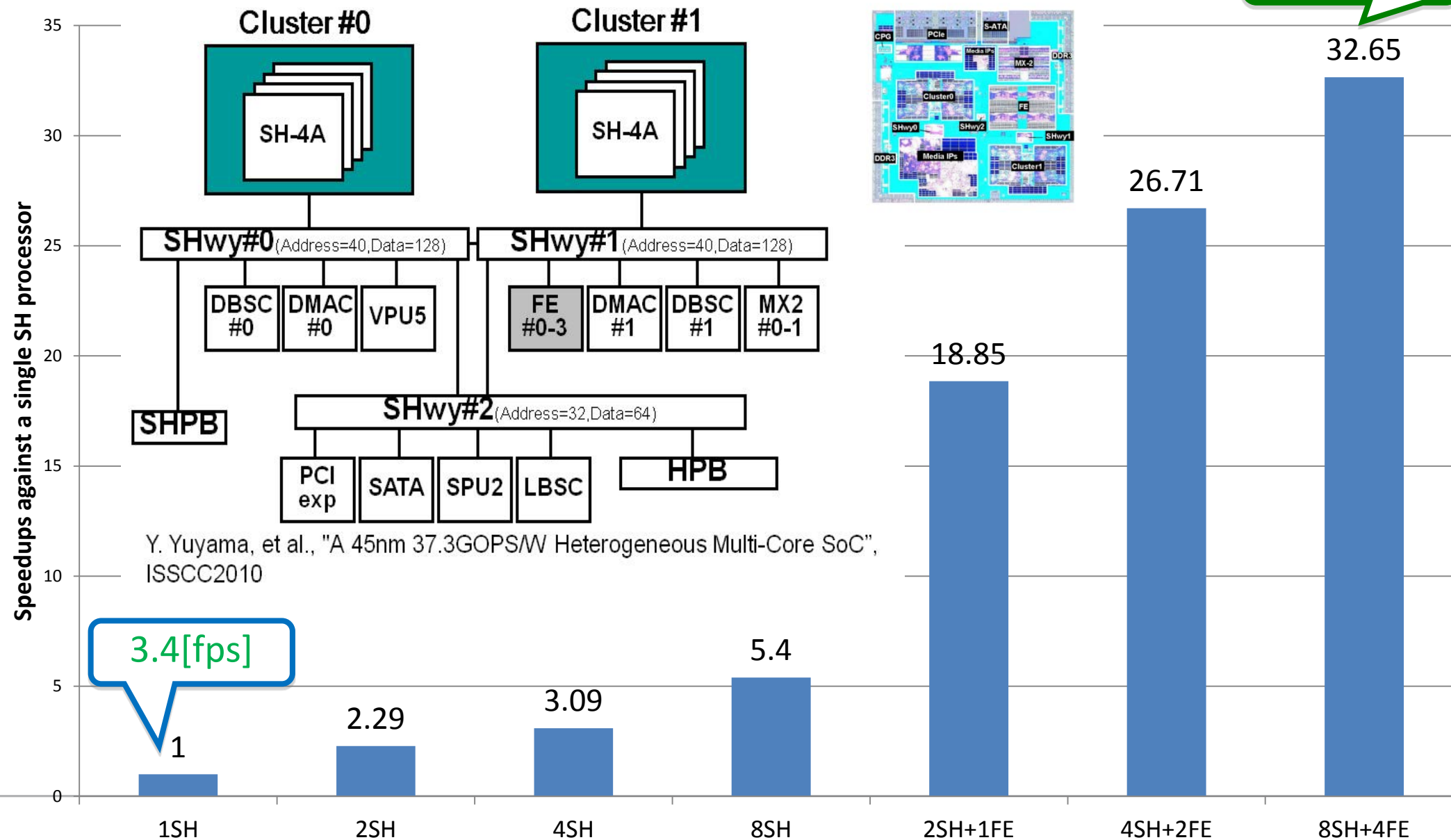 - noncacheable
  - aligncache

2 hint directives for OSCAR compiler
- accelerator_task
- oscar_comment

from V2.0

SEMICON JAPAN

semi

33 Times Speedup Using OSCAR Compiler and OSCAR API on RP-X (Optical Flow with a hand-tuned library)

Y. Yuyama, et al., "A 45nm 37.3GOPS/W Heterogeneous Multi-Core SoC", ISSCC2010

Power Reduction in a real-time execution controlled by OSCAR Compiler and OSCAR API on RP-X
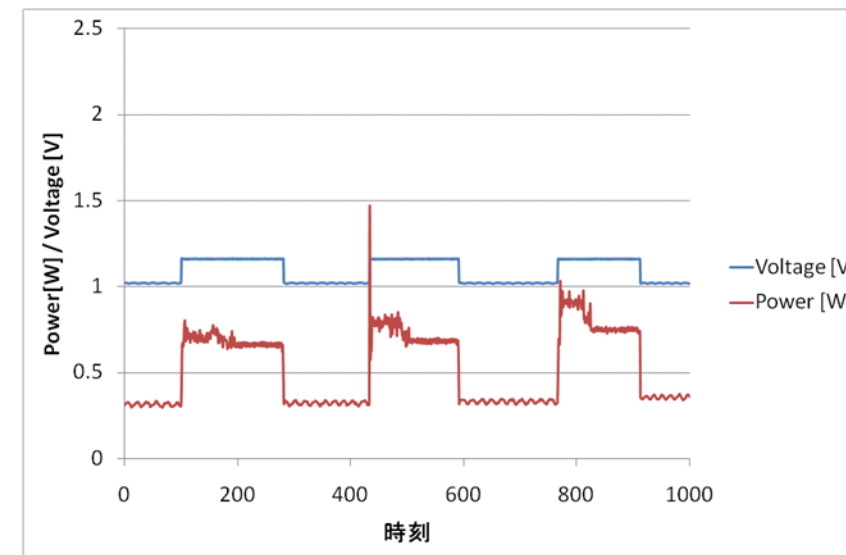## (Optical Flow with a hand-tuned library)

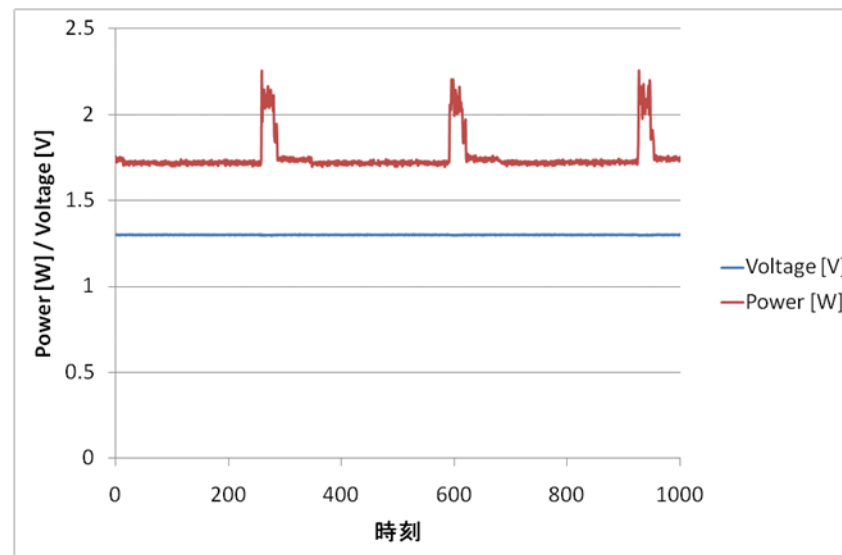**Without Power Reduction**

With Power Reduction by OSCAR Compiler
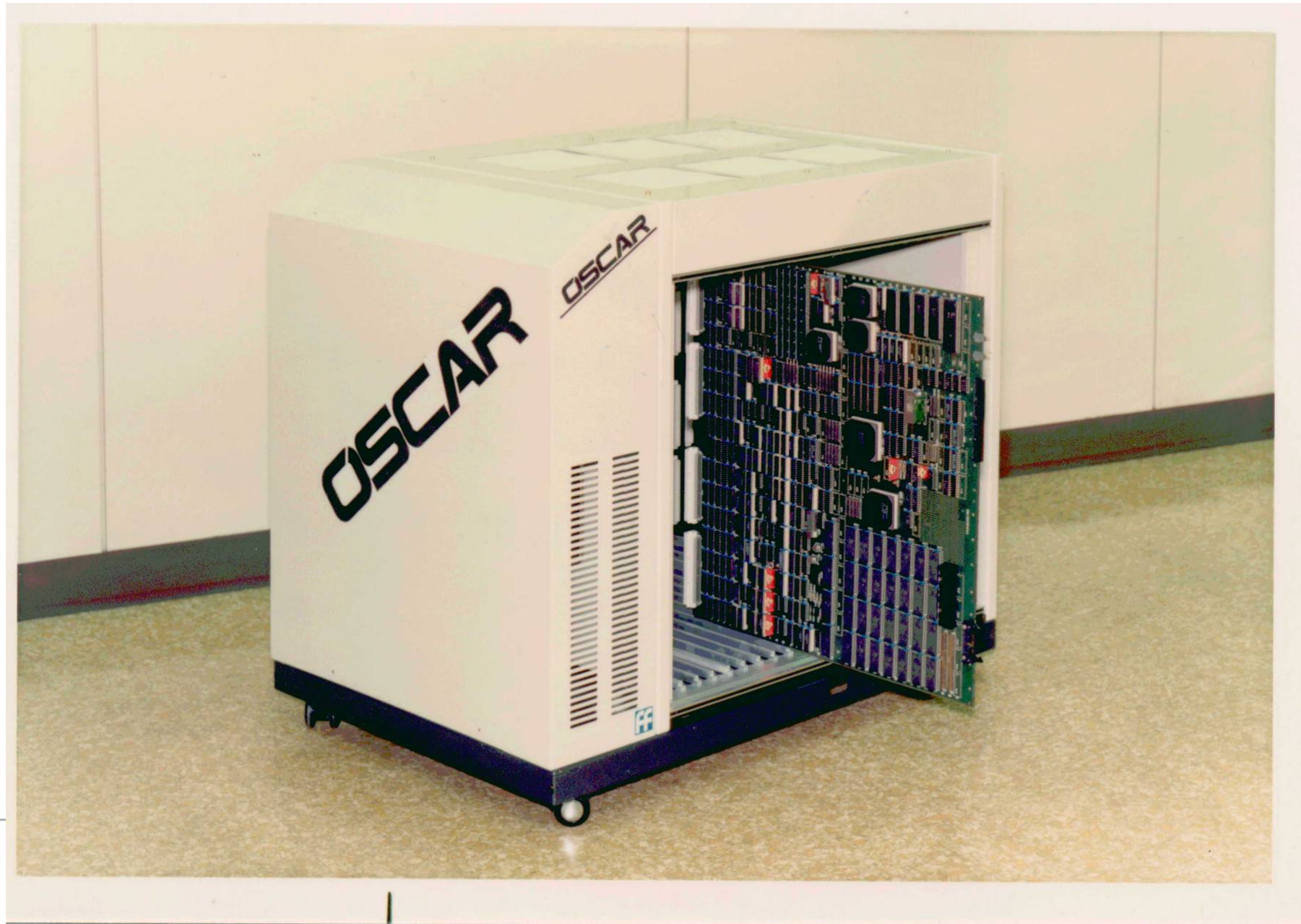
70% of power reduction
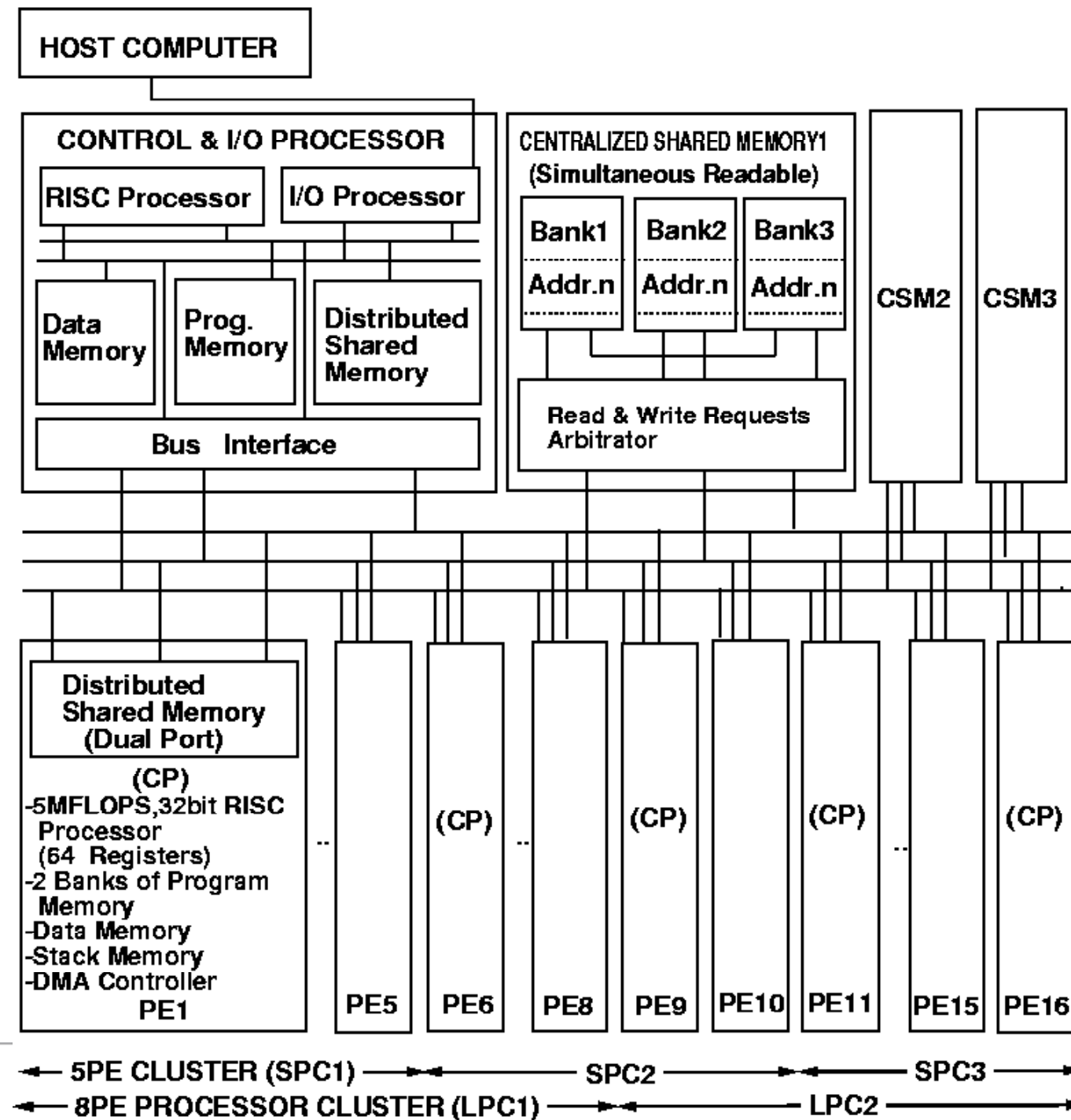
Average:1.76[W] → Average:0.54[W]

1cycle : 33[ms]
→30[fps]

1987 OSCAR(Optimally Scheduled Advanced Multiprocessor)

Co-design of Compiler and Architecture

Looking at various applications, design a parallelizing compiler and design
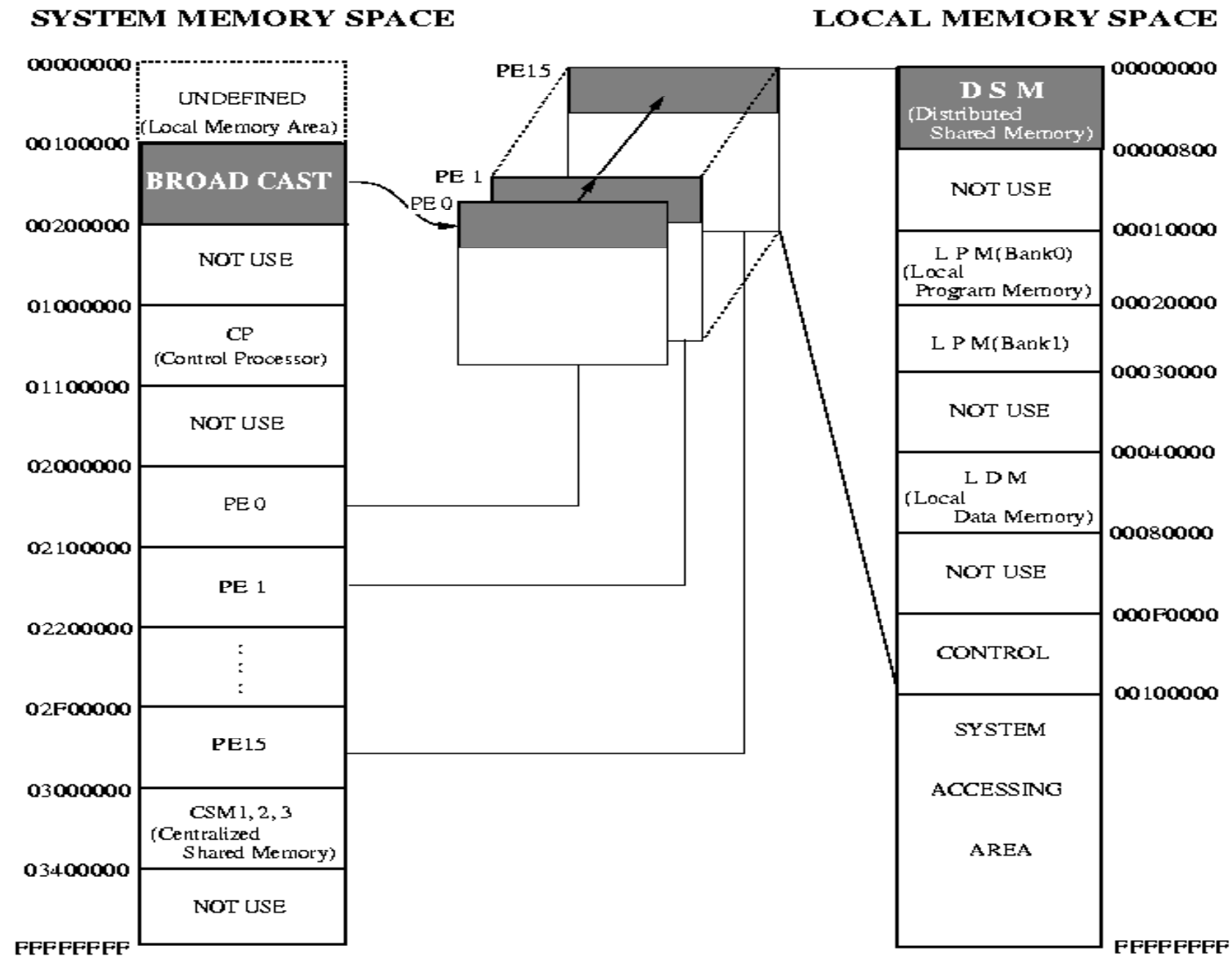a multiprocessor/multicore-processor to support compiler optimization

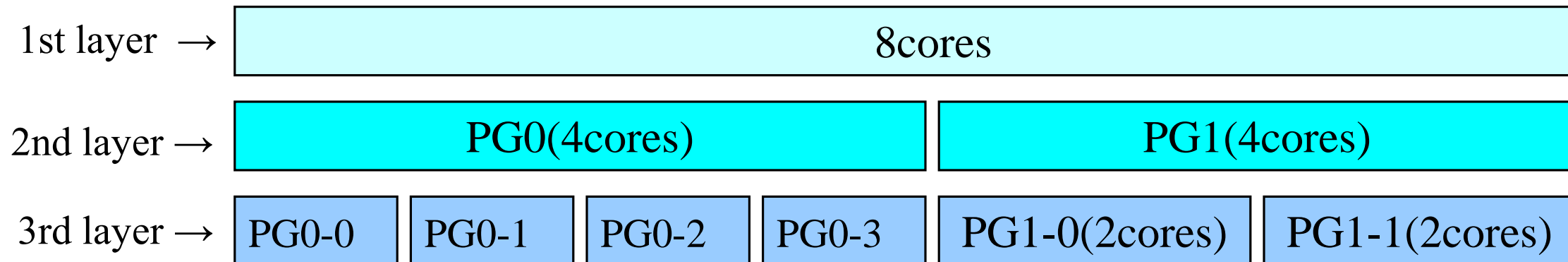# OSCAR(Optimally Scheduled Advanced Multiprocessor) 1987

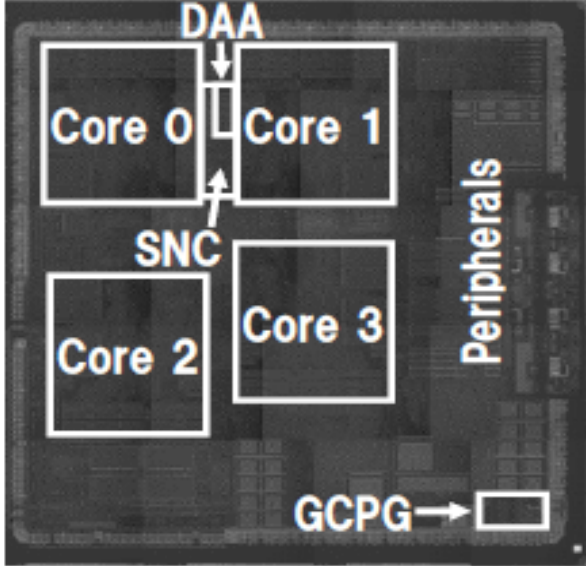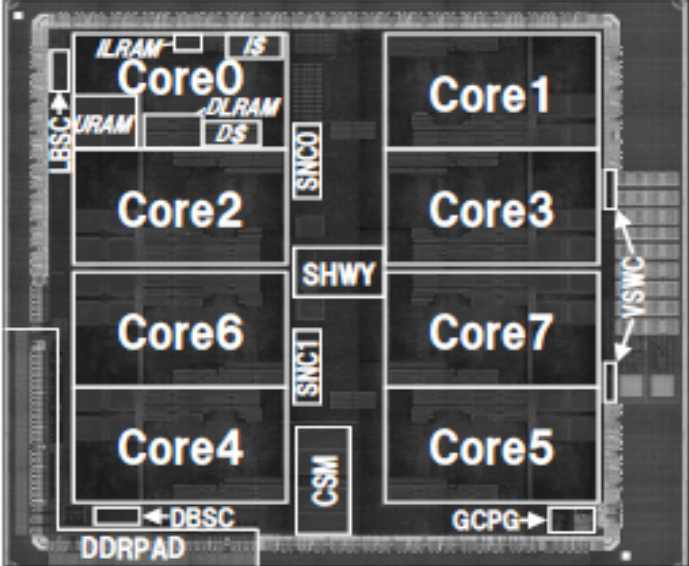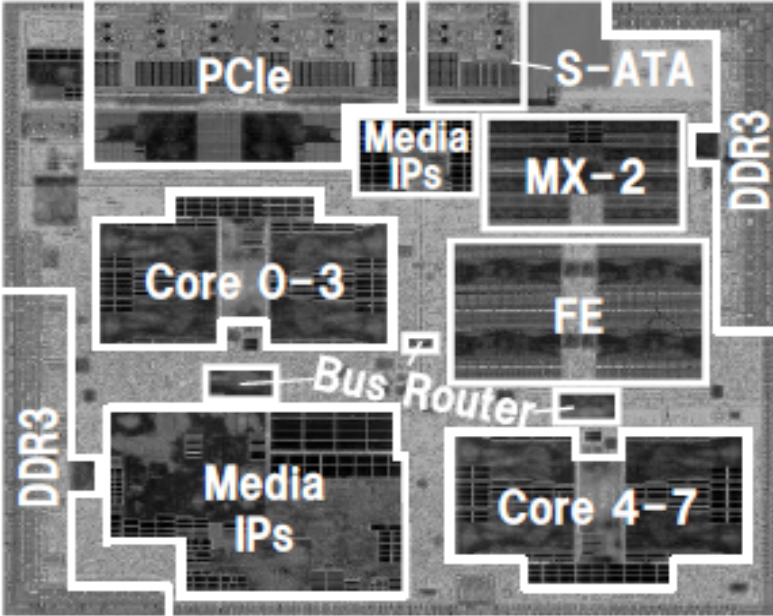# OSCAR Memory Space (Global Address Space)

Hierarchical Barrier Synchronization

- **Specifying a hierarchical group barrier**
  - **#pragma oscar group_barrier (C)**
  - **!$oscar group_barrier (Fortran)**

1st layer →	8cores					
2nd layer →	PG0(4cores)				PG1(4cores)	
3rd layer →	PG0-0	PG0-1	PG0-2	PG0-3	PG1-0(2cores)	PG1-1(2cores)

4 core multicore RP1 (2007) , 8 core multicore RP2 (2008) and 15 core Heterogeneous multicore RPX (2010) developed in NEDO Projects with Hitachi and Renesas

RP-1 (ISSCC2007 #5.3)	**RP-2** (ISSCC2008 #4.5)	**RP-X** (ISSCC2010 #5.3)
90nm, 8-layer, triple-Vth, CMOS	90nm, 8-layer, triple-Vth, CMOS	45nm, 8-layer, triple-Vth, CMOS
97.6 mm^2 (9.88 x 9.88 mm)	104.8 mm^2 (10.61 x 9.88 mm)	153.8 mm^2 (12.4 x 12.4 mm)
1.0V (internal), 1.8/3.3V (I/O)	1.0-1.4V (internal), 1.8/3.3V (I/O)	1.0-1.2V (internal), 1.2-3.3V (I/O)
600MHz ,4.32 GIPS,16.8 GFLOPS	600MHz , 8.64 GIPS, 33.6 GFLOPS	648MHz, 13.7GIPS, 115GOPS, 36.2GFLOPS
11.4 GOPS/W（32b換算）	18.3 GOPS/W（32b換算）	37.3 GOPS/W（32b換算）

Automatic Parallelization of JPEG-XR for Drinkable Inner Camera

10 times more speedup needed after parallelization for 128 cores of Power 7.
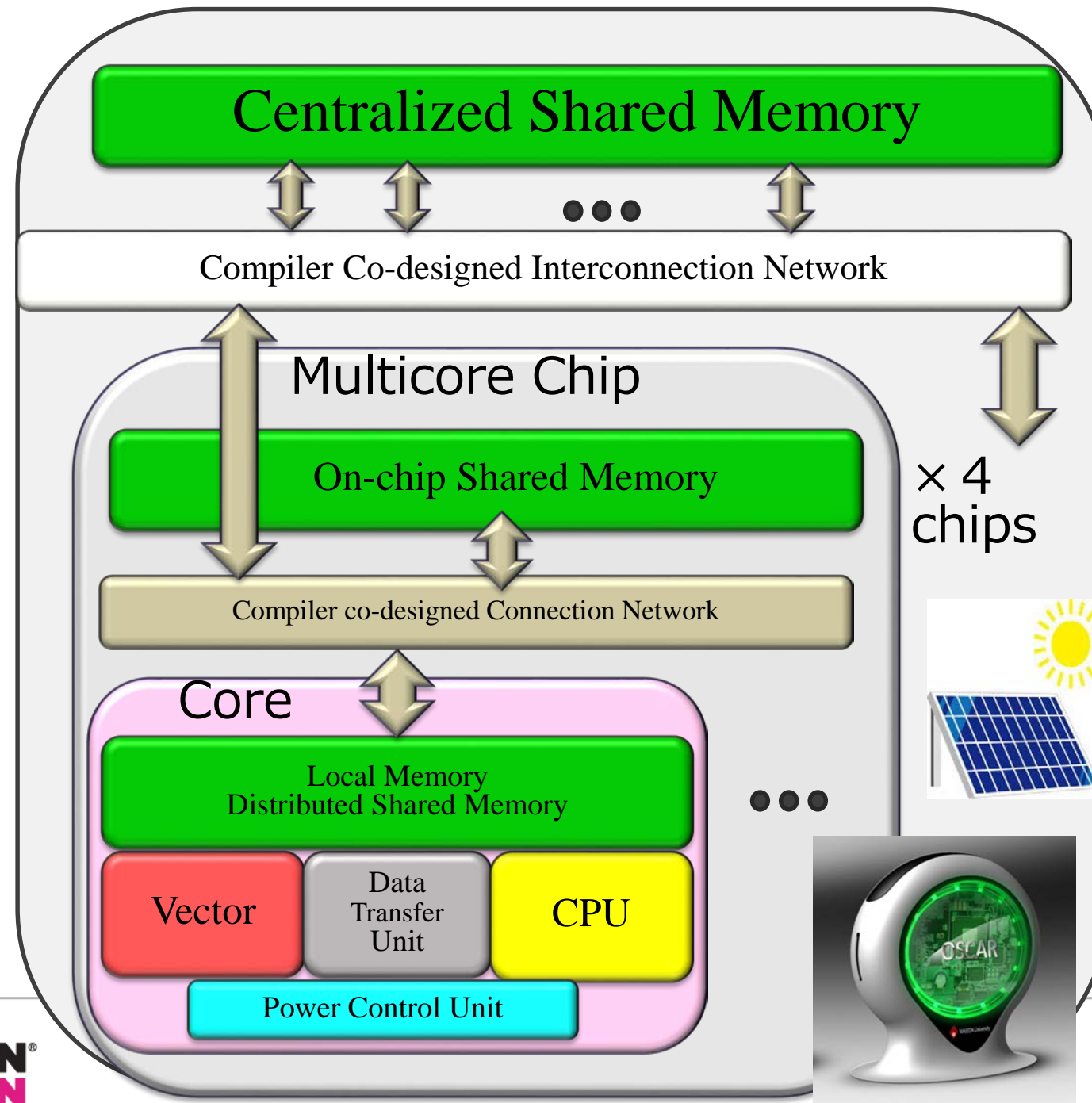## Less than 35mW power consumption is required.

- TILEPro64

Speed-ups on TILEPro64 Manycore

64cores
0.18[s]

1core
10.0[s]

Speed up values: 1.00, 1.96, 3.95, 7.86, 15.82, 30.79, 55.11
Cores: 1, 2, 4, 8, 16, 32, 64

55 times speedup with 64 cores
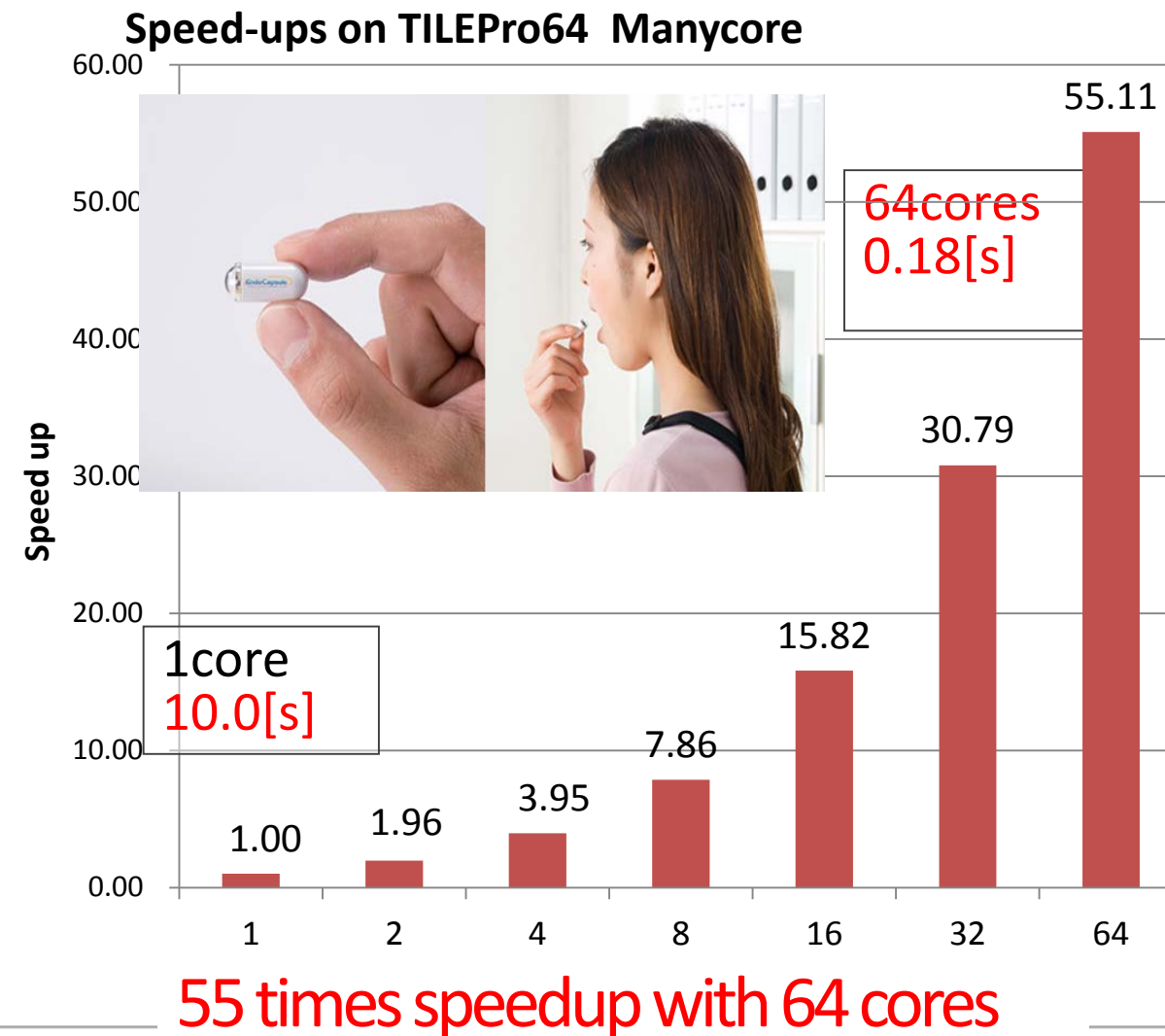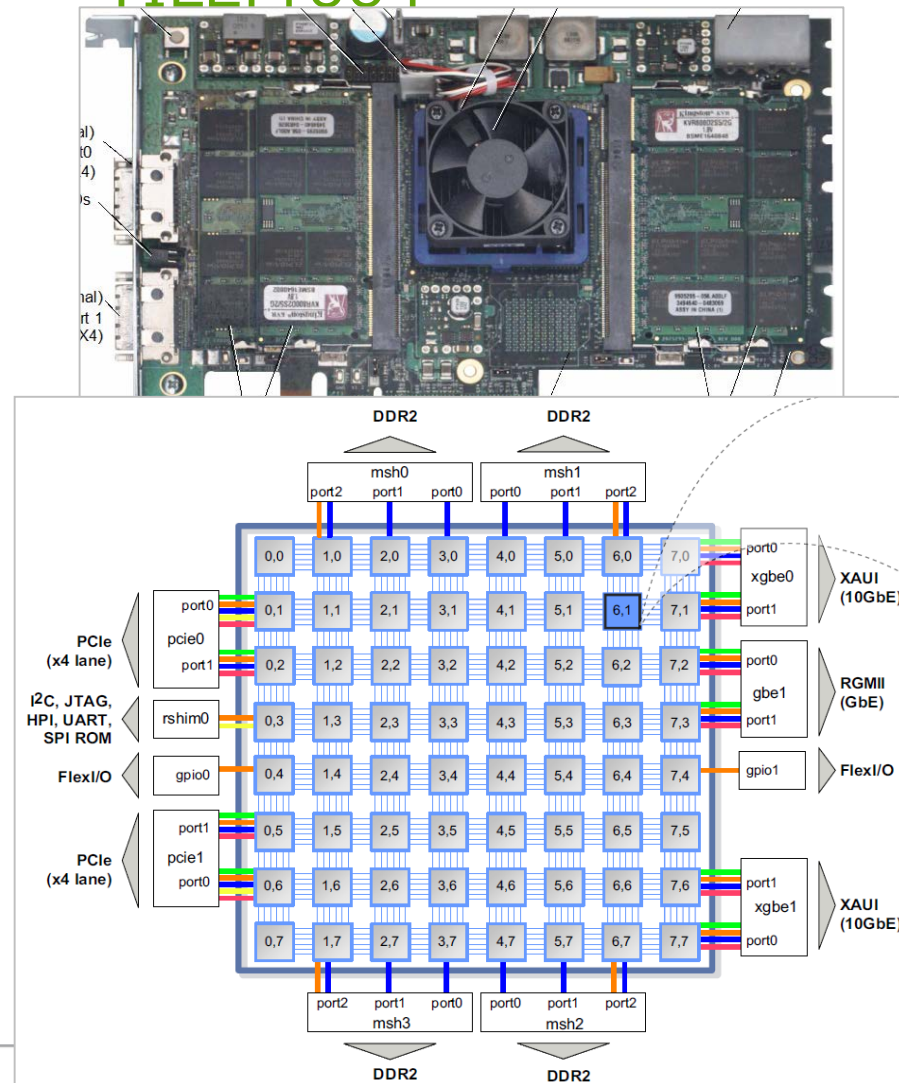
OSCAR Vector Multicore and Compiler for Embedded to Severs with OSCAR Technology

Centralized Shared Memory

Compiler Co-designed Interconnection Network

• • •

Multicore Chip

On-chip Shared Memory

× 4 chips

Compiler co-designed Connection Network

Core

Local Memory
Distributed Shared Memory

• • •

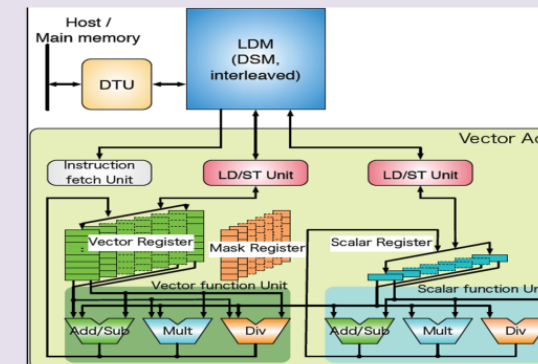Vector | Data Transfer Unit | CPU

Power Control Unit

Target:

➢ Solar Powered

➢ Compiler power reduction.

➢ Fully automatic parallelization and vectorization including local memory management and data transfer.

Vector Accelerator

Features
- Attachable for any CPUs (Intel, ARM, IBM)
- Data driven initiation by sync flags

Function Units [tentative]
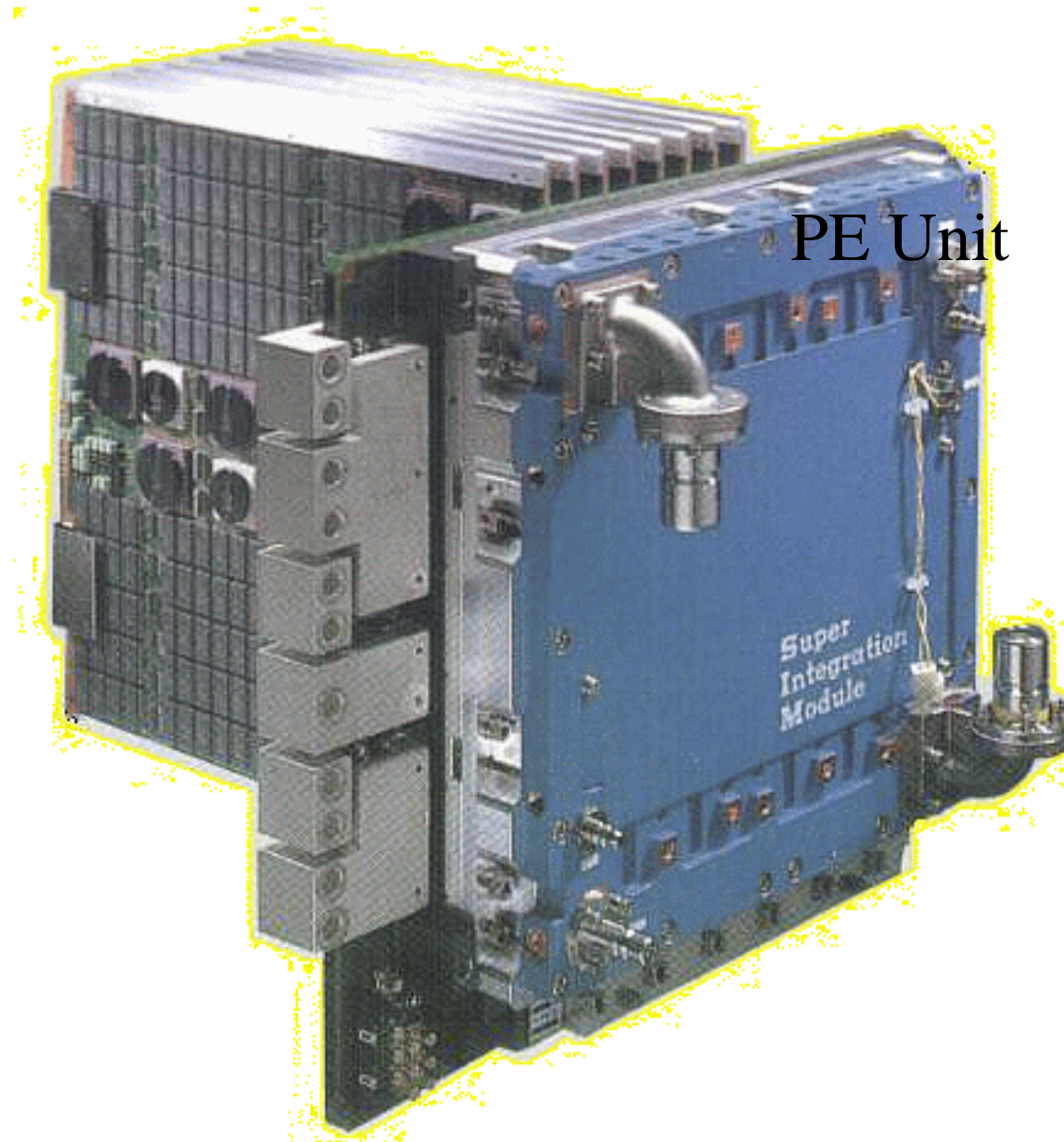- **Vector Function Unit**
  - 8 double precision ops/clock
  - 64 characters ops/clock
  - Variable vector register length
  - Chaining LD/ST & Vector pipes
- Scalar Function Unit

Registers[tentative]
- Vector Register 256Bytes/entry, 32entry
- Scalar Register 8Bytes/entry
- Floating Point Register 8Bytes/entry
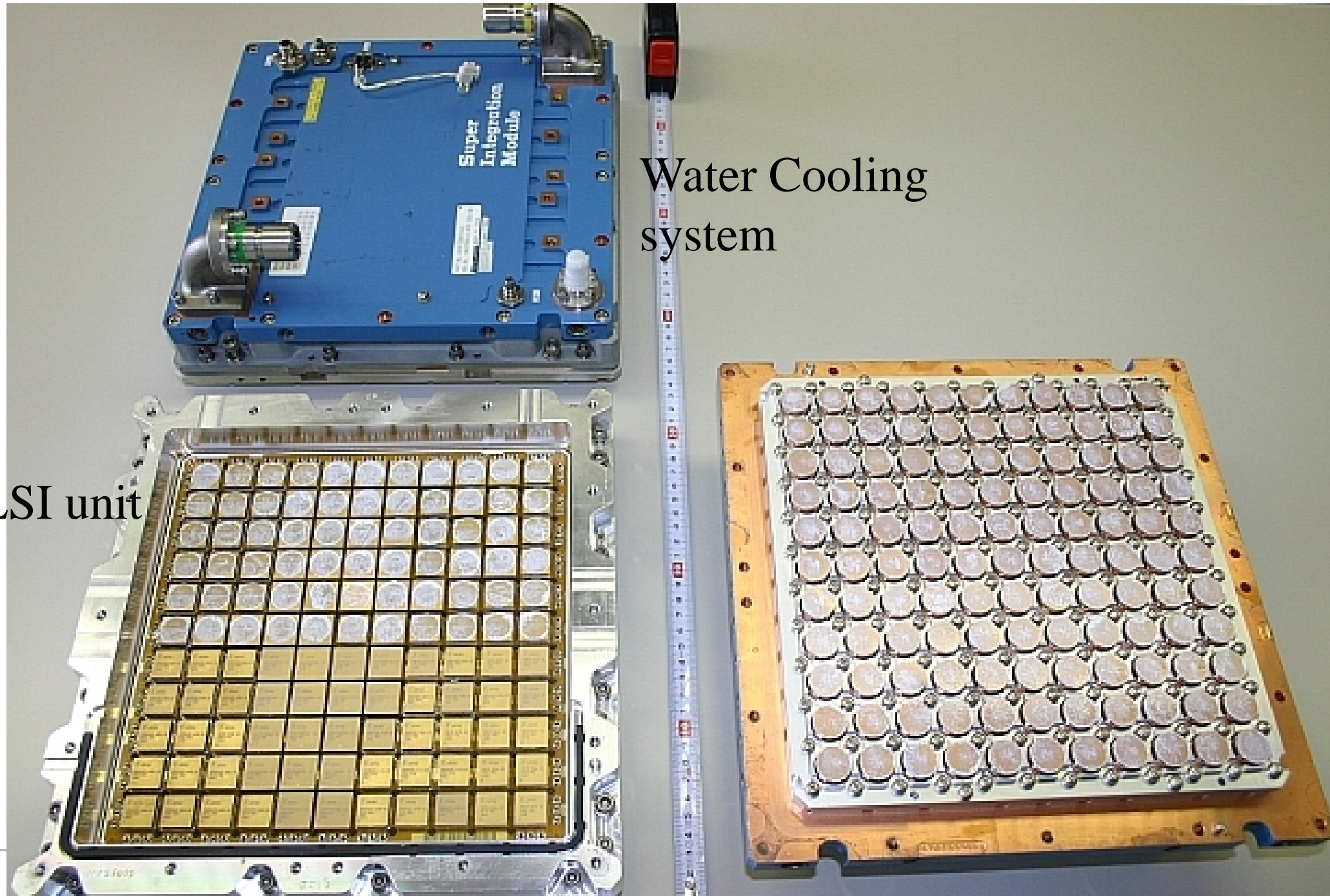- Mask Register 32Bytes/entry

Fujitsu VPP500/NWT

PE Unit

FujitsuVPP500/NWT

Water Cooling system

PE LSI unit

38

Earth Simulator

(http://www.es.jamstec.go.jp/)

• Earth Environmental simulation like Global Warming,
  El Nino, PlateMovement for the all lives onr this planet.

•Developed in Mar. 2002 by STA (MEXT) and NEC with
  400 M$ investment under Dr. Miyoshi's direction.
    (Dr.Miyoshi: Passed away in Nov.2001. NWT, VPP500, SX6)

Mr. Hajime Miyoshi

Image of Earth Simulator   4 Tennis Courts

Disks

Cartridge Tape Library System

Processor Node (PN)
Cabinets (320)

Interconnection Network (IN)
Cabinets (65)

Air Conditioning System

65m
71yd

Power Supply System

50m
55yd

Double Floor for Cables
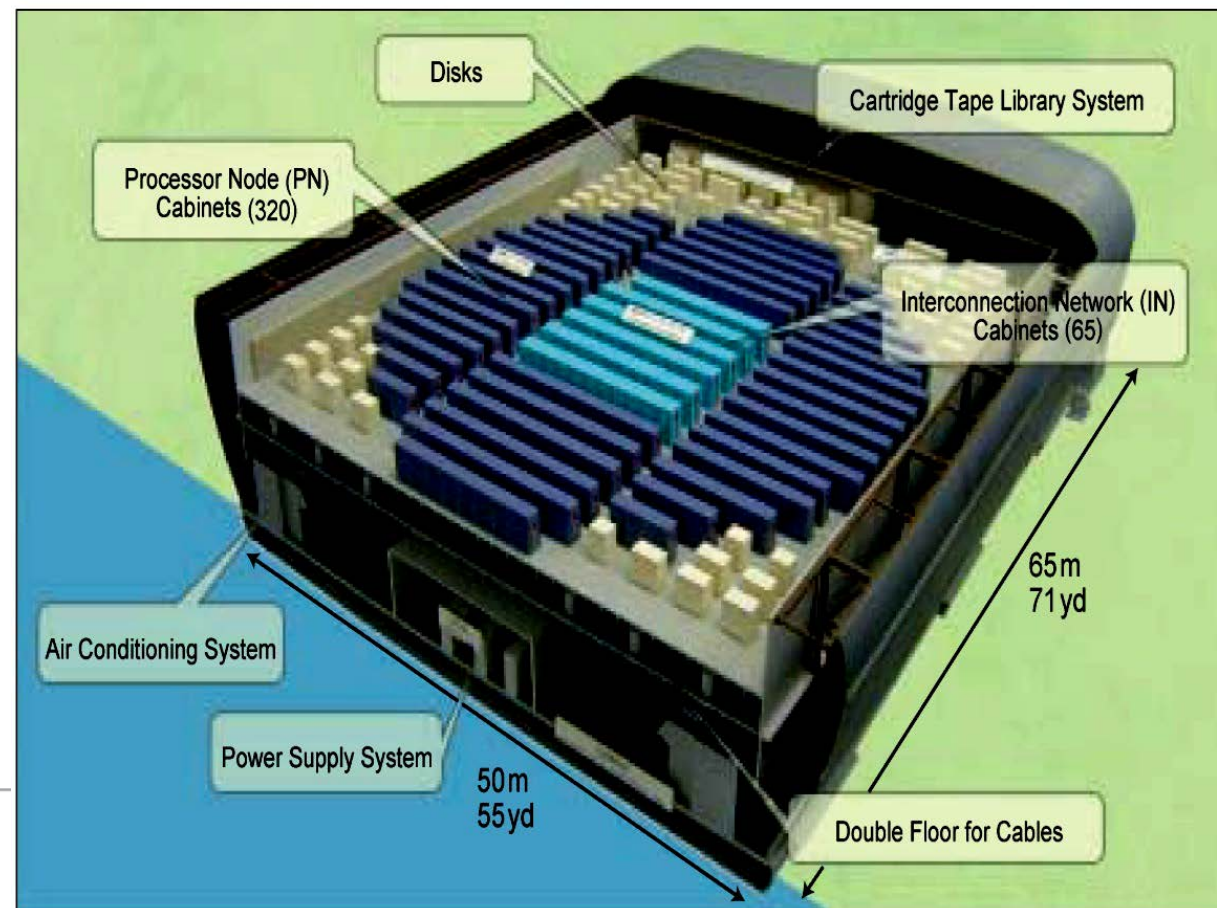
40 TFLOPS Peak (40*10^{12})

35.6 TFLOPS Linpack

PN-07-12/13   PN-08-08/09   PN-09-14/15

OSCAR Technology Corp.

Started up on Feb. 28, 2013:

Licensing the all patents and OSCAR compiler from Waseda Univ.

Founder and CEO: Dr. T. Ono (Ex- CEO of First Section-listed Company, Director of National U., Invited Prof. of Waseda U.)

Executives: Dr. M. Ohashi : COO (Ex- OO of Ono Sokki)

Mr. A. Nodomi : CTO (Ex- Spansion)

Mr. N. Ito (Ex- Visiting Prof. Tokyo Agricult. And Tech. U.)

Dr. K. Shirai (Ex- President of Waseda U., Ex- Chairman of Japanese Open U.)

Mr. K. Ashida (Ex- VP Sumitomo Trading, Adhida Consult. CEO)

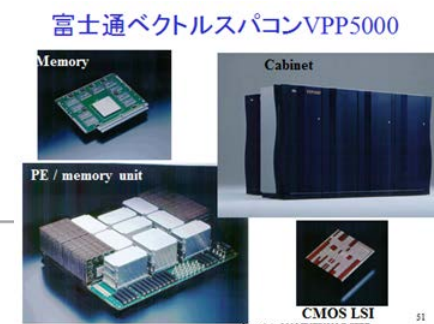**Mr. S. Tsuchida (Co-Chief Investment Officer of Innovation Network Corp. of Japan)**

Auditor: Mr. S. Honda (Ex- Senior VP and General Manager of MUFG)

Dr. S. Matuda (Emeritus Prof. of Waseda U., Chairman of WERU INVESTMENT)

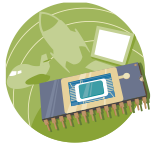**Mr. Y. Hirowatari (President of AGS Consulting)**

Advisors: Prof. H. Kasahara (Waseda U.)

Prof. K. Kimura (Waseda U.)

富士通ベクトルスパコンVPP5000

Memory

Cabinet

PE / memory unit

CMOS LSI

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SEMICON® JAPAN

semi

Future Multicore Products

Next Generation Automobiles

- Safer, more comfortable, energy efficient, environment friendly
- Cameras, radar, car2car communication, internet information integrated brake, steering, engine, moter control

Smart phones

-From everyday recharging to less than once a week
- Solar powered operation in emergency condition
- Keep health

Advanced medical systems

Cancer treatment,
Drinkable inner camera
- Emergency solar powered
- No cooling fun, No dust , clean usable inside OP room

Personal / Regional Supercomputers

Solar powered with more than 100 times power efficient : FLOPS/W
- Regional Disaster Simulators saving lives from tornadoes, localized heavy rain, fires with earth quakes

Summary

- Waseda University Green Computing Systems R&D Center supported by METI has been researching on low-power high performance Green Multicore hardware, software and application with industry including Hitachi, Fujitsu, NEC, Renesas, Denso, Toyota, Olympus and OSCAR Technology.

- OSCAR Automatic Parallelizing and Power Reducing Compiler has succeeded speedup and/or power reduction of scientific applications including "Earthquake Wave Propagation", medical applications including "Cancer Treatment Using Carbon Ion", and "Drinkable Inner Camera", industry application including "Automobile Engine Control", "Smartphone", and "Wireless communication Base Band Processing" on various multicores from different vendors including Intel, ARM, IBM, AMD, Qualcomm, Freescale, Renesas and Fujitsu.

- In automatic parallelization, 110 times speedup for "Earthquake Wave Propagation Simulation" on 128 cores of IBM Power 7 against 1 core, 55 times speedup for "Carbon Ion Radiotherapy Cancer Treatment" on 64cores IBM Power7, 1.95 times for "Automobile Engine Control" on Renesas 2 cores using SH4A or V850, 55 times for "JPEG-XR Encoding for Capsule Inner Cameras" on Tilera 64 cores Tile64 manycore.

  - The compiler will be available on market from OSCAR Technology.

- In automatic power reduction, consumed powers for real-time multi-media applications like Human face detection, H.264, mpeg2 and optical flow were reduced to 1/2 or 1/3 using 3 cores of ARM Cortex A9 and Intel Haswell and 1/4 using Renesas SH4A 8 cores against ordinary single core execution.

- Local memory management for automobiles and software coherent control have been patented and already realized by OSCAR compiler.