OSCAR Vector Multicore System
Platinum Vector Accelerator on FPGA

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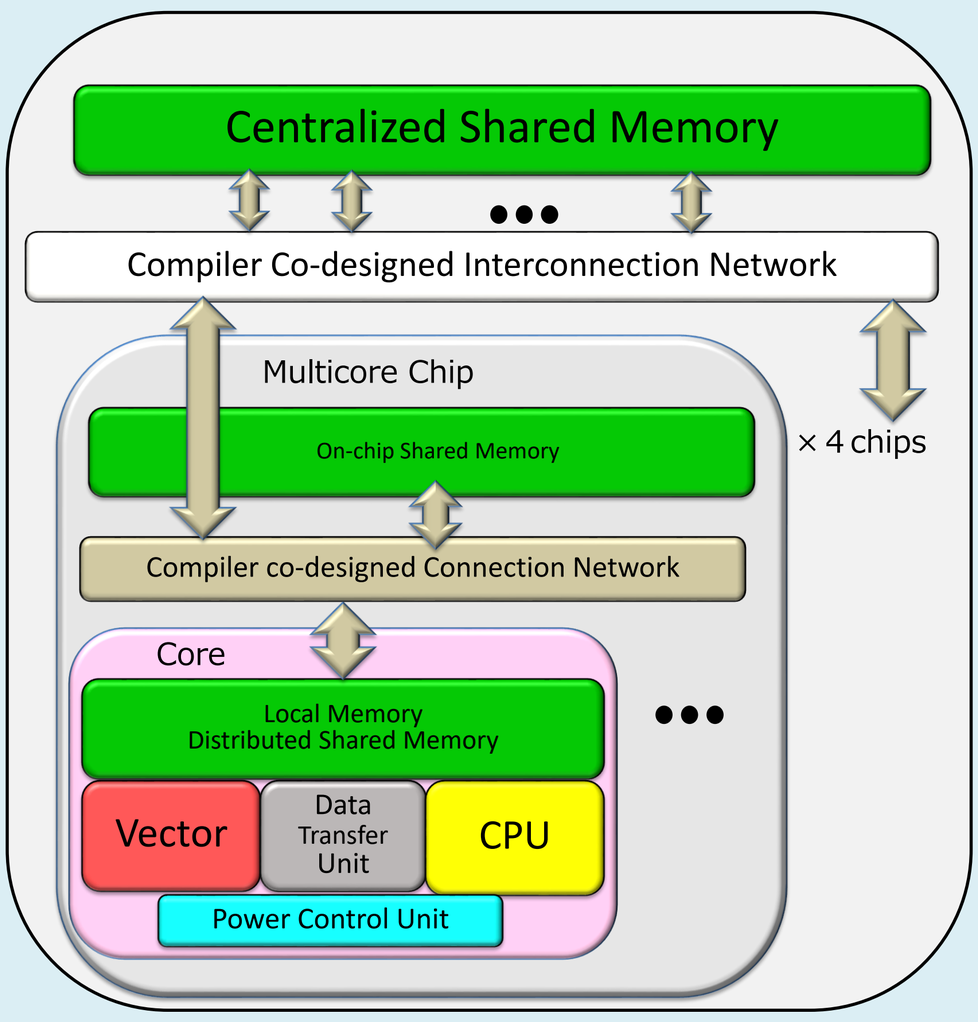
- OSCAR Compiler
- Vector Accelerator
- Clang/LLVM

Platinum Multicore Architecture



FPGA Implementation

Implemented in Altera Arria 10 FPGA

Specification:

- 16 single precision ops/cycle
- Local Data Memory Bandwidth 32 byte/clock
- All data located on Local Data Memory
- Local Data Memory size: 1 MB (current implementation)

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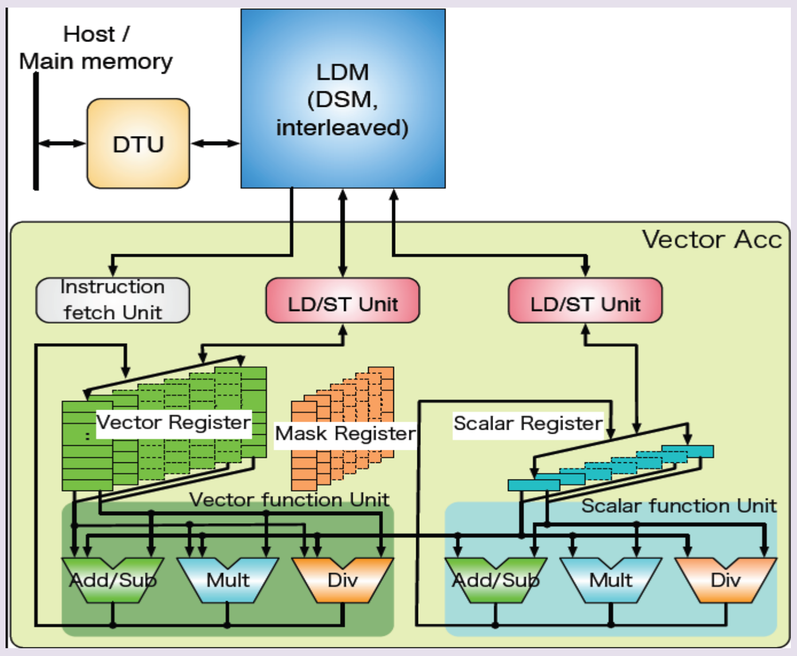
Vector Accelerator

Features

- Attachable for any CPUs (Intel, ARM, IBM)
- Data driven initiation (sync flags)



Function Units [tentative]

- Vector Function Unit
  - 8 double precision ops/clock
  - 64 characters ops/clock
  - Variable vector register length
  - Chaining LD/ST & Vector pipes
- Scalar Function Unit

Registers [tentative]

- Vector Register 256Bytes/entry, 32entry
- Scalar Register 8Bytes/entry
- Floating Point Register 8Bytes/entry
- Mask Register 32Bytes/entry

Performance on FPGA

Performance Evaluation of Vector Accelerator in Altera Arria 10 FPGA

Applications

- Matrix Multiplication:
  - Size: 256x256, Data type: float
- 2D Convolution:
  - Size: 256x256, Data type: float, kernel size:9x9

Compilers

- Vector Accelerator: Manual code generation
- NIOS: nios2-elf-gcc (FPU: FPH2)
- openRISC: GCC 4.1.1
- LEON3: sparc-elf-gcc 4.7.1