

Application Power Control

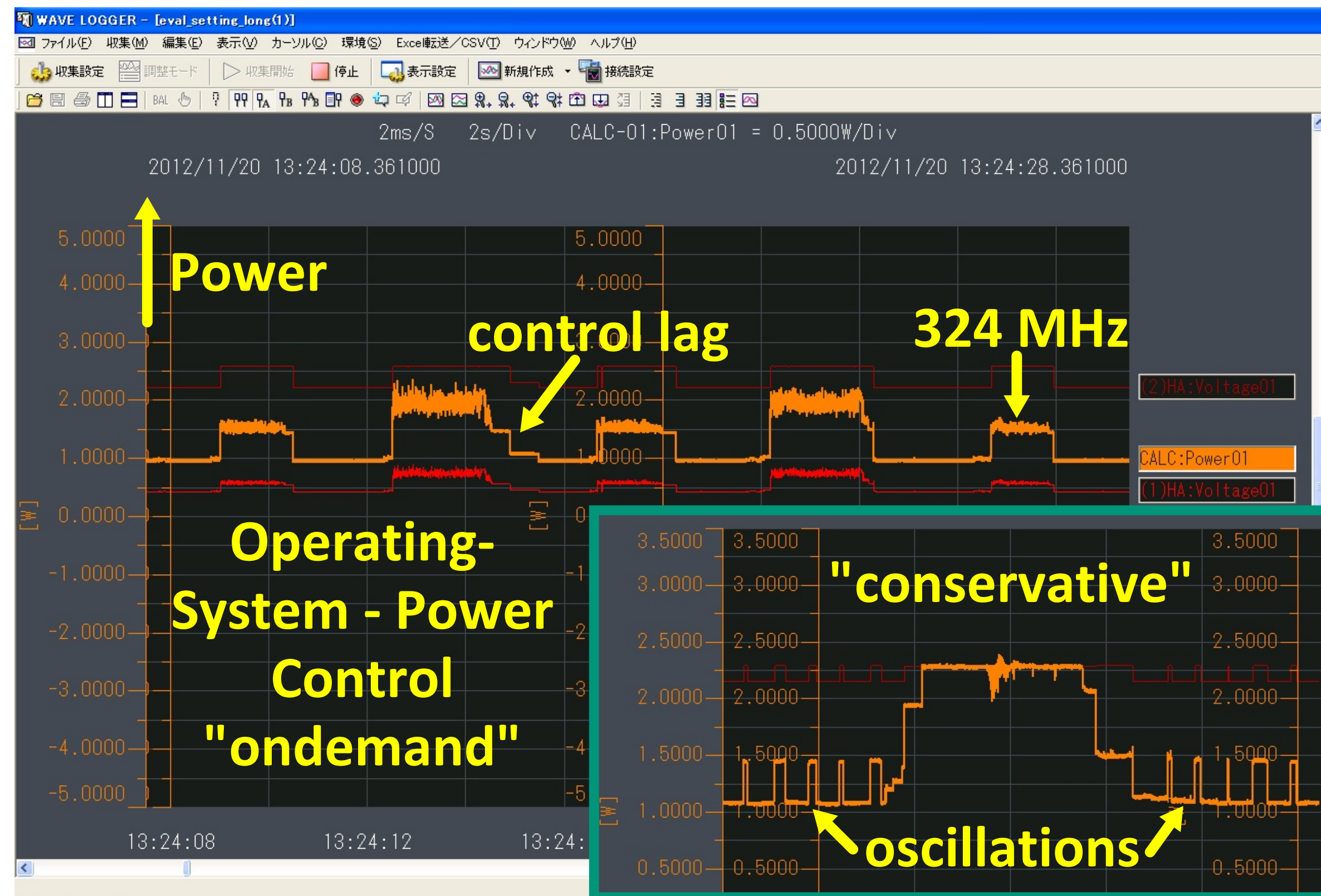
Green Computing Systems R&D Center
Department of Computer Science and Engineering

Opportunities and Challenges of Application-Power Control in the Age of Dark Silicon

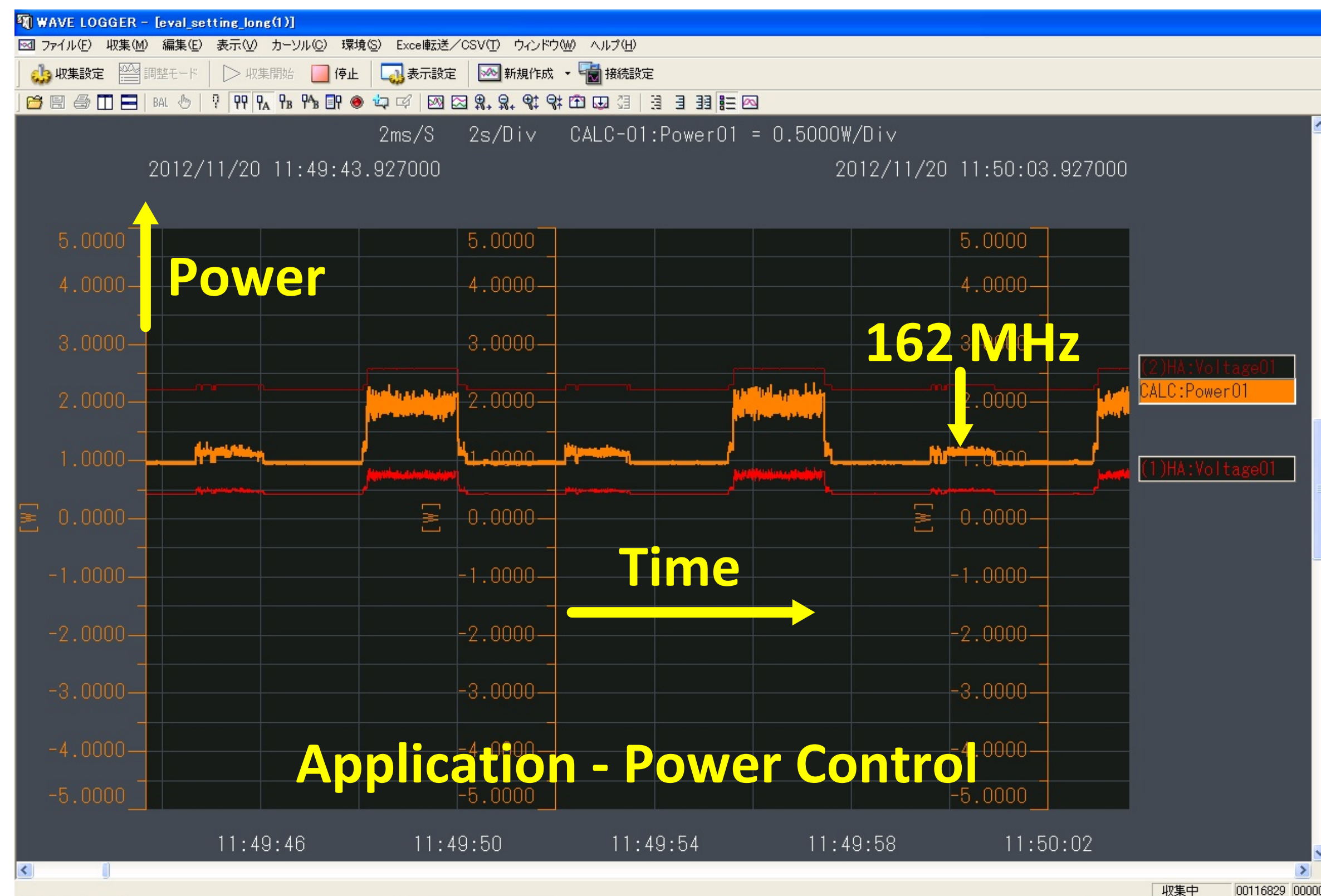
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WASEDA UNIVERSITY

Before: Webserver with **operating system** DFVS-control



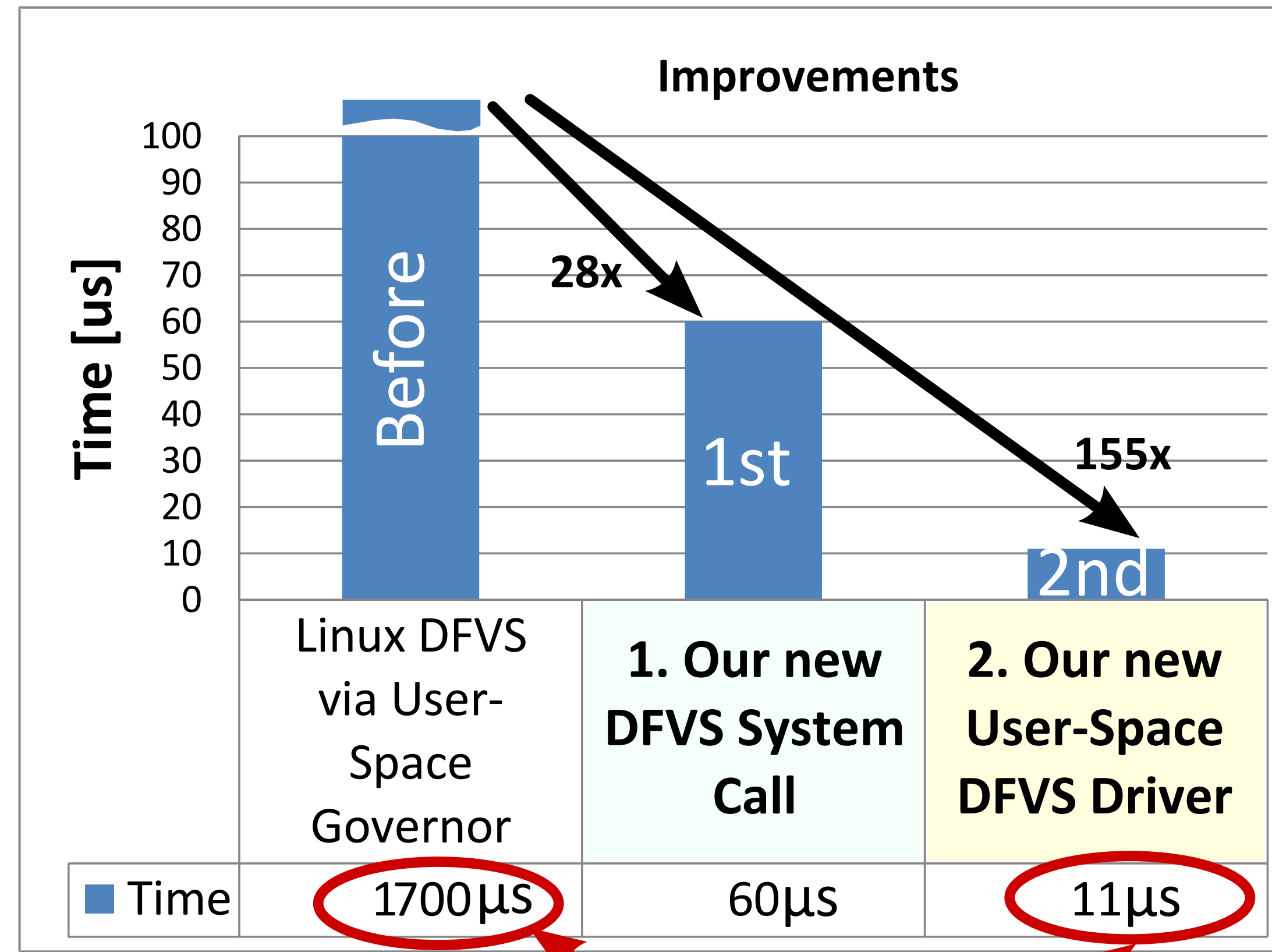
Now: Webserver with **application-level** DFVS-control



DFVS depends on HTTP-transfer type

- compressed @ 648 MHz
- uncompressed @ 162 MHz

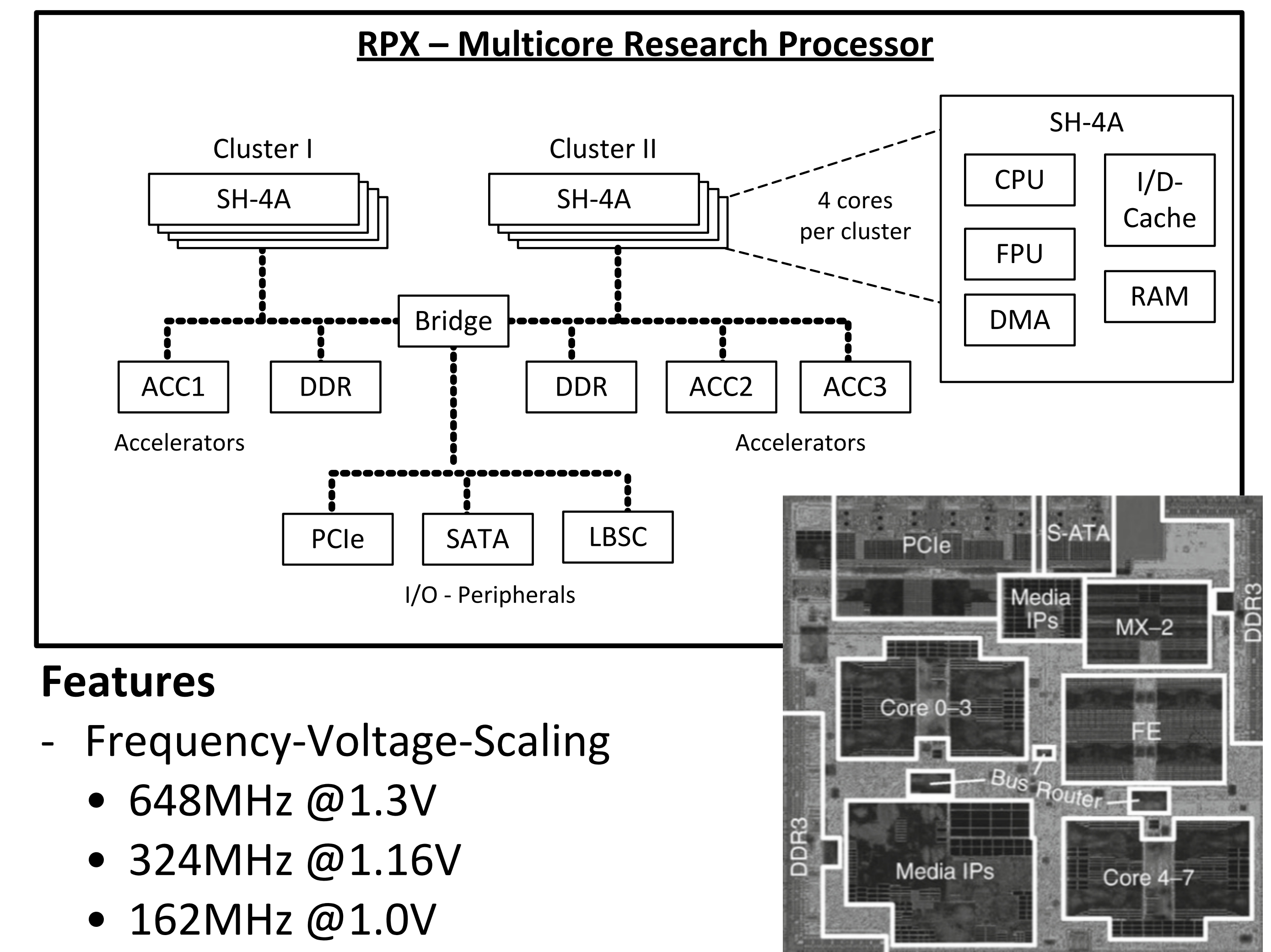
Our Two Approaches to Low Latency DFVS



DFVS Hardware Latency **6 µs**
 System Call **3 µs**
 Clock Gating **0,002 µs**

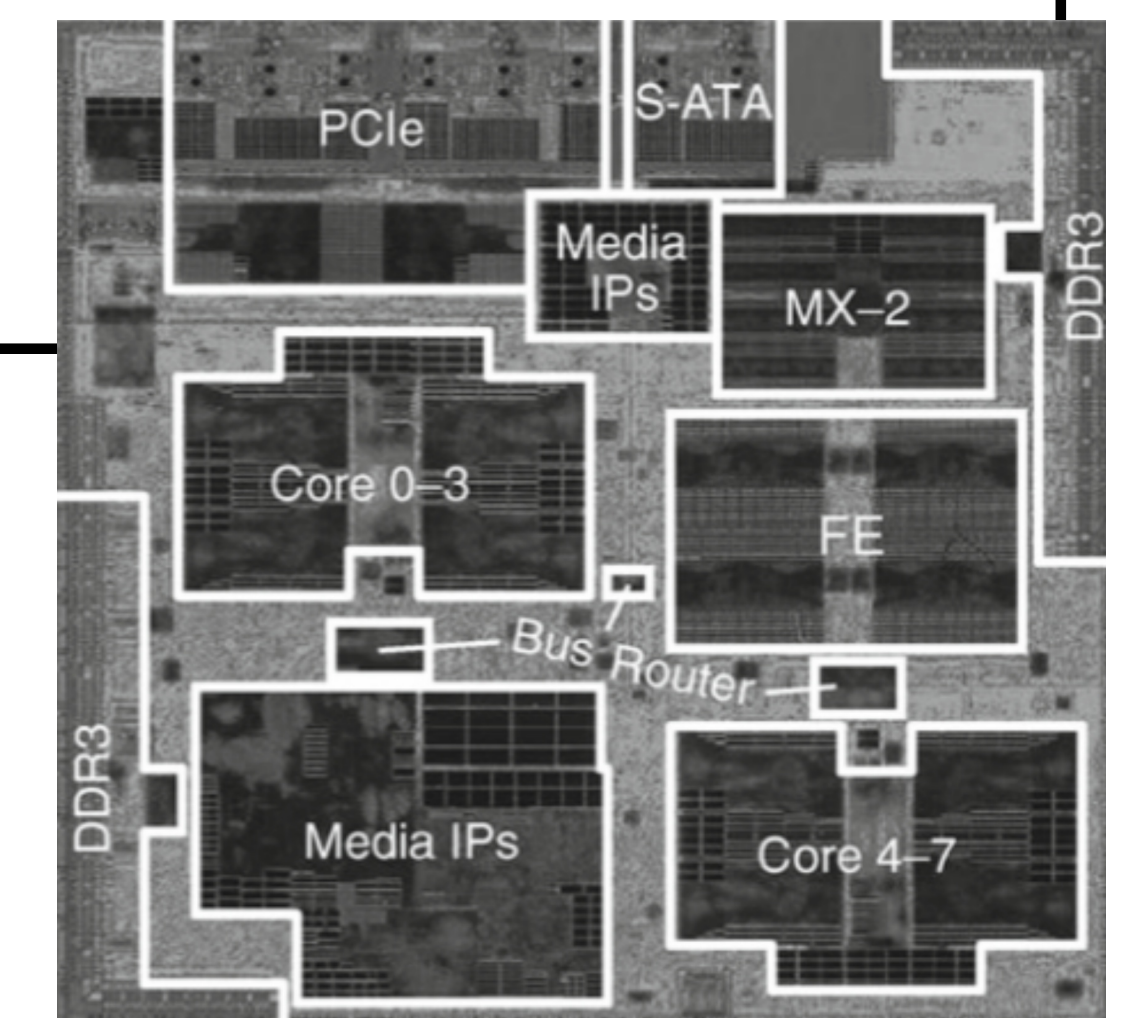
- Low-latency DFVS
- Linux/Android-Kernel
- User-Space Driver

Our Target Architecture

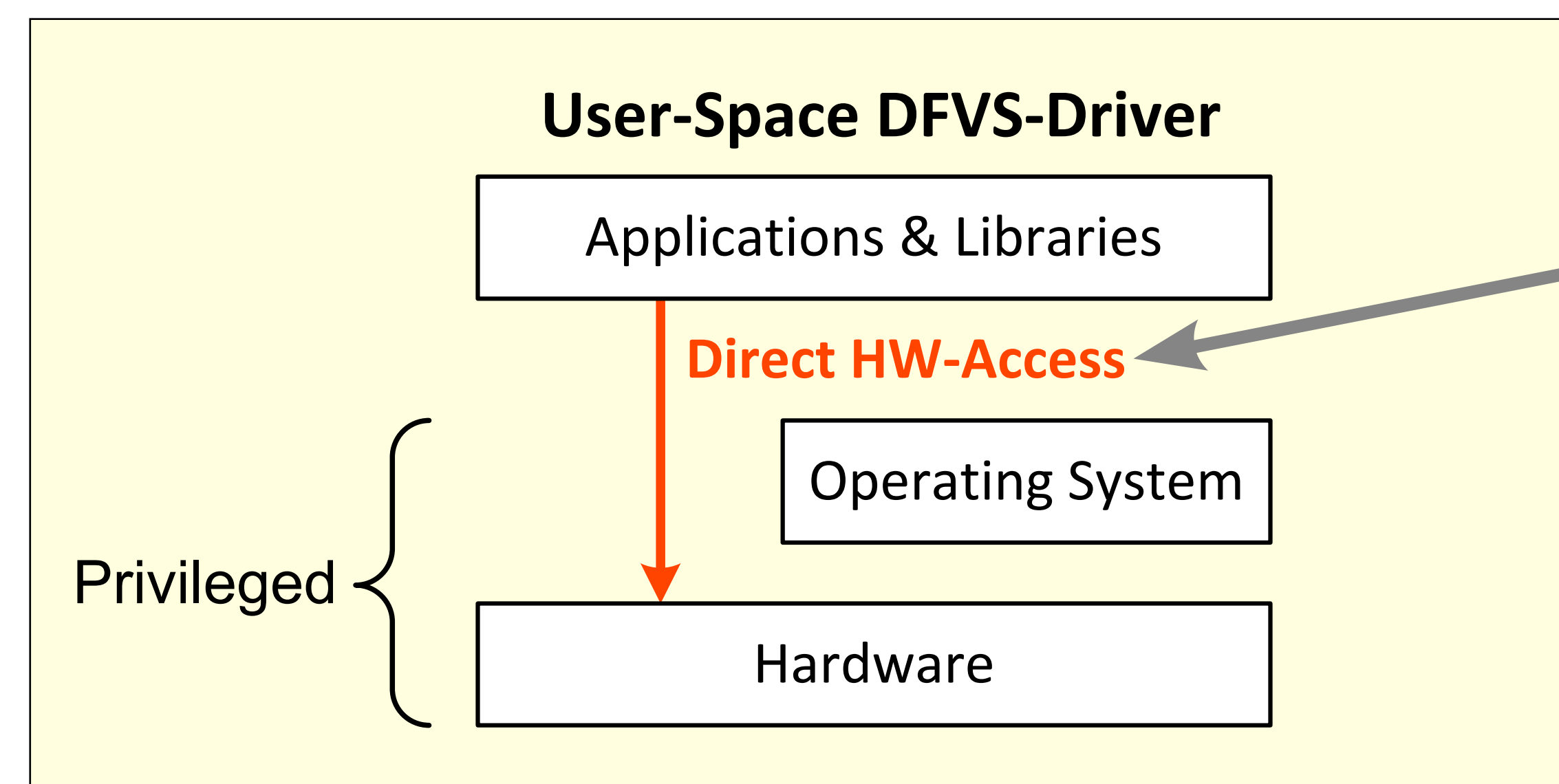
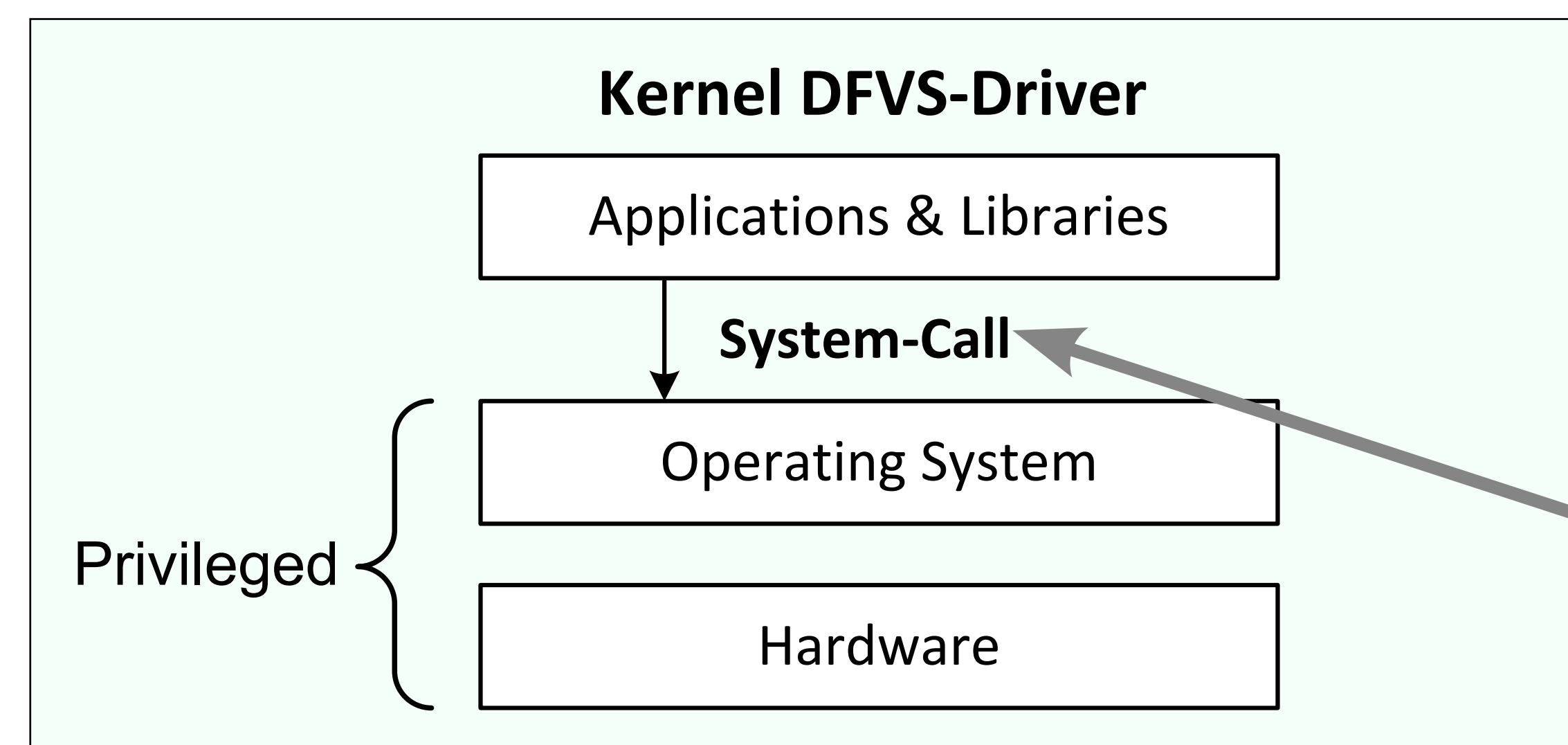


Features

- Frequency-Voltage-Scaling
 - 648MHz @1.3V
 - 324MHz @1.16V
 - 162MHz @1.0V
- Frequency per core
- Fine grained clock/power gating



RPX-Die - 45nm



New System Call

- + Utilizes kernel DFVS-drivers
- + Portable
- + Works across applications

User-Space DFVS-Driver

- + **Very-low latency**
- Temporary inconsistencies → Kernel-driver
- Requires HW/SW-Codesign
- Memory mapped register access on SH4