Multigrain Parallelization of Restricted C Programs on SMP Servers and Low Power Multicores

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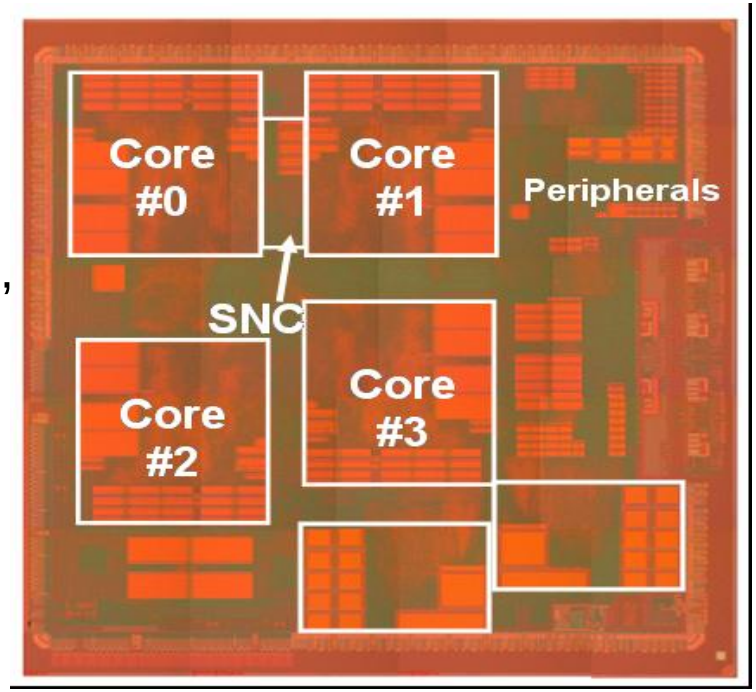
Multicore Everywhere

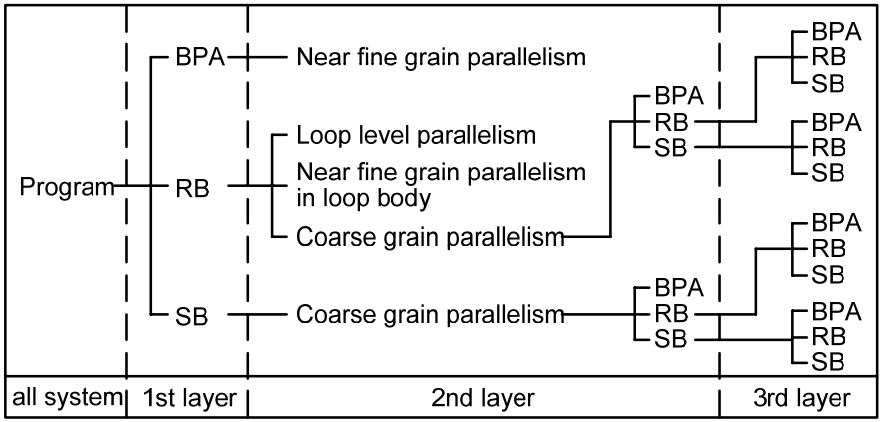
- Multicore from embedded to supercomputer
  - Consumer Electronics (Embedded)
    - Mobile phone, Automotive Navigation,
    - Digital TV, DVD, Camera
  - PCs, Servers
  - Peta-scale supercomputers
- Software productivity
  - Needs for many high quality application software
  - Difficulty in parallel programming
- Advanced parallelizing compiler
  - More parallelism over ILP and Loop parallelism
  - Data locality optimization
  - Minimizing power dissipation



OSCAR Type Multi-core Chip by Renesas in METI/NEDO Multi-core for Real-time Consumer Electronics Project (Leader: Prof. Kasahara)

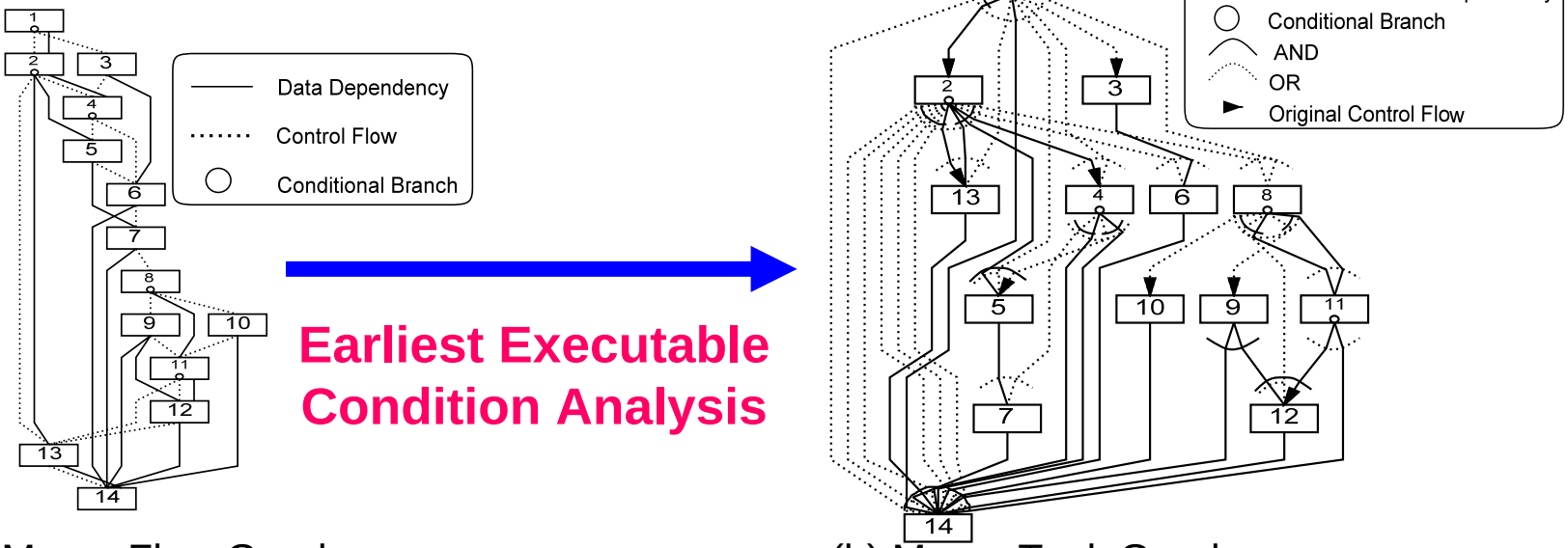
Multigrain Parallelization in OSCAR Compiler

- Hierarchical Macro Task Generation



BPA (Block of Pseudo Assignment)
Basic Blocks
RB (Repetition Block)
Loops
SB (Subroutine Block)
Subroutines

- Exploiting Coarse grain task Parallelism



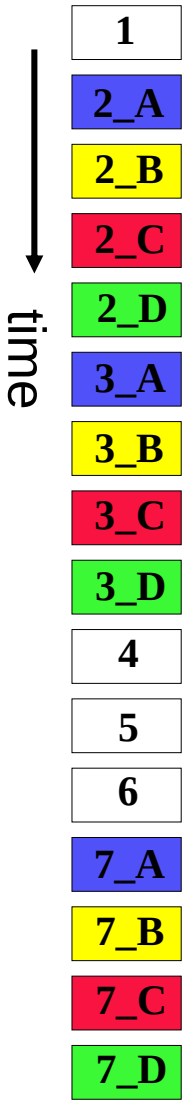
(a) Macro Flow Graph

(b) Macro Task Graph

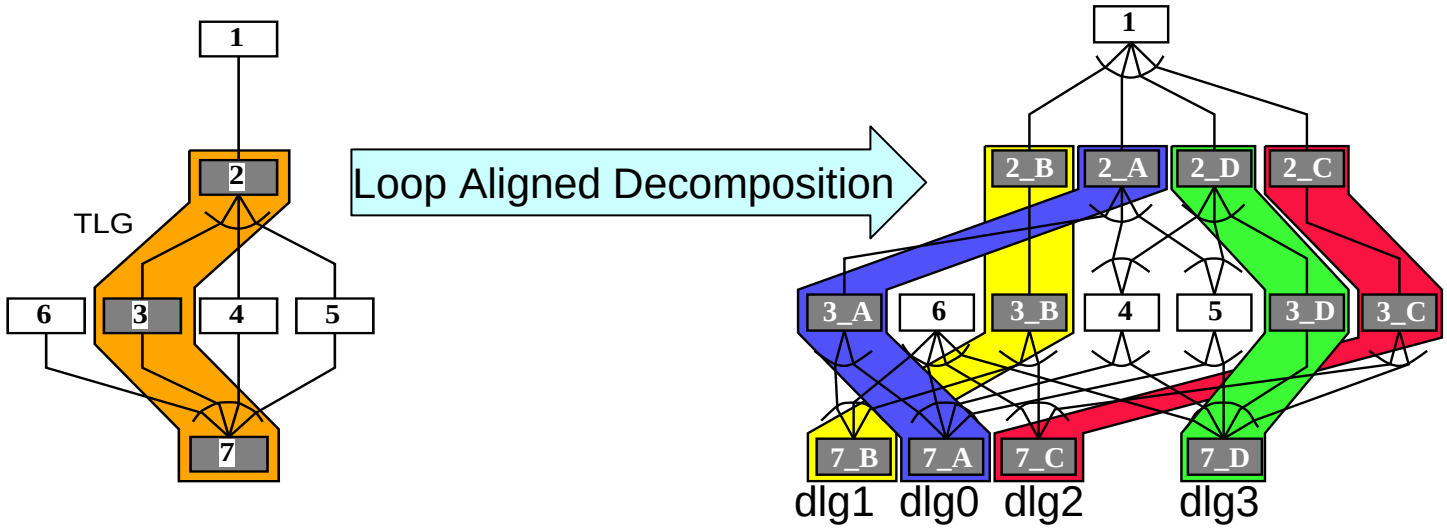
Original execution order on single processor

Data Localization

Scheduled result on single processor

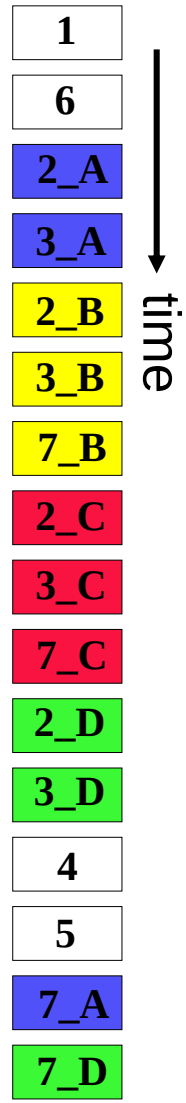


- Exploitation of Data Locality
- Loop Aligned Decomposition (LAD)
- Consecutive MT scheduling
  - Shared data can be passed through processor local memory



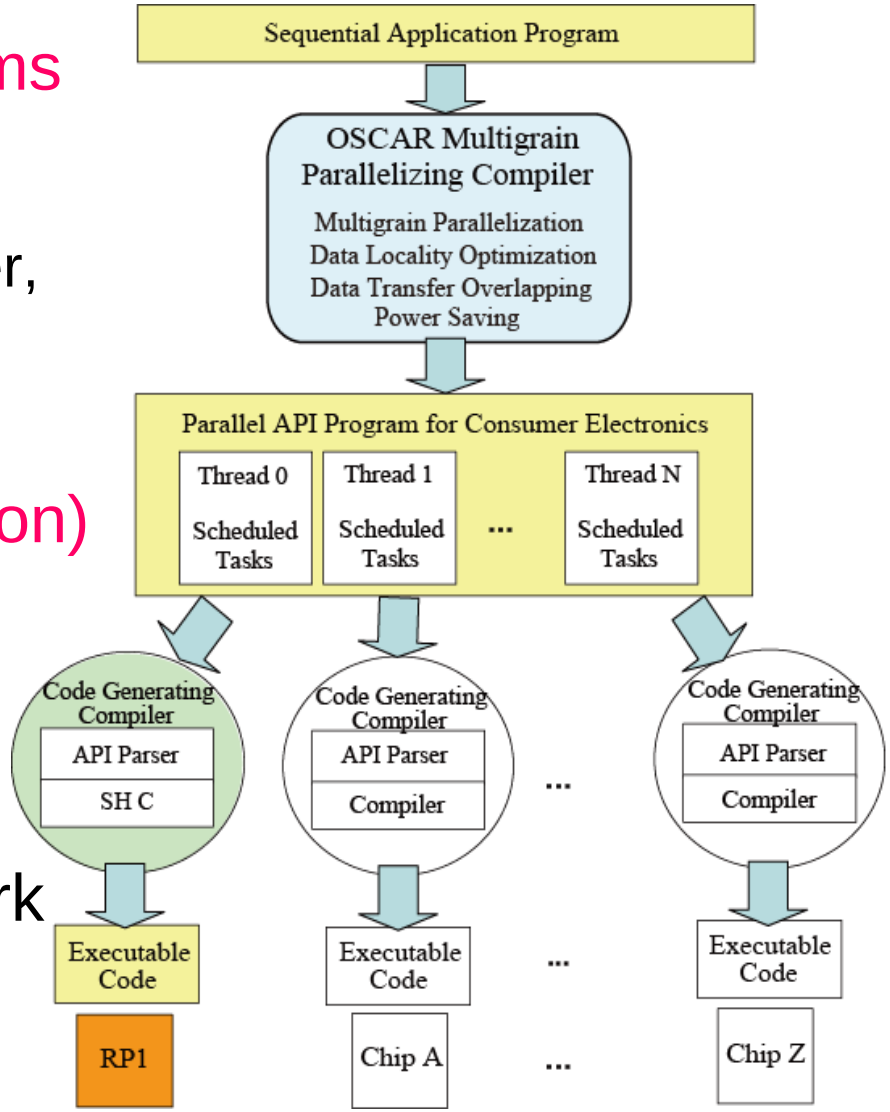
(a) Before loop decomposition

(b) after loop decomposition



Restricted C Language

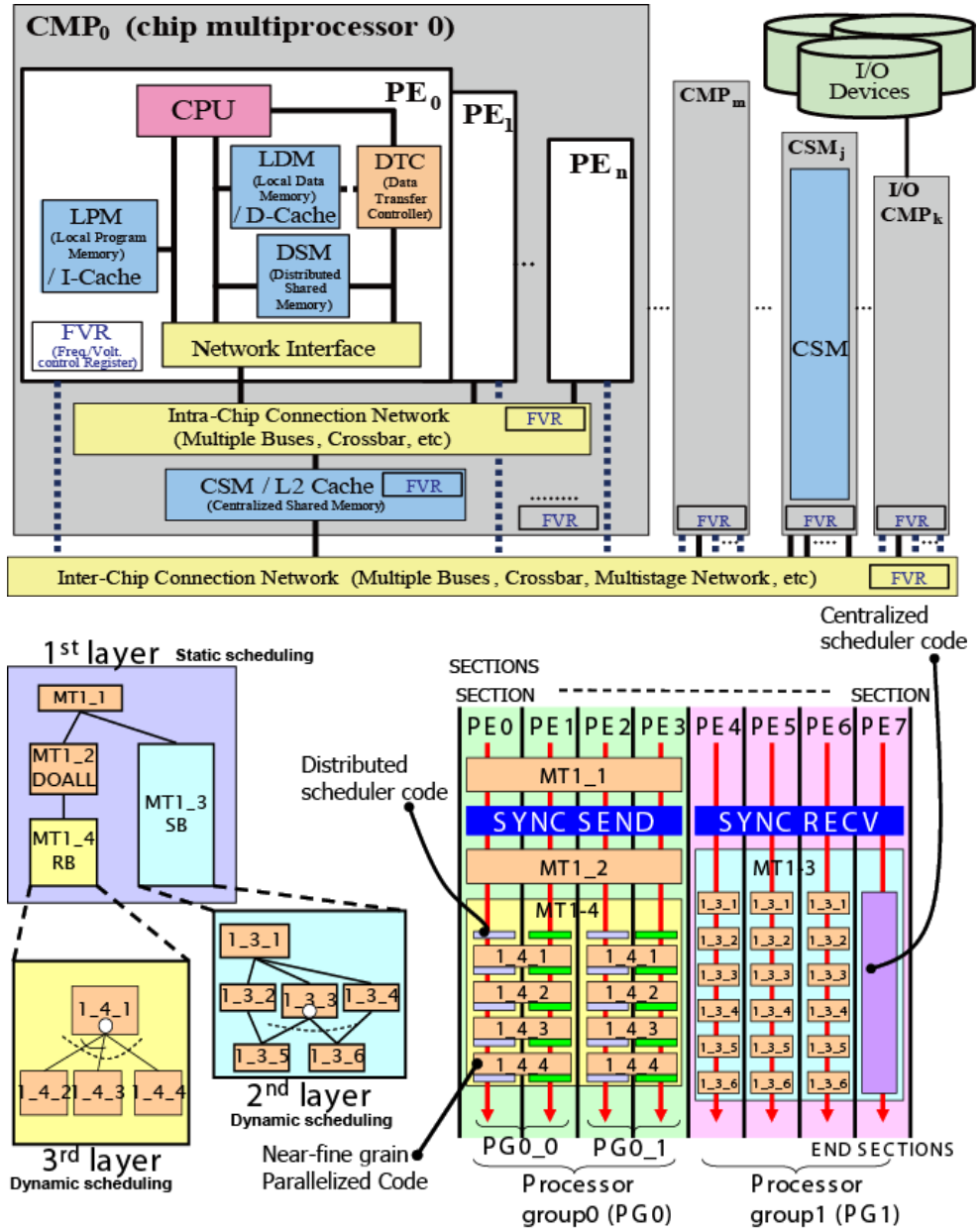
- Compiler-conscious C programs
- Current Applications
  - AAC Encoder, MPEG2 Encoder, MP3 Encoder
  - SPEC2000 art, MiBench susan
- Fortran like C (current restriction)
  - No recursive calls
  - No structures and pointers
- Relaxing restrictions using pointer analysis is a future work



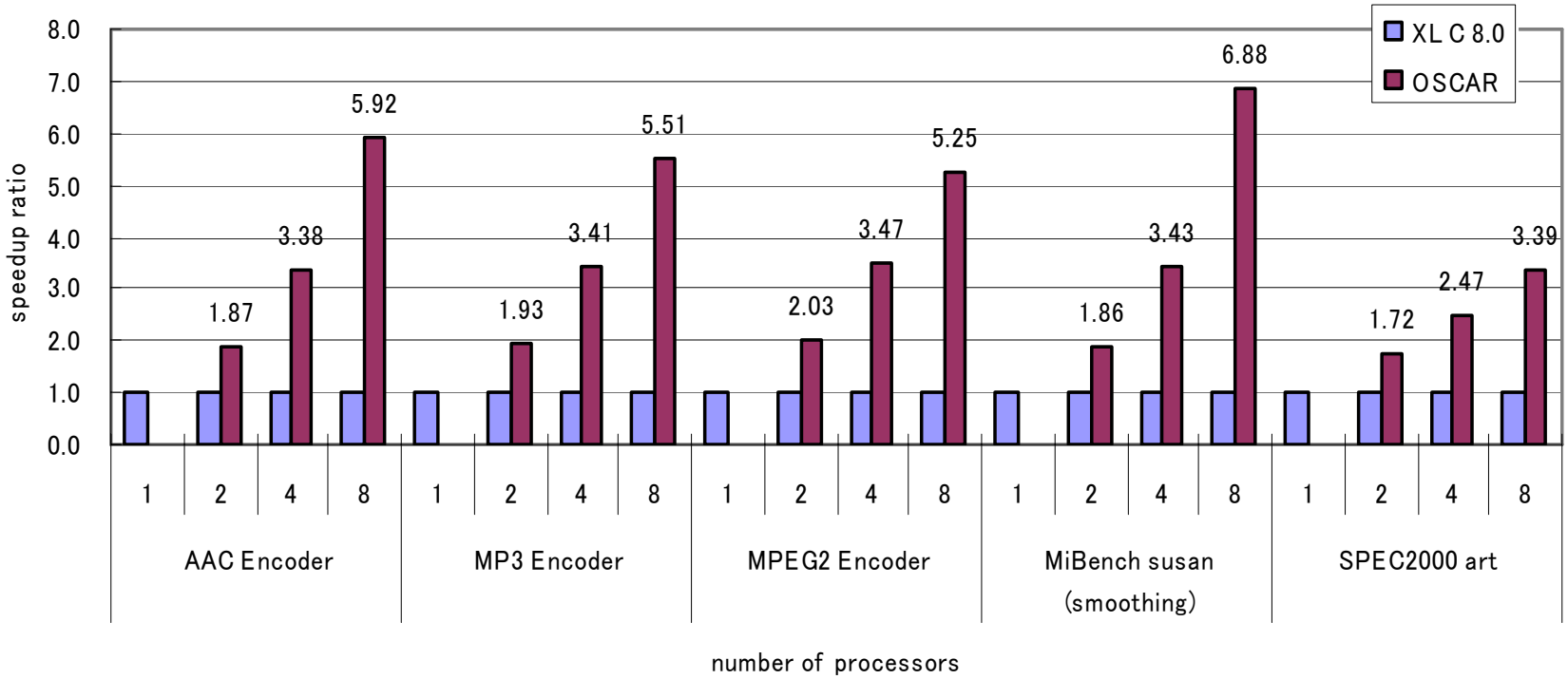
Multicore API for Consumer Electronics

- Aiming common use for multicores from different vendors
  - METI/NEDO “Advanced Multicore for Realtime Consumer Electronics Project”
  - Hitachi, Renesas, Fujitsu, Toshiba, Panasonic, NEC
- Subset of OpenMP directives
  - Thread generation
    - parallel sections directive
  - Synchronization
    - flush directive
  - Critical section
    - critical directive

  SMP Multigrain Parallelization
- Additional directives for
  - Memory mapping of data
  - Data transfer using DTC
  - F/V and Power supply control
    - (currently under evaluation)

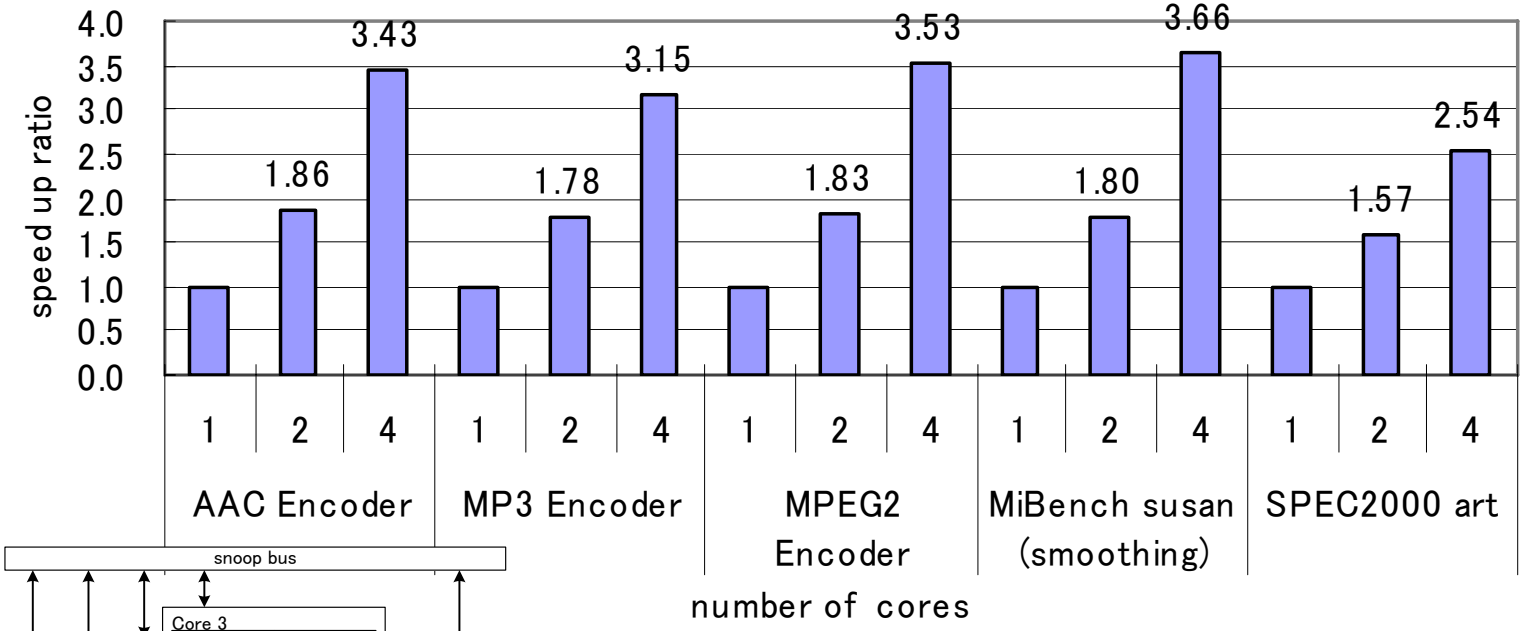


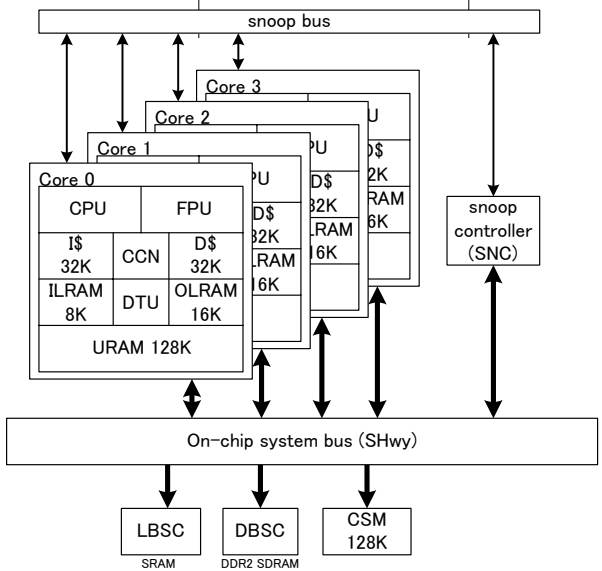
Performance on IBM p5 550Q 8-way SMP Server



Power5+ (1.5GHz) 8 processors (2 cores × 4 chips)
L2 cache 1.9MB / chip (10-way associative)
L3 cache 36MB / chip (12-way associative)

Performance of SMP execution mode on Renesas/Hitachi/Waseda RP1 SH-X3 4 cores Low Power Multicore





SH-X3 4 cores Multicores
- CPU : SH4A 600MHz
- I-Cache : 32kB (4-way set associative) /core
- D-Cache : 32kB (4-way set associative) /core
- Snoop cache (MESI protocol)