OSCAR Automatic Parallelizing Compiler

Automatic Speedup and Power Reduction

Kasahara & Kimura Lab, Waseda University, TOKYO
http://www.kasahara.cs.waseda.ac.jp

Parallel Processing of MATLAB/Simulink by OSCAR Compiler on Intel, ARM & Renesas multi cores

Kasahara & Kimura Lab, Waseda University, TOKYO

- OSCAR Compiler
- MATLAB/Simulink
- Multi grain Parallelization

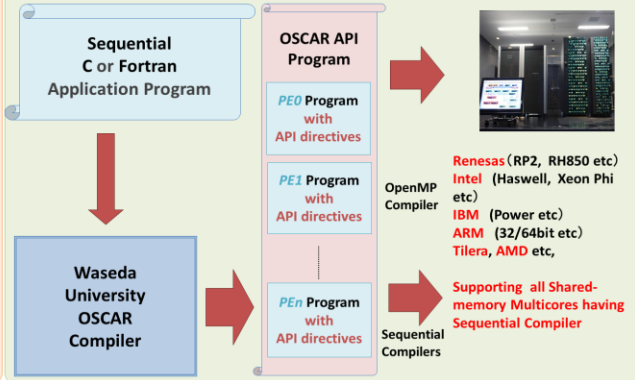
http://www.kasahara.cs.waseda.ac.jp

OSCAR Automatic Parallelizing Compiler

Automatic Parallelized and Power Reduction Software for Embedded to HPC Programs on Multicore

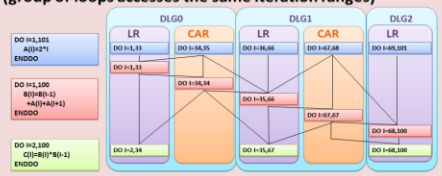
<Application>
Automobile, Medical, Image, Scientific HPC

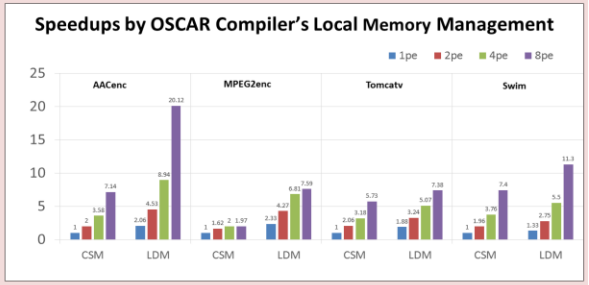
Multi-Platform (ARM, IBM, Intel, Renesas) : OSCAR API



Automatic Localization

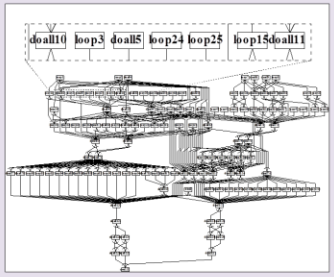
LR: Localizable Region
(data can be passed through LDM)
CAR: Commonly Accessed Region
(possibly data transfers are required among processors)
DLG: Data Localization Group
(group of loops accesses the same iteration ranges)



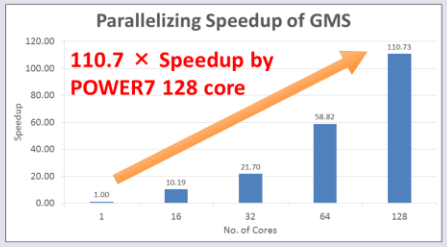


LCPC 2016, "Automatic Local Memory Management ...", Yamamoto et al.

Parallelizing of "National Research Institute for Earth Science and Disaster Resilience" Earthquake Wave Simulation GMS by OSCAR Compiler



Task graph of OSCAR API Program

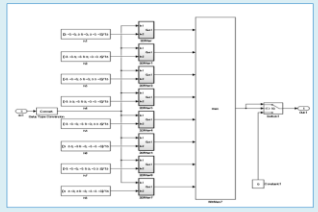


Execution environment: Hitachi SR16000 Model VM1 (IBM POWER7 Processor: 128core)

SC16 members

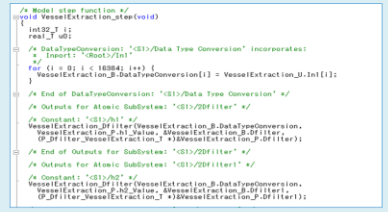
A.Maruoka
Y.Mushu
S.Karino
K.Miyamoto
T.Kawata
K.Yamamoto
T.Shirakawa
Y.Oki
T.Kitamura
M.Takamura
K.Kimura
H.Kasahara

Automatic Parallelization of MATLAB/Simulink by OSCAR Compiler

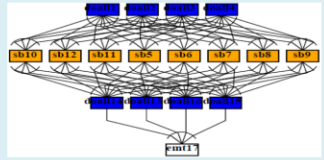


Simulink model

Generate C code using Embedded Coder

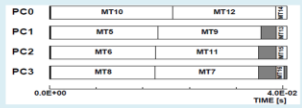


C code

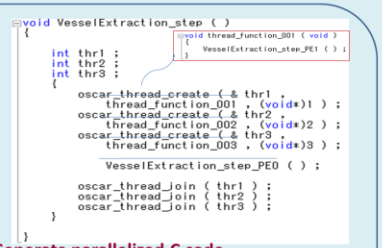


(1)Generate MTG → Parallelism

OSCAR Compiler

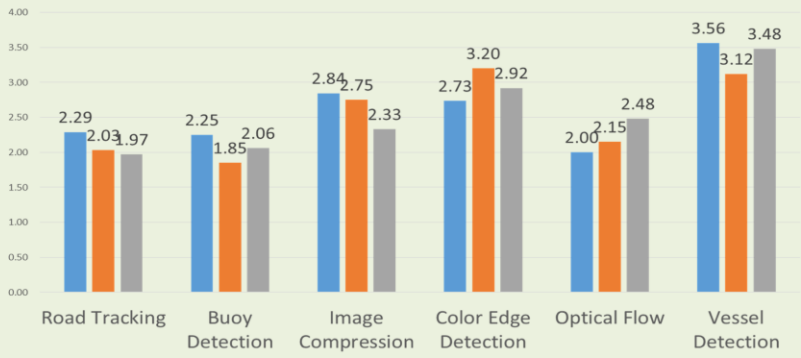


(2) Generate gantt chart → Scheduling in a multicore



(3) Generate parallelized C code using the OSCAR API → Multiplatform execution (Intel, ARM and SH etc)

Speedups of MATLAB/Simulink Image Processing on Various 4core Multicores (Intel Xeon, ARM Cortex A15 and Renesas SH4A)



Road Tracking, Image Compression : http://www.mathworks.co.jp/jp/help/vision/examples
Buoy Detection : http://www.mathworks.co.jp/matlabcentral/fileexchange/44706-buoy-detection-using-simulink
Color Edge Detection : http://www.mathworks.co.jp/matlabcentral/fileexchange/28114-fast-edges-of-a-color-image--actual-color--not-converting-to-grayscale-/
Vessel Detection : http://www.mathworks.co.jp/matlabcentral/fileexchange/24990-retinal-blood-vessel-extraction/

OSCAR Vector Multicore System & Parallelizing / Vectorizing Compiler

Kasahara & Kimura Lab, Waseda University, TOKYO
http://www.kasahara.cs.waseda.ac.jp

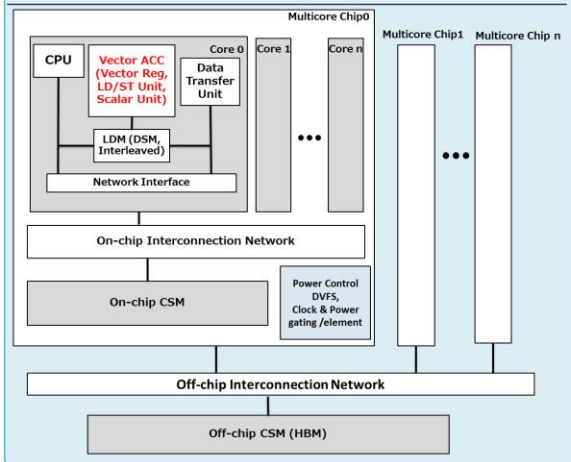
■OSCAR Compiler
■Vector Accelerator
■Clang/LLVM

Power Reduction of Face Recognition on Intel Haswell 3 cores by OSCAR Compiler - Reduced Power to 2/5 on Intel-

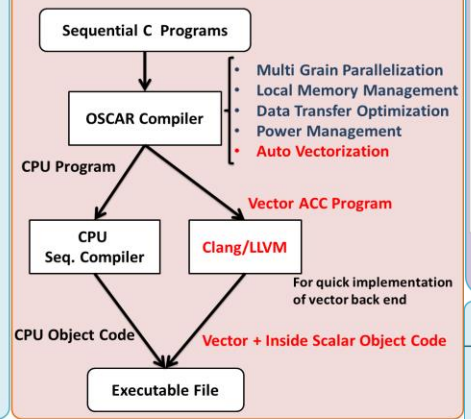
Kasahara & Kimura Lab, Waseda University, TOKYO
http://www.kasahara.cs.waseda.ac.jp

■OSCAR Compiler
■Intel Haswell
■Power Reduction

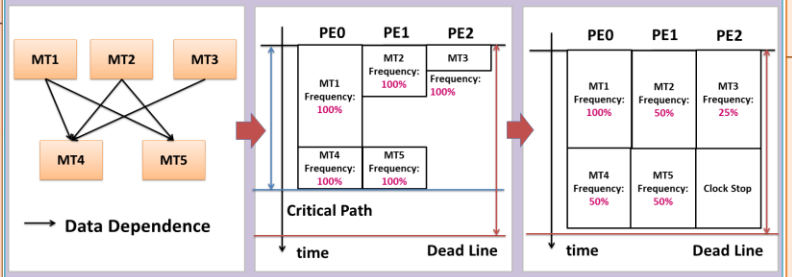
Platinum Multicore Architecture



OSCAR Compiler Flow w/ OSCAR API



Saving Energy by Compiler



Task graph | Tasks assigned to 3 cores | Schedule Minimizing Power

Face Recognition program

Detecting Human Face in Input Image from Camera and ○ Marking

Measuring Environment

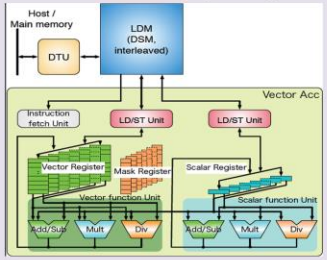
CPU : Intel Core i7 4770K
No. of Cores : 4
Frequency : 3.5GHz～0.8GHz
Motherboard : ASUS H81M-A

Measuring current from CPU power source

Vector Accelerator

Features

- Attachable for any CPUs (Intel, ARM, IBM)
- Data driven initiation by sync flags



Function Units [tentative]

- Vector Function Unit
  - 8 double precision ops/clock
  - 64 characters ops/clock
  - Variable vector register length
  - Chaining LD/ST & Vector pipes
- Scalar Function Unit

Registers[tentative]

- Vector Register 256Bytes/entry, 32entry
- Scalar Register 8Bytes/entry
- Floating Point Register 8Bytes/entry
- Mask Register 32Bytes/entry

Performance w/ OSCAR Simulator

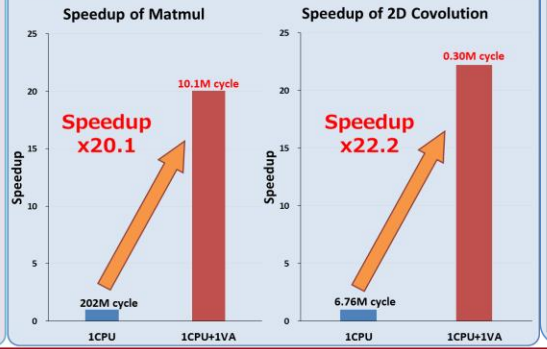
Evaluate performance of Vector Accelerator with cycle accurate simulator

Simulation Settings

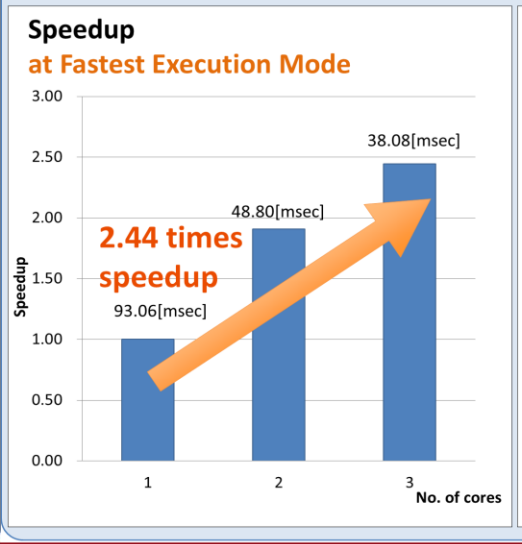
- 16 single precision ops/cycle
- Local Data Memory Bandwidth 32 byte/clock
- All data located on Local Data Memory in initial state

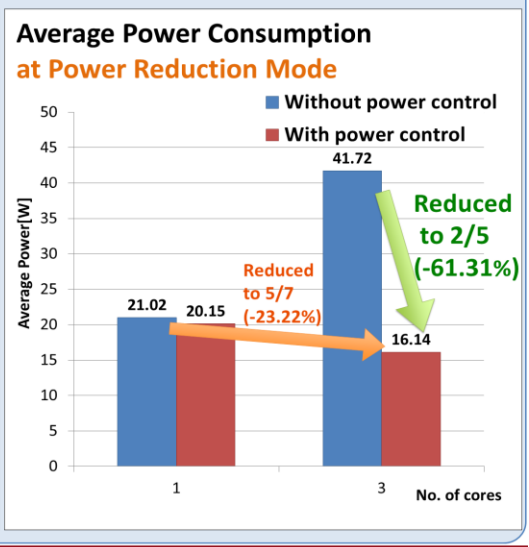
Applications

- Matmul:
  - Size:256x256, Data type: float
- 2D Convolution:
  - Size:256x256, Data type: float, kernel size:3x3



Speedup and Power reduction on Intel Haswell 3 Cores





SC16