OSCAR Parallelizing Compiler and Its Performance for Embedded Applications

Hironori Kasahara
Professor, Dept. of Computer Science & Engineering
Director, Advanced Multicore Processor Research Institute
Waseda University, Tokyo, Japan
IEEE Computer Society Board of Governors
IEEE Computer Society Multicore STC Chair
URL: http://www.kasahara.cs.waseda.ac.jp/
Industry-government-academia collaboration in R&D and target practical applications

- Solar Powered Smart phones
- Cameras
- Robots
- Cool desktop servers
- Consumer electronic Internet TV/DVD
- On-board vehicle technology (navigation systems, integrated controllers, infrastructure coordination)
- Camcorders
- Capsule inner cameras
- Solar Powered Smart phones: Operation/recharging by solar cells
- Medical servers: Heavy particle radiation planning, cerebral infarction
- Non-fan, cool, quiet servers designed for server
- Waseda University: R&D
- Many-core system technologies with ultra-low power consumption
- OSCAR many-core chip
- Stock trading
- Cool desktop servers
- Super real-time disaster simulation (tectonic shifts, tsunami, tornado, flood, fire spreading)
- Green cloud servers
- Green supercomputers
- Industry
- Intelligent home appliances
- Supercomputers and servers
- Protect lives
- Protect environment
- For smart life
- Protect environment
- National Institute of Radiological Sciences
- For smart life
- Many-core system technologies with ultra-low power consumption
- Many-core system technologies with ultra-low power consumption
- Waseda University: R&D
To improve **effective performance**, **cost-performance** and **software productivity** and reduce power.

**Multigrain Parallelization**
- coarse-grain parallelism among loops and subroutines, **near fine grain parallelism** among statements in addition to loop parallelism

**Data Localization**
- Automatic data management for distributed shared memory, cache and local memory

**Data Transfer Overlapping**
- Data transfer overlapping using Data Transfer Controllers (DMAs)

**Power Reduction**
- Reduction of consumed power by compiler control DVFS and Power gating with hardware supports.
Multicore Program Development Using OSCAR API V2.0

Sequential Application Program in Fortran or C
(Consumer Electronics, Automobiles, Medical, Scientific computation, etc.)

Manual parallelization / power reduction

Accelerator Compiler/ User
Add “hint” directives before a loop or a function to specify it is executable by the accelerator with how many clocks

Waseda OSCAR Parallelizing Compiler
- Coarse grain task parallelization
- Data Localization
- DMAC data transfer
- Power reduction using DVFS, Clock/ Power gating

Low Power Homogeneous Multicore Code Generation
- Proc0
  - Code with directives Thread 0
- Proc1
  - Code with directives Thread 1
  - Accelerator 1
    - Code
  - Accelerator 2
    - Code

Low Power Heterogeneous Multicore Code Generation
- Existing sequential compiler
- API Analyzer
- OSCAR API for Homogeneous and/or Heterogeneous Multicores and manycores
  - Directives for thread generation, memory, data transfer using DMA, power managements

Parallelized API F or C program
- OpenMP Compiler

Server Code Generation

Generation of parallel machine codes using sequential compilers

OSCAR: Optimally Scheduled Advanced Multiprocessor API: Application Program Interface

Executable on various multicores

Hitachi, Renesas, NEC, Fujitsu, Toshiba, Denso, Olympus, Mitsubishi, Esol, Cats, Gaio, 3 univ.
Though so far parallel processing of the engine control on multicore has been very difficult, Denso and Waseda succeeded 1.95 times speedup on 2core V850 multicore processor.
Speedup with 2cores for Engine Crankshaft Handwritten Program on RPX Multi-core Processor

Macrotask graph with plenty of conditional branches

Macrotask graph after task fusion

Speed up against 1core
Automatic Parallelization of Still Image Encoding Using JPEG-XR for the Next Generation Cameras and Drinkable Inner Camera

- TILEPro64

55 times speedup with 64 cores against 1 core
Parallel Processing of Face Detection on Manycore, Highend and PC Server

- OSCAR compiler gives us **11.55 times** speedup for 16 cores against 1 core on SR16000 Power7 highend server.
Performance of OSCAR Compiler & API on 2 ARMv7-cores Qualcomm MSM8960 (Snapdragon) Android 4.0 for Smart Phones

1.81 times speedup by 2 cores on the average against 1 core
Parallel Processing Performance on 3Cores NaviEngine with Realtime OS eT-Kernel Multi-Core Edition

NaviEngine (ARM11 MPCore) 400MHz 3 core SMP (Renesas Electronics EC-4260)

- 2.37 times speedup on 3ARM cores against 1 core
Power Reduction of MPEG2 Decoding to 1/4 on 8 Core Homogeneous Multicore RP-2 by OSCAR Parallelizing Compiler

MPEG2 Decoding with 8 CPU cores

Without Power Control
(Voltage : 1.4V)

With Power Control
(Frequency,
Resume Standby:
Power shutdown & Voltage lowering 1.4V-1.0V)

Avg. Power
5.73 [W] 73.5% Power Reduction 1.52 [W]

11
Future Multicore Products

Next Generation Automobiles
- Safer, more comfortable, energy efficient, environment friendly
- Cameras, radar, car2car communication, internet information integrated brake, steering, engine, motor control

Smart phones
- From everyday recharging to less than once a week
- Solar powered operation in emergency condition
- Keep health

Advanced medical systems
Cancer treatment, Drinkable inner camera
- Emergency solar powered
- No cooling fun, No dust, clean usable inside OP room

Personal / Regional Supercomputers
Solar powered with more than 100 times power efficient: FLOPS/W
- Regional Disaster Simulators saving lives from tornadoes, localized heavy rain, fires with earth quakes

- From everyday recharging to less than once a week
- Solar powered operation in emergency condition
- Keep health