How is specifically multicore programming different from traditional parallel computing?

Hironori Kasahara

Professor, Department of Computer Science

Director, Advanced Chip-Multiprocessor Research Institute

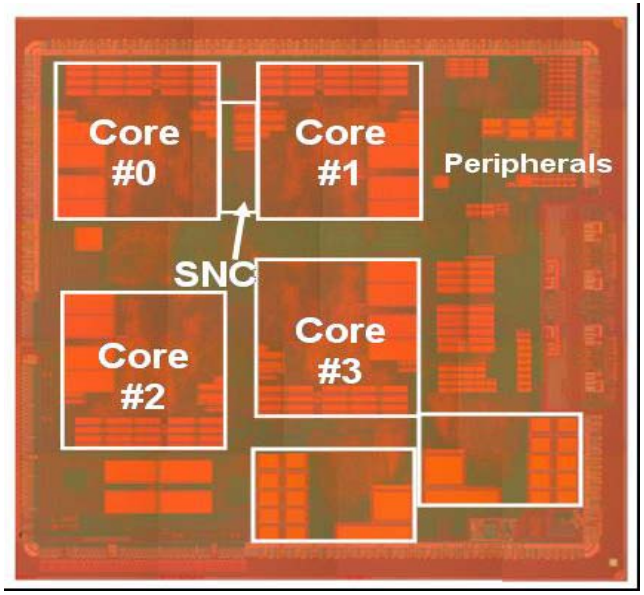
Waseda University

Tokyo, Japan

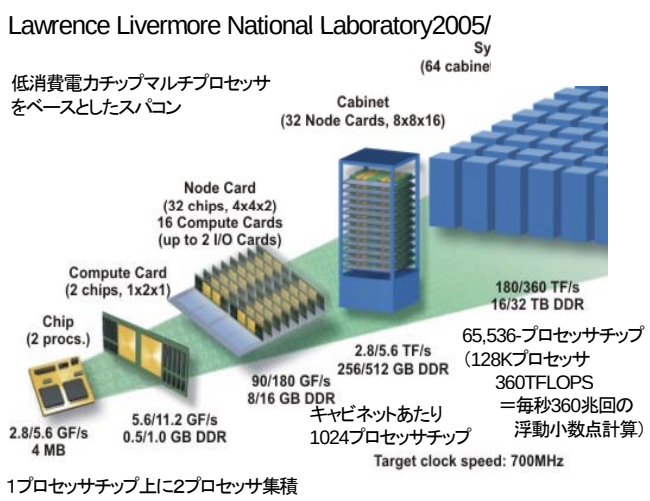
http://www.kasahara.cs.waseda.ac.jp

October 11, 2007, 13:00 to 14:00, 20th LCPC, UIUC

Multi-core Everywhere



OSCAR Type Multi-core Chip by Renesas in METI/NEDO Multicore for Real-time Consumer Electronics Project (Leader: Prof.Kasahara)



Multi-core from embedded to supercomputers

- **Consumer Electronics (Embedded)**
  - Mobile Phone, Game, Digital TV, Car Navi, DVD,
  - IBM/ Sony/ Toshiba Cell, Fuijtsu FR1000,
  - NEC/ARMMPCore&MP211, Panasonic Uniphier,
  - Renesas SH multi-core(RP1)
- **PCs, Servers**
  - Intel Dual-Core Xeon, Core 2 Duo, Montecito
  - AMD Quad and Dual-Core Opteron
- **WSs, Deskside & Highend Servers**
  - IBM Power4,5,5+, pSeries690(32way), p5 550Q(8 way) ,
  - Sun N iagara(SparcT1,T2), SGI ALTIX350,
- **Supercomputers**
  - IBM Blue Gene/L: 360TFLOPS, 2005, (BG/P, 2007?)
    - Low power CMP based 128K processor chips

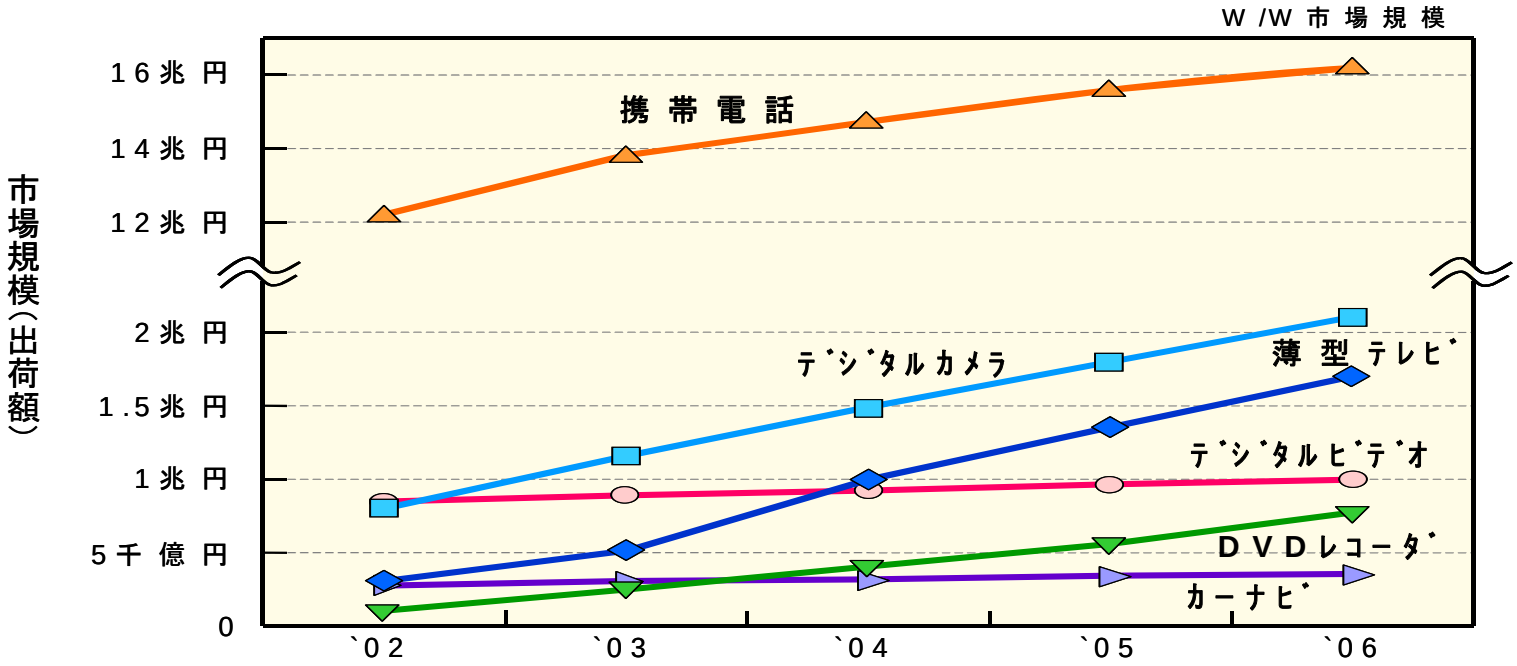
Huge number of parallel applications must be developed in a few years

→ Best programming method?

Sequential programming which can be easily parallelized by compiler

Ex.) Restricted C without pointers and recursive calls

Market of Consumer Electronics 1 Trillion Dollars in 2010 (World Wide)



		‘03	‘07	年平均成長率%
Dig. Camera	デジタルスチルカメラ(M台)	49	76	12
Dig. TV	デジタルTV(M台)	6	27	45
DVD Recorder	DVDレコーダ(M台)	3.6	33	74
DVD for PC	PC用DVD(記録型)(M台)	27	114	43
Mobile Phone	携帯電話(M台)	490	670	8
LSI for Cars	自動車用半導体需要(B$)	14.0	20.9	11

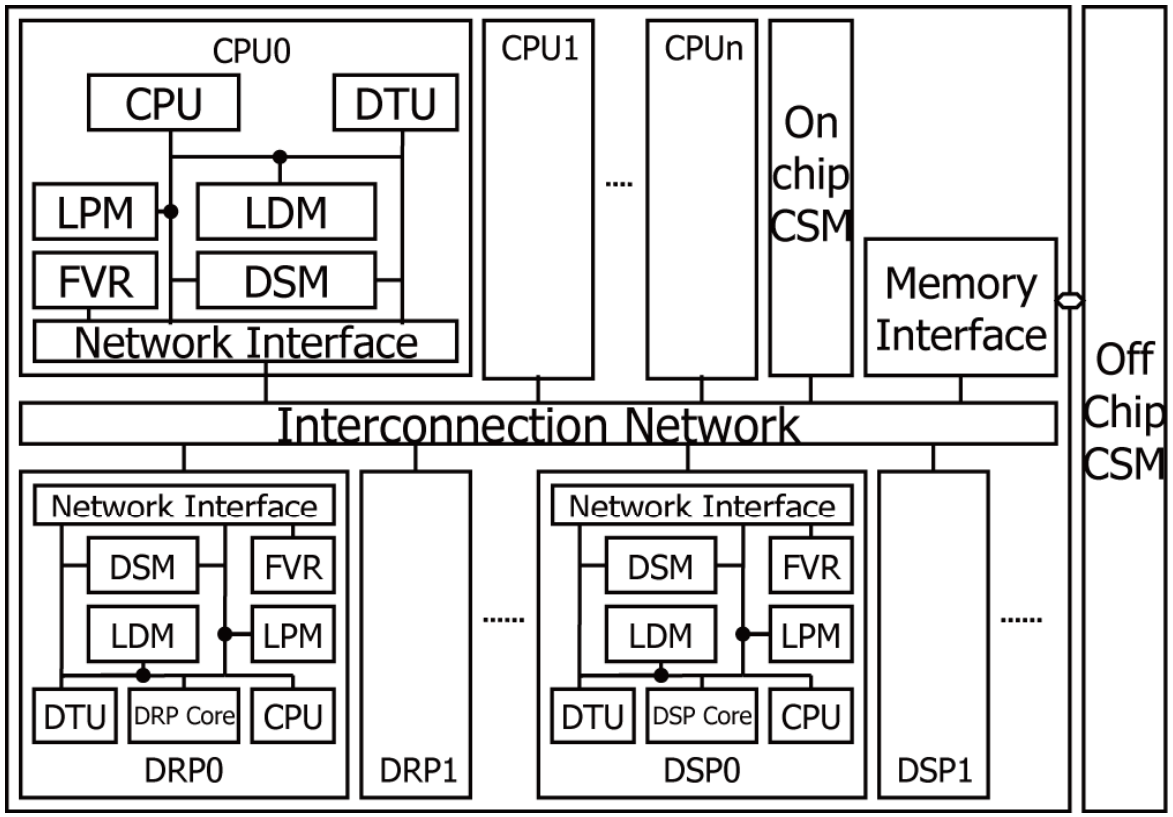
Annual Growth Rates

2005.5.11
NEDOロードマップ報告会
電子・情報技術開発部
「技術開発戦略」より

If you want to make parallel programming

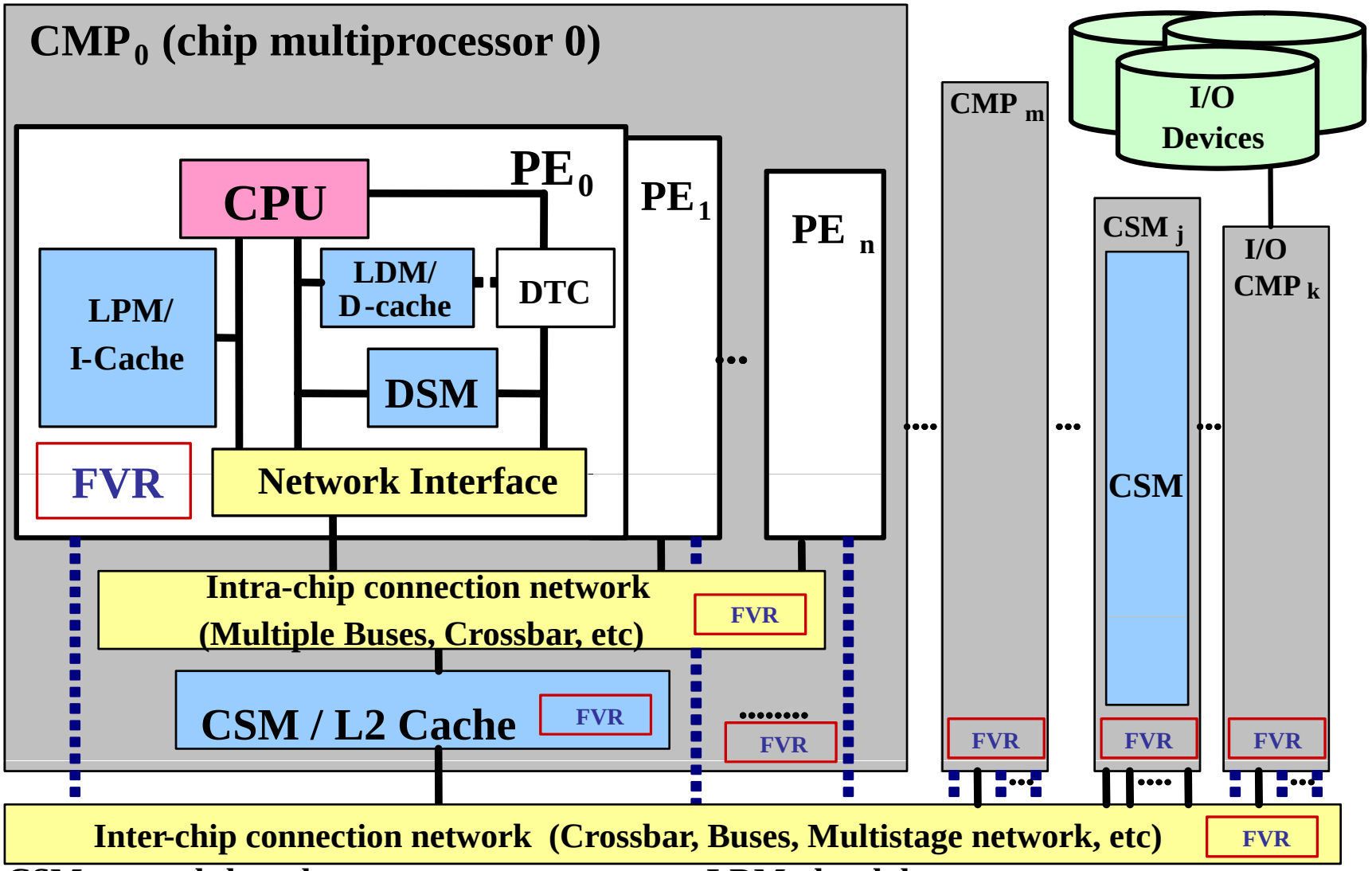
- **To improve effective performance, cost-performance and productivity and reduce consumed power**
  - **More parallelism considering core heterogeneity**
    - **Multigrain Parallelization**
      - **coarse-grain parallelism in addition to loop parallelism**
  - **Limited size of memory management considering real-time**
    - **Data localization for local memories and distributed shoared memories in addition to cache**
  - **Data Transfer Overlapping using DMA controllers**
    - **Data transfer overhead hiding by overlapping task execution and data transfer using DMA or data pre-fetching**
  - **Power reduction controlling FV and power shut-down**
    - **Reduction of consumed power by compiler control of frequency, voltage and power shut down with hardware supports.**

OSCAR Heterogeneous Multicore



- OSCAR Type Memory Architecture
- LPM
  - Local Program Memory
- LDM
  - Local Data Memory
- DSM
  - Distributed Shared Memory
- CSM
  - Centralized Shared Memory
    - On Chip and/or Off Chip
- DTU
  - Data Transfer Unit
- Interconnection Network
  - Multiple Buses
  - Split Transaction Buses
  - CrossBar …

OSCAR Multi-Core Architecture



CSM: central shared mem.

DSM: distributed shared mem.

DTC: Data Transfer Controller

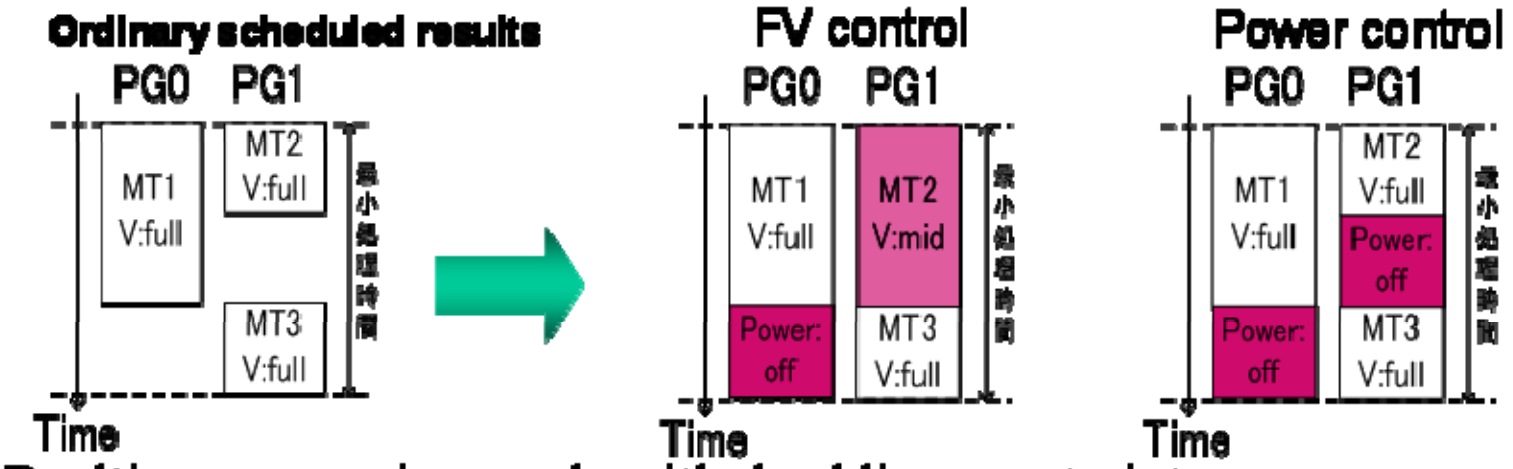
LDM : local data mem.

LPM : local program mem.

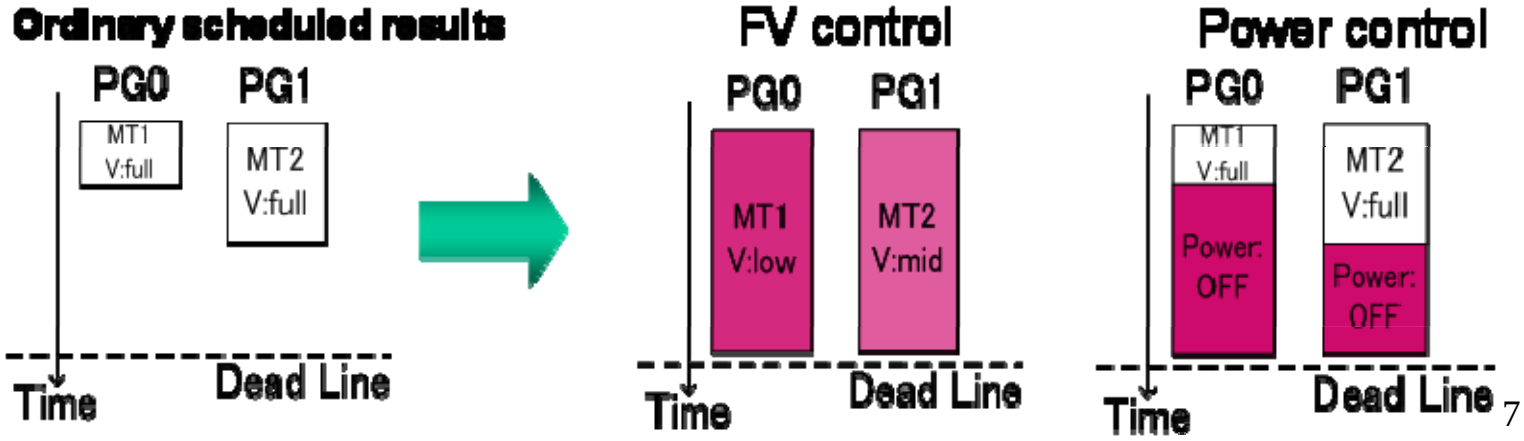
FVR: frequency / voltage control register

Power Reduction by Power Supply, Clock Frequency and Voltage Control by OSCAR Compiler

- Shortest execution time mode



- Realtime processing mode with dead line constraints



Current approach in METI/NEDO Multicore Project

OperMP(Section, Flush, Critical) + Directives for data assignment for LDM, DSM, On-chip CSM, Off-chip CSM,DMA transfers and FV & Power Shut-down control

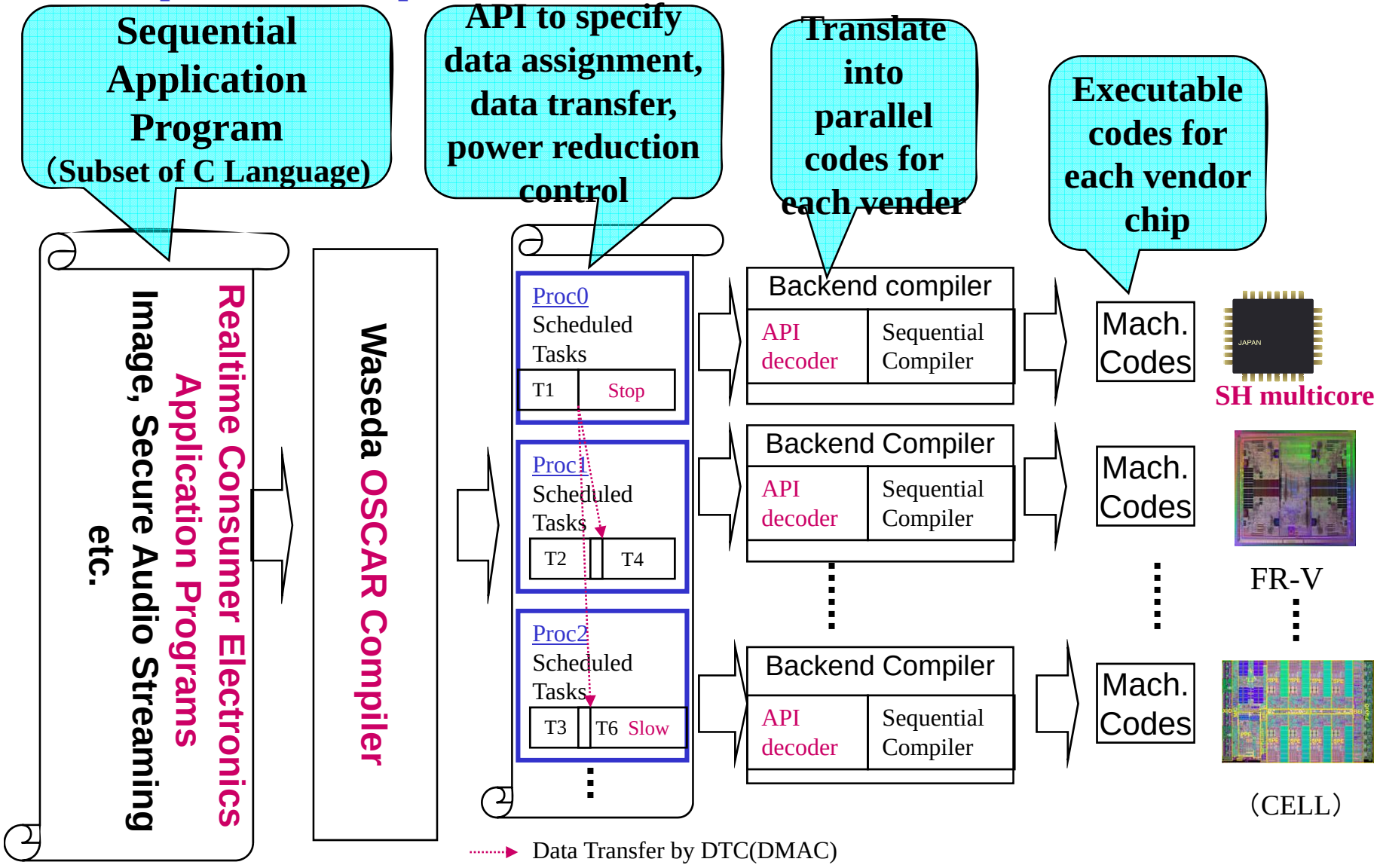
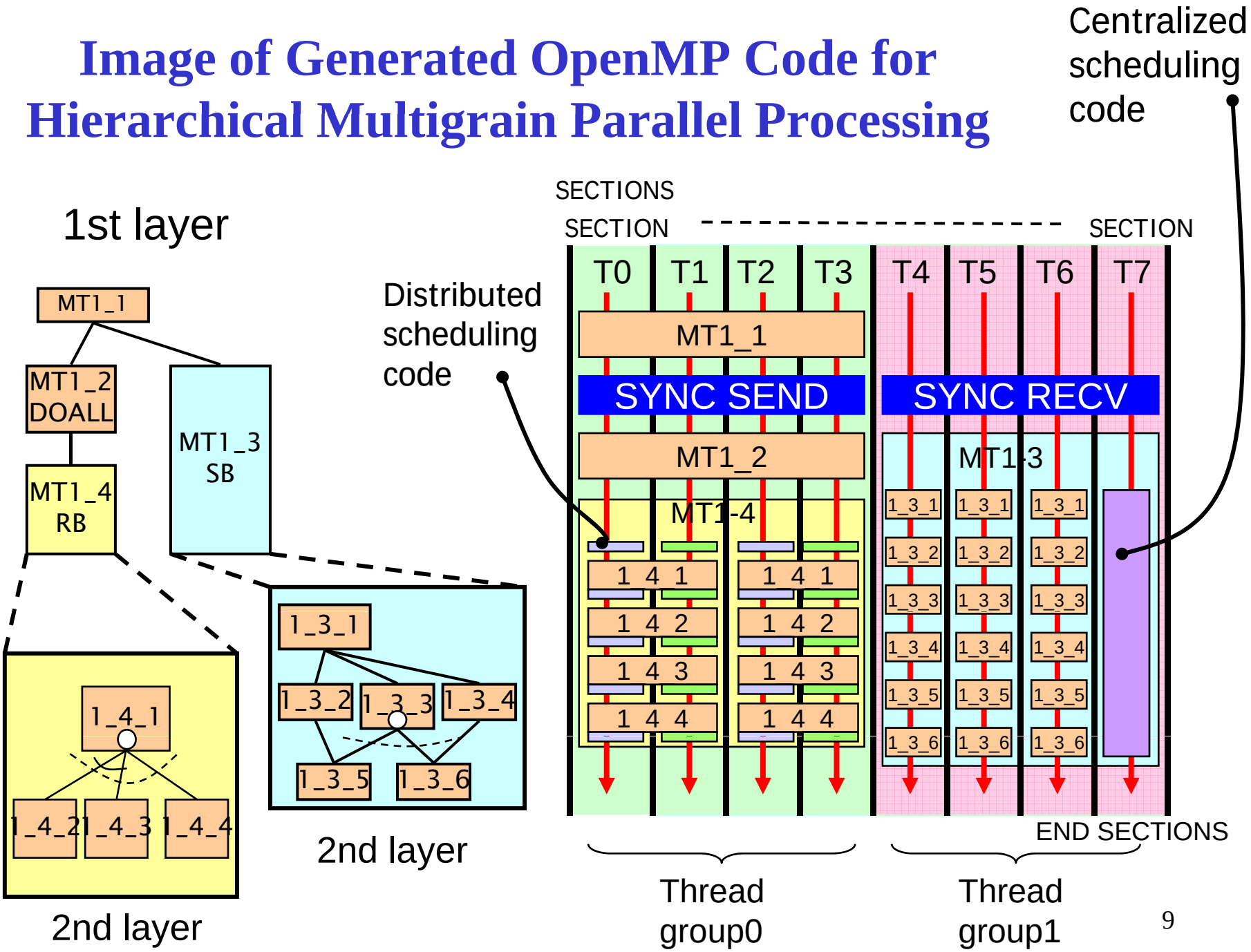
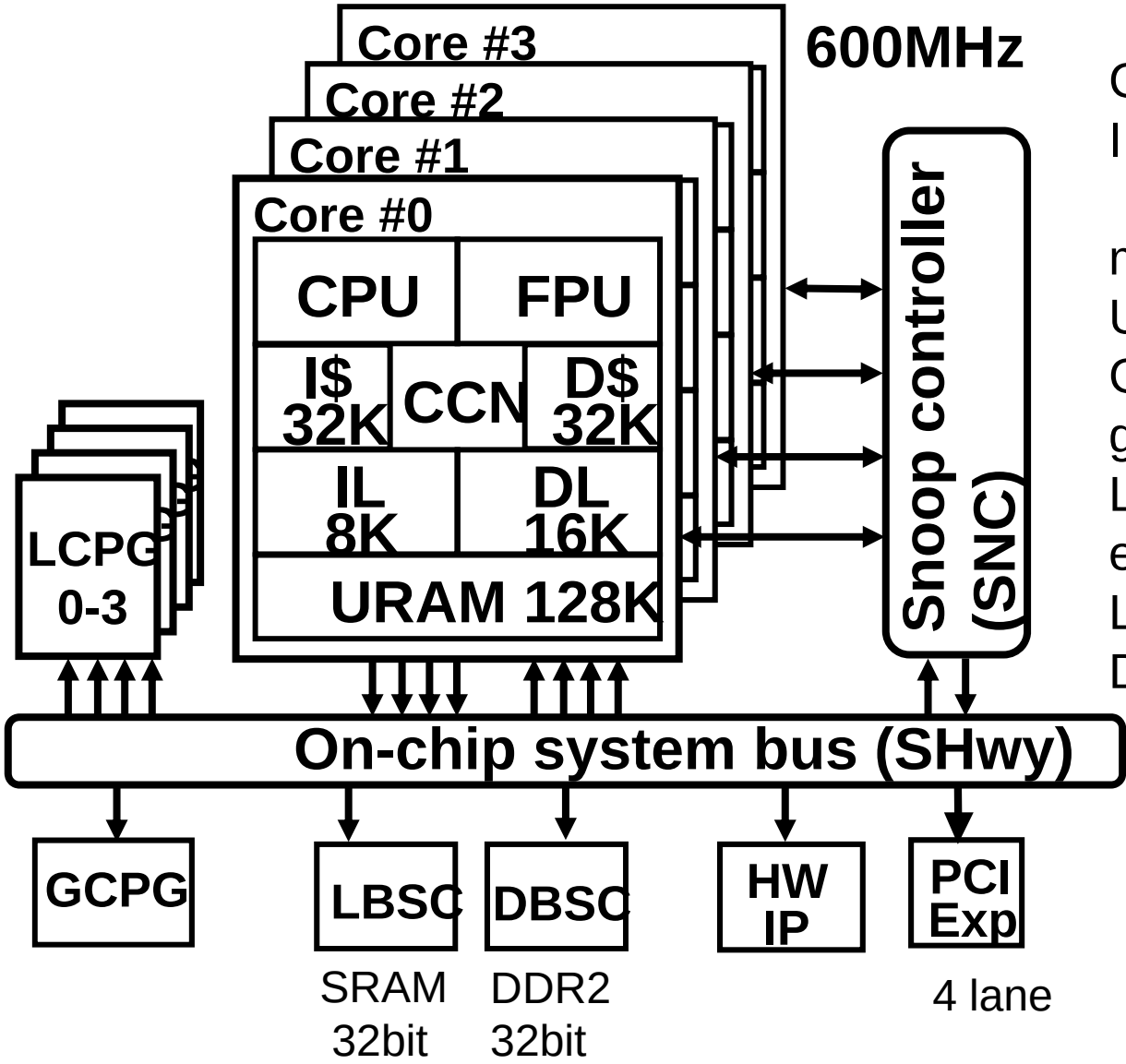


Image of Generated OpenMP Code for Hierarchical Multigrain Parallel Processing

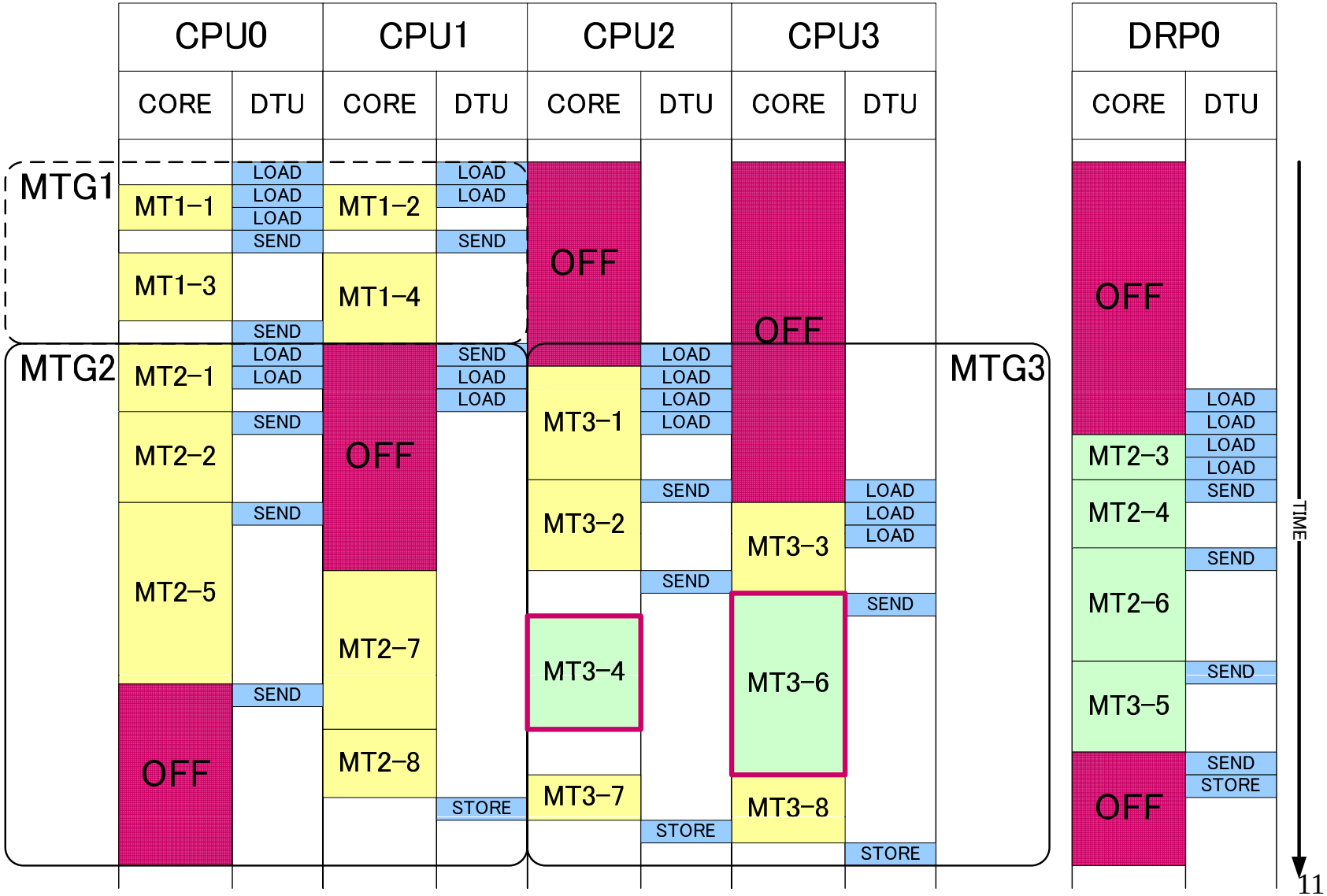


Processor Block Diagram

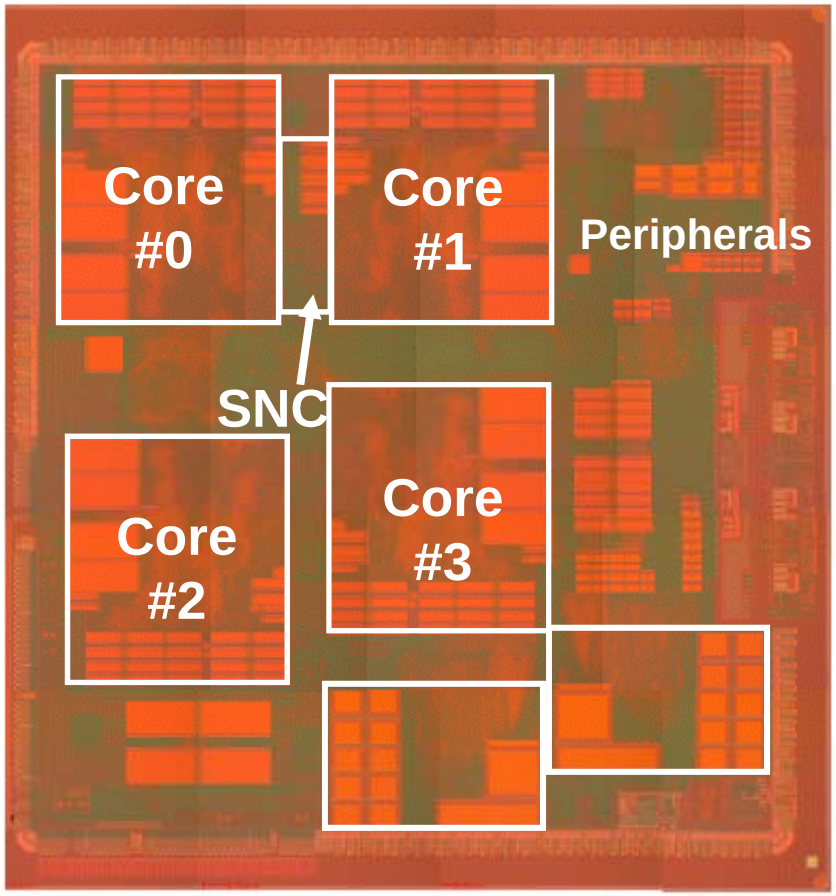


CCN:Cache controller
IL, DL: Instruction/Data local memory
URAM: User RAM
GCPG: Global clock pulse generator
LCPG: Local CPG for each core
LBSC: SRAM controller
DBSC: DDR2 controller

An Image of Static Schedule for Heterogeneous Multi-core with Data Transfer Overlapping and Power Control



Chip Overview



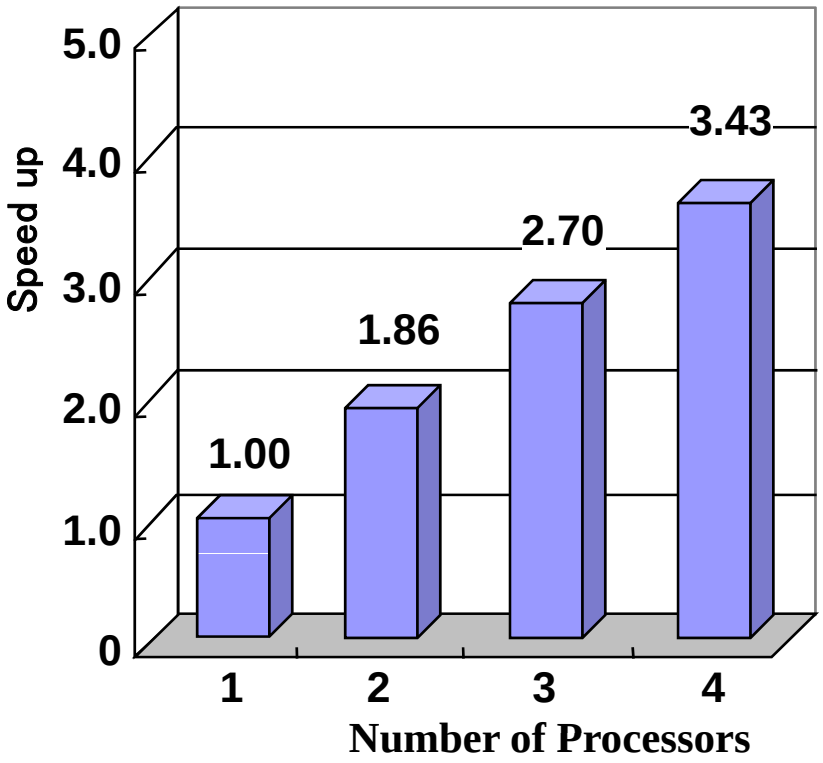
SH4A Multicore SoC Chip

Process Technology	90nm, 8-layer, triple-Vth, CMOS
Chip Size	97.6mm^2 (9.88mm x 9.88mm)
Supply Voltage	1.0V (internal), 1.8/3.3V (I/O)
Power Consumption	0.6 mW/MHz/CPU @ 600MHz (90nm G)
Clock Frequency	600MHz
CPU Performance	4320 MIPS (Dhrystone 2.1)
FPU Performance	16.8 GFLOPS
I/D Cache	32KB 4way set-associative (each)
ILRAM/OLRAM	8KB/16KB (each CPU)
URAM	128KB (each CPU)
Package	FCBGA 554pin, 29mm x 29mm

ISSCC07 Paper No.5.3, Y. Yoshida, et al., "A 4320MIPS Four-Processor Core SMP/AMP with Individually Managed Clock Frequency for Low Power Consumption"

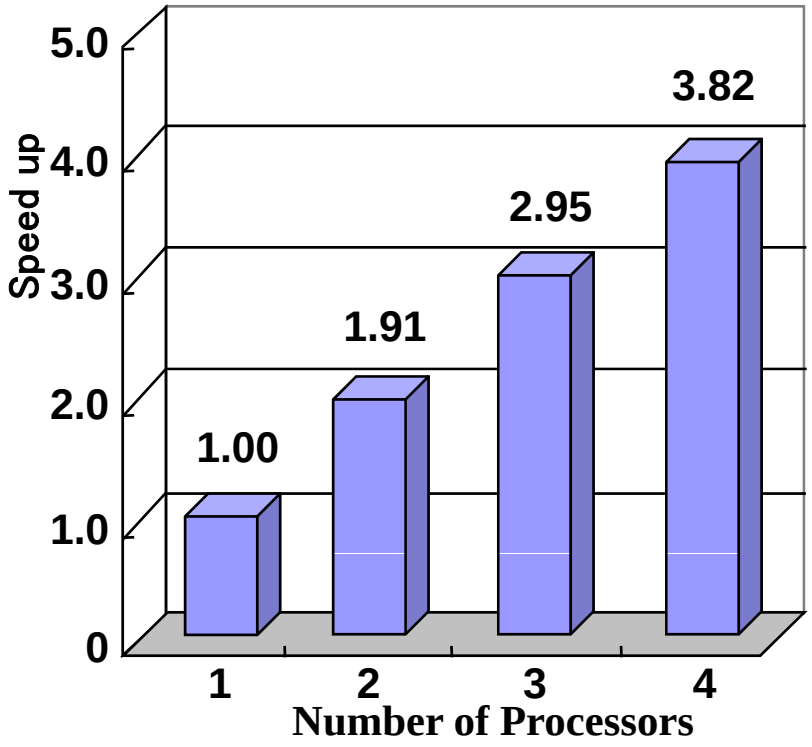
Performance on a Developed SH Multi-core (RP1: SH-X3) Using Compiler and API

Audio AAC* Encoder



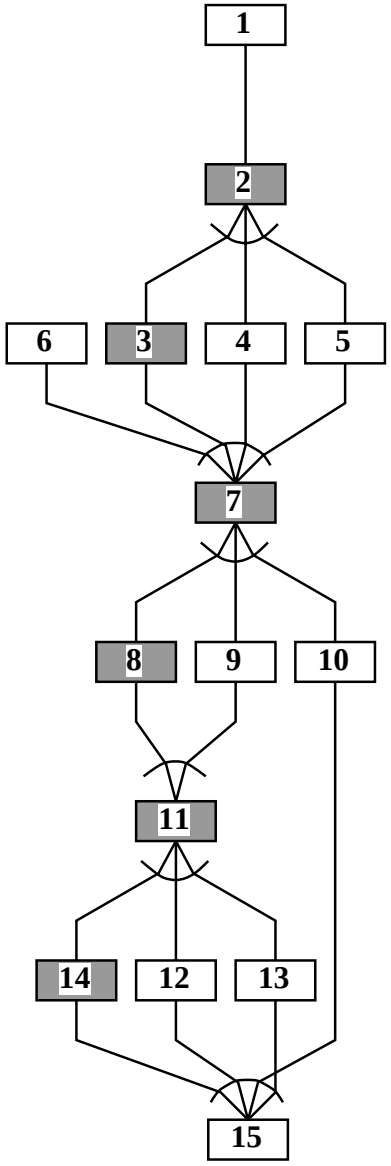
*) ISO Advanced Audio Coding :

Image Susan Smoothing

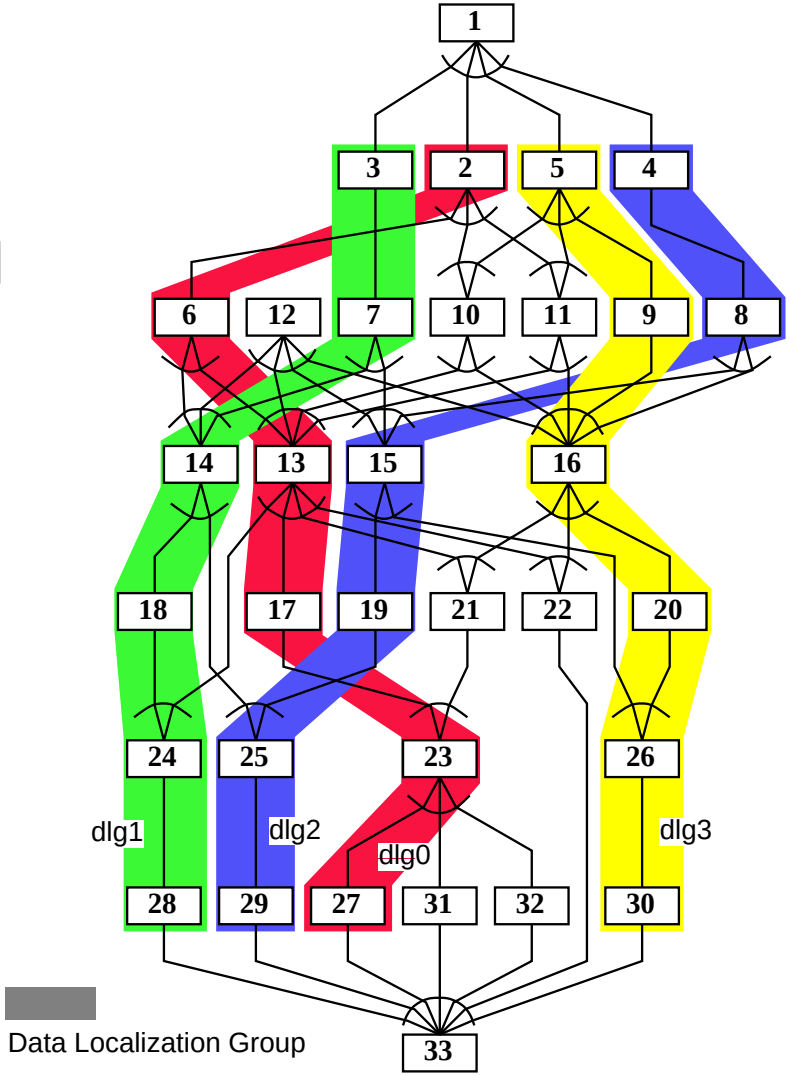


**) Mibench Embedded application benchmark by Michigan Univ.

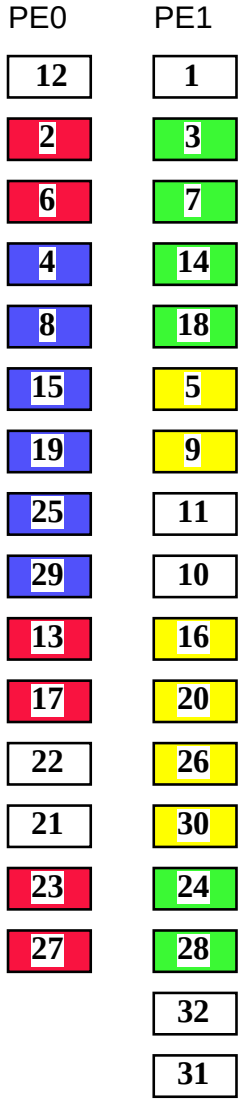
Data Localization



MTG



MTG after Division



A schedule for two processors