OSCAR Compiler and API for High Performance Low Power Multicores and Their Application to Smartphones, Automobiles, Medical Systems

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IEEE Computer Society Board of Governors
IEEE Computer Society Multicore Strategic Technical Committee (STC) Chair
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Intel/Kai, 2012.10.18(Thursday)
Multi/Many-core Everywhere

Multi-core from embedded to supercomputers

- Consumer Electronics (Embedded)
  - Mobile Phone, Game, TV, Car Navigation, Camera,
    IBM/ Sony/ Toshiba Cell, Fujitsu FR1000,
    Panasonic Uniphier, NEC/ARM MPCore/MP211/NaviEngine,
    Renesas 4 core RP1, 8 core RP2, 15core Hetero RP-X,
    Plurality HAL 64(Marvell), Tilera Tile64/ Gx100(->1000cores),
    DARPA UHPC (2017: 80GFLOPS/W)

- PCs, Servers
  - Intel Quad Xeon, Core 2 Quad, Montvale, Nehalem(8cores),
    Larrabee(32cores), SCC(48cores), Night Corner(50 core+:22nm),
    AMD Quad Core Opteron (8, 12 cores)

- WSs, Deskside & Highend Servers
  - IBM(Power4,5,6,7), Sun (SparcT1,T2), Fujitsu SPARC64fx8

- Supercomputers
    BG/Q (A2:16cores) Water Cooled20PFLOPS, 3-4MW (2011-12),
    BlueWaters(HPCS) Power7, 10 PFLOP+(2011.07),
    Tianhe-1A (4.7PFLOPS,6coreX5670+ Nvidia Tesla M2050),
    Godson-3B (1GHz40W 8core128GFLOPS) -T (64 core,192GFLOPS:2011)
    RIKEN Fujitsu “K” 10PFLOPS(8core SPARC64VIIIfx, 128GFLOPS)

High quality application software, Productivity, Cost performance, Low power consumption are important
Ex, Mobile phones, Games

Compiler cooperated multi-core processors are promising to realize the above futures
Green Computing Systems R&D Center
Waseda University
Supported by METI (Mar. 2011 Completion)

<R & D Target>
Hardware, Software, Application for Super Low-Power Manycore Processors
- More than 64 cores
- Natural air cooling (No fan)
  Cool, Compact, Clear, Quiet
- Operational by Solar Panel

<Industry, Government, Academia>
Hitachi, Fujitsu, NEC, Renesas, Olympus, Toyota, Denso, Mitsubishi, Toshiba, etc

<Ripple Effect>
- Low CO₂ (Carbon Dioxide) Emissions
- Creation Value Added Products
  - Consumer Electronics, Automobiles, Servers

Beside Subway Waseda Station, Near Waseda Univ. Main Campus
Research, development and practical utilization through industry-government-academia partnerships (spillover effect)

Environment

Industrial business

Automotive/car-mounted systems (car navigation, integrated control, infrastructure coordination)

Information appliance

Internet TV/DVD

Camera Camcorder

Mobile many-core

Smartphone Netbook

Desktop server Desk-side server

Solar cell-driven cool server

Super computer (global warming, earthquake, bio, new devices)

Cloud computing center

Waseda University: Research & Development

Low power consumption/many-core system technology

Cancer Treatment Carbon Ion Radiotherapy

Capsule Inner Camera

Industry Lives
Green Computing Systems R&D Center, 2011.11.1 (Clear)
Solar Power Generation & Server Consumption

WASEDA University

太陽光発電システム

商用電源 配電盤

外気温度 24.2℃
日射強度 0.71 kwh/m²
発電電力 28.8 kW
ノートPC換算(台) 1440
サーバー使用電力 24.7 kW

商用電源 配電盤

太陽光最大発電可能電力：40kW

A系統
3相200V 0 kW
30kW系発電電力 21.9 kW
サーバー消費電力 24.7 kW

B系統
10kW系発電電力 6.9 kW
蓄電池装置入力電力 0 kW

40kWパワー コンディショナ

Fujitsu M9000
Hitachi SR16000

直流電源出力電力 0 kW
グリーンサーバー消費電力 0 kW

10KWPowerコンディショナ
2012.4.2 (Clear) Power Generation and Server Consumption: One day Trends

電力量の1日の変化

電力量(kWh)

発電電力量
サーバー使用電力量

(時)
Super Low Power Web Server Using Embedded Multicore Processor RPX

1W with 8 SH4A processor cores

Supercomputing
Parallelizing Compiler
Clean Energy ManyCore
Advanced Computing Systems
METI/NEDO National Project
Multi-core for Real-time Consumer Electronics

**Goal** R&D of compiler cooperative multi-core processor technology for consumer electronics like Mobile phones, Games, DVD, Digital TV, Car navigation systems.

**Period** From July 2005 to March 2008

**Features**
- Good cost performance
- Short hardware and software development periods
- Low power consumption
- Scalable performance improvement with the advancement of semiconductor
- Use of the same parallelizing compiler for multi-cores from different vendors using newly developed API

API: Application Programming Interface

**Hitachi, Renesas, Fujitsu, Toshiba, Panasonic, NEC**
Renesas-Hitachi-Waseda Low Power 8 core RP2
Developed in 2007 in METI/NEDO project

IEEE ISSCC08: Paper No. 4.5, M.Ito, ... and H. Kasahara, “An 8640 MIPS SoC with Independent Power-off Control of 8 CPUs and 8 RAMs by an Automatic Parallelizing Compiler”
Demo of NEDO Multicore for Real Time Consumer Electronics at the Council of Science and Engineering Policy on April 10, 2008

CSTP Members
Prime Minister: Mr. Y. FUKUDA
Minister of State for Science, Technology and Innovation Policy: Mr. F. KISHIDA
Chief Cabinet Secretary: Mr. N. MACHIMURA
Minister of Internal Affairs and Communications: Mr. H. MASUDA
Minister of Finance: Mr. F. NUKAGA
Minister of Education, Culture, Sports, Science and Technology: Mr. K. TOKAI
Minister of Economy, Trade and Industry: Mr. A. AMARI
OSCAR Parallelizing Compiler

To improve effective performance, cost-performance and software productivity and reduce power

Multigrain Parallelization
coarse-grain parallelism among loops and subroutines, near fine grain parallelism among statements in addition to loop parallelism

Data Localization
Automatic data management for distributed shared memory, cache and local memory

Data Transfer Overlapping
Data transfer overlapping using Data Transfer Controllers (DMAs)

Power Reduction
Reduction of consumed power by compiler control DVFS and Power gating with hardware supports.
Generation of coarse grain tasks

- **Macro-tasks (MTs)**
  - Block of Pseudo Assignments (BPA): Basic Block (BB)
  - Repetition Block (RB): natural loop
  - Subroutine Block (SB): subroutine
Earliest Executable Condition Analysis for coarse grain tasks (Macro-tasks)

A Macro Flow Graph

A Macro Task Graph
MTG of Su2cor-LOOPS-DO400

- Coarse grain parallelism PARA_ALD = 4.3
Data Localization

MTG

MTG after Division

A schedule for two processors
Generated Multigrain Parallelized Code
(The nested coarse grain task parallelization is realized by only OpenMP “section”, “Flush” and “Critical” directives.)
Multicore Program Development Using OSCAR API V2.0

Sequential Application Program in Fortran or C
(Consumer Electronics, Automobiles, Medical, Scientific computation, etc.)

Manual parallelization / power reduction

Accelerator Compiler/ User
Add “hint” directives before a loop or a function to specify it is executable by the accelerator with how many clocks

Waseda OSCAR Parallelizing Compiler
- Coarse grain task parallelization
- Data Localization
- DMAC data transfer
- Power reduction using DVFS, Clock/ Power gating

Low Power Homogeneous Multicore Code Generation

API Analyzer
Existing sequential compiler

Low Power Heterogeneous Multicore Code Generation

API Analyzer (Available from Waseda)
Existing sequential compiler

Server Code Generation
OpenMP Compiler

Generation of parallel machine codes using sequential compilers

OSCAR API for Homogeneous and/or Heterogeneous Multicores and manycores
Directives for thread generation, memory, data transfer using DMA, power managements

Parallelized API F or C program

Proc0
Code with directives
Thread 0

Proc1
Code with directives
Thread 1

Accelerator 1
Code

Accelerator 2
Code

Proc0
Thread 0

Proc1
Thread 1

Accelerator 1
Code

Accelerator 2
Code

Homegeneous Multicores from Vendor A
(SMP servers)

Heterogeneous Multicores from Vendor B

Hitachi, Renesas, NEC, Fujitsu, Toshiba, Denso, Olympus, Mitsubishi, Esol, Cats, Gaio, 3 univ.

.oscar: Optimally Scheduled Advanced Multiprocessor API: Application Program Interface

Executable on various multicores

Shred memory servers
OSCAR API Ver. 2.0 for Homogeneous/Heterogeneous Multicores and Manycores

List of Directives (22 directives)

- Parallel Execution API
  - parallel sections (*)
  - flush (*)
  - critical (*)
  - execution
- Memory Mapping API
  - threadprivate (*)
  - distributedshared
  - onchipshared
- Synchronization API
  - groupbarrier
- Data Transfer API
  - dma_transfer
  - dma_contiguous_parameter
  - dma_stride_parameter
  - dma_flag_check
  - dma_flag_send

- Power Control API
  - fvcontrol
  - get_fvstatus
- Timer API
  - get_current_time

- Accelerator
  - accelerator_task_entry
- Cache Control
  - cache_writeback
  - cache_selfinvalidate
  - complete_memop
  - noncacheable
  - aligncache

2 hint directives for OSCAR compiler
- accelerator_task
- oscar_comment

(* from OpenMP)
Power Reduction by Power Supply, Clock Frequency and Voltage Control by OSCAR Compiler

- Shortest execution time mode

- Realtime processing mode with deadline constraints
An Example of Machine Parameters for the Power Saving Scheme

- **Functions of the multiprocessor**
  - Frequency of each proc. is changed to several levels
  - Voltage is changed together with frequency
  - Each proc. can be powered on/off

<table>
<thead>
<tr>
<th>state</th>
<th>FULL</th>
<th>MID</th>
<th>LOW</th>
<th>OFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>frequency</td>
<td>1</td>
<td>1/2</td>
<td>1/4</td>
<td>0</td>
</tr>
<tr>
<td>voltage</td>
<td>1</td>
<td>0.87</td>
<td>0.71</td>
<td>0</td>
</tr>
<tr>
<td>dynamic energy</td>
<td>1</td>
<td>3/4</td>
<td>1/2</td>
<td>0</td>
</tr>
<tr>
<td>static power</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

- **State transition overhead**  
  (Example: not for RP2)

<table>
<thead>
<tr>
<th>state</th>
<th>FULL</th>
<th>MID</th>
<th>LOW</th>
<th>OFF</th>
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<tbody>
<tr>
<td>FULL</td>
<td>0</td>
<td>40k</td>
<td>40k</td>
<td>80k</td>
</tr>
<tr>
<td>MID</td>
<td>40k</td>
<td>0</td>
<td>40k</td>
<td>80k</td>
</tr>
<tr>
<td>LOW</td>
<td>40k</td>
<td>40k</td>
<td>0</td>
<td>80k</td>
</tr>
<tr>
<td>OFF</td>
<td>80k</td>
<td>80k</td>
<td>80k</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>state</th>
<th>FULL</th>
<th>MID</th>
<th>LOW</th>
<th>OFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>FULL</td>
<td>0</td>
<td>20</td>
<td>20</td>
<td>40</td>
</tr>
<tr>
<td>MID</td>
<td>20</td>
<td>0</td>
<td>20</td>
<td>40</td>
</tr>
<tr>
<td>LOW</td>
<td>20</td>
<td>20</td>
<td>0</td>
<td>40</td>
</tr>
<tr>
<td>OFF</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>0</td>
</tr>
</tbody>
</table>

delay time [u.t.]  
energy overhead [μJ]
Power Reduction Scheduling

Fig. 6. V/F control of applu (4 proc.)
Low-Power Optimization with OSCAR API

Scheduled Result by OSCAR Compiler

VC0

VC1

MT1

MT2

MT3

MT4

Scheduled Result
by OSCAR Compiler

Generate Code Image by OSCAR Compiler

void main_VC0() {
    Sleep
}

void main_VC1() {
    #pragma oscar fvcontrol ¥
    ((OSCAR_CPU(),0))
    MT2

    #pragma oscar fvcontrol ¥
    (1,(OSCAR_CPU(),100))
    MT1

    MT2
    Sleep

    MT1
     }

    MT3
    MT4

    MT3
    MT4

    }
Performance of OSCAR Compiler on IBM p6 595 Power6 (4.2GHz) based 32-core SMP Server

OpenMP codes generated by OSCAR compiler accelerate IBM XL Fortran for AIX Ver.12.1 about **3.3 times** on the average

Compile Option:

| (*1) Sequential: | -O3 -qarch=pwr6, XLF: -O3 -qarch=pwr6 -qsmp=auto, OSCAR: -O3 -qarch=pwr6 -qsmp=noauto |
| (*)2 Sequential: | -O5 -q64 -qarch=pwr6, XLF: -O5 -q64 -qarch=pwr6 -qsmp=auto, OSCAR: -O5 -q64 -qarch=pwr6 -qsmp=noauto |
| Others Sequential: | -O5 -qarch=pwr6, XLF: -O5 -qarch=pwr6 -qsmp=auto, OSCAR: -O5 -qarch=pwr6 -qsmp=noauto |
OSCAR Compiler’s Performance on Fujitsu9000 SparcVII 256core SMP

![Bar Chart](chart.png)

- OSAR Compiler
- Fujitsu Compiler
- Sun Studio Compiler
- OSAR + Sun Studio Compiler

**Speedup Ratio**

**spec2000 swim**

**# of PEs**
Engine Control by multicore with Denso

Though so far parallel processing of the engine control on multicore has been very difficult, Denso and Waseda succeeded 1.95 times speedup on 2core V850 multicore processor.
Performance of OSCAR Compiler & API on 2 ARMv7-cores Qualcomm MSM8960 (Snapdragon) Android 4.0 for Smart Phones

1.81 times speedup by 2 cores on the average against 1 core
Parallel Processing Performance on 3Cores NaviEngine with Realtime OS eT-Kernel Multi-Core Edition

NaviEngine (ARM11 MPCore) 400MHz 3 core SMP
(Renesas Electronics EC-4260)

• 2.37 times speedup on 3ARM cores against 1 core
Power Reduction of MPEG2 Decoding to 1/4 on 8 Core Homogeneous Multicore RP-2 by OSCAR Parallelizing Compiler

Avg. Power

Without Power Control
(Voltage: 1.4V)

With Power Control
(Frequency, Resume Standby: Power shutdown & Voltage lowering 1.4V-1.0V)

Avg. Power
5.73 [W]  
73.5% Power Reduction  
1.52 [W]
An Image of Static Schedule for Heterogeneous Multi-core with Data Transfer Overlapping and Power Control

<table>
<thead>
<tr>
<th></th>
<th>CPU0</th>
<th></th>
<th>CPU1</th>
<th></th>
<th>CPU2</th>
<th></th>
<th>CPU3</th>
<th></th>
<th>DRP0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CORE</td>
<td>LOAD</td>
<td>LOAD</td>
<td>LOAD</td>
<td>LOAD</td>
<td>LOAD</td>
<td>LOAD</td>
<td>LOAD</td>
<td>LOAD</td>
<td>LOAD</td>
</tr>
<tr>
<td>DTU</td>
<td>SEND</td>
<td>SEND</td>
<td>SEND</td>
<td>SEND</td>
<td>SEND</td>
<td>SEND</td>
<td>SEND</td>
<td>SEND</td>
<td>SEND</td>
</tr>
<tr>
<td>CORE</td>
<td>OFF</td>
<td>MT3-1</td>
<td>MT3-2</td>
<td>MT3-3</td>
<td>MT3-4</td>
<td>MT3-5</td>
<td>MT3-6</td>
<td>MT3-7</td>
<td>MT3-8</td>
</tr>
<tr>
<td>DTU</td>
<td>STORE</td>
<td>STORE</td>
<td>STORE</td>
<td>STORE</td>
<td>STORE</td>
<td>STORE</td>
<td>STORE</td>
<td>STORE</td>
<td>STORE</td>
</tr>
</tbody>
</table>

MTG1, MTG2, MTG3 represent different time segments with tasks assigned to CPU cores. Each core performs either load, send, or store operations.
33 Times Speedup Using OSCAR Compiler and OSCAR API on RP-X (Optical Flow with a hand-tuned library)

CPU performs data transfers between SH and FE

Y. Yuyama, et al., “A 45nm 37.3GOPS/W Heterogeneous Multi-Core SoC”, ISSCC2010

3.4 [fps]

111 [fps]
Power Reduction in a real-time execution controlled by OSCAR Compiler and OSCAR API on RP-X (Optical Flow with a hand-tuned library)

Without Power Reduction

With Power Reduction by OSCAR Compiler

70% of power reduction

Average: 1.76[W] → Average: 0.54[W]

1 cycle: 33[ms] → 30[fps]
8 Core RP2 Chip Block Diagram

On-chip system bus (SuperHyway)

LCPG: Local clock pulse generator
PCR: Power Control Register
CCN/BAR: Cache controller/Barrier Register
URAM: User RAM (Distributed Shared Memory)
Faster or Equal Processing Performance with Hardware Coherence Control on 8 core RP2 Multicore Processor Having Hardware Coherent Mechanism Up-to 4 cores by OSCAR Compiler’s Software Coherence Control

<table>
<thead>
<tr>
<th>No. of processor cores</th>
<th>AAC Encoder</th>
<th>MPEG2 Decoder</th>
<th>MPEG2 Encoder</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>2</td>
<td>1.02</td>
<td>1.01</td>
<td>1.02</td>
</tr>
<tr>
<td>4</td>
<td>1.92</td>
<td>1.62</td>
<td>2.10</td>
</tr>
<tr>
<td>8</td>
<td>1.89</td>
<td>1.61</td>
<td>1.85</td>
</tr>
</tbody>
</table>

Graph showing Seed Up against sequential Processing with SMP and Non-Coherent Cache for various applications.
92 Times Speedup against the Sequential Processing for GMS Earthquake Wave Propagation Simulation on Hitachi SR16000 (Power7 Based 128 Core Linux SMP)
Cancer Treatment
Carbon Ion Radiotherapy
(Previous best was 2.5 times speedup on 16 processors with hand optimization)

8.9 times speedup by 12 processors
Intel Xeon X5670 2.93GHz 12 core SMP (Hitachi HA8000)

55 times speedup by 64 processors
IBM Power 7 64 core SMP (Hitachi SR16000)
# CS Multicore STC Team

## Chair
- Hironori Kasahara

## FTs Proj. Mgr.
- ? (to be hired)

## BoG “Angel”
- Hironori Kasahara

### Conferences
- **Hard+Soft+Industrial Applications from Embedded to HPC Systems with Gov., Acad. & Indus.**
  - Co-Chair Josep Torrellas (UIUC)
  - Co-Chair Hironori Kasahara
  - Vivek Sarkar (Rice U.)
  - Dr. Ahmed Jerraya, CEA-LETI, MINATEC, Fr
  - + Industry: Automobile, Smart Phone, Medical etc
  - Carrie Walsh (SE)

### Standards
- **Architecture Committee**
  - 3D Integ., Memory (Non volatile), etc
- **Software Committee**
  - API, Development Env. etc
- **Industrial Application Comm.**
  - Consumer Electronics (Smart Phones): ATT, NTT, Apple,
  - Automobile (GM, Mercedes, Toyota, Bosch, Denso, etc)
  - Medical (Varian, Hitachi, Siemens, etc)
  - Anne Marie Kelly (SE)

### Publishing
- **Online Publication for quick and low cost**
  - Trans. on Multicores
  - Multicore Magazine
- **Start as online publication through Web Portal**: Not only written papers and also Online Presentation by especially Industry Leaders
- **Think introduction of “Mileage system” for Editorial, Programing Committee members and reviewers**
  - Lars Jentsch (SE), Alicia Stickley (SE)

### Education
- **Start from “Online Lecture”:**
  - Ask the lecture to the world best researcher for the topics
  - David Padua (UIUC)
  - Dorian McClenahan (SE)

### Body of Knowledge
- **Thesaurus**
  - Based on Parallel Processing Encyclopedia
  - David Padua & others
  - Dante David (SE)

### Web Portal
- **Start from Online lecture with Education and Online Magazine with Publishing**
- Thematic:
  - Theresa McNeill (SE)
  - Chris Jensen (SE)

### Newsletter
- **First, with Conference, Education and Publishing push the latest attractive information to members.**
  - Theresa McNeill (SE)
  - Margo McCall (SE)

---

*GL − Group Lead  SE − Staff Expert*
Conclusions

- OSCAR compiler automatic parallelizes C or Fortran program using multigrain parallelization, data localization for cache and local memory with DMA data transfers and generates C or Fortran parallelized code with OSCAR API version 2.0.
- It supports shared memory homogeneous and heterogeneous multicores and manycores including non-coherent cache architectures.
- In addition to the automatic parallelization, automatic power control using DVFS and Clock and Power gating has been implemented for real-time processing and minimum execution time processing modes.
- The following performance has been attained on various multicores and servers:
  - 55 times speedup by 64 processor cores for Carbon Ion Radiotherapy Cancer treatment on IBM Power 7 64 core SMP (Hitachi SR16000)
  - 92 Times Speedup for GMS Earthquake Wave Propagation Simulation on 128 processor cores SMP (Hitachi SR16000)
  - Faster or Equal Processing Performance with Hardware Coherence Control on 8 core RP2 Multicore Precessor Having Hardware Coherent Mechanism Up-to 4 cores by OSCAR Compiler’s Software Coherence Control
  - 33 Times Speedup for Optical Flow on 8 SH4A and 4 DRP accelerators on RP-X heterogeneous multicore.
  - Power Reduction of MPEG2 Decoding to 1/4 on 8 Core Homogeneous Multicore RP-2.
  - 1.95 times speedup on Renesas V850 2 core embedded multicore for automobile engine control program generated by MATLAB/SIMLINK embedded coder.
  - 2.9 Times Speed-up for AAC Encodeing on 3 Core NaviEngine (ARM MPcore) with Realtime OS eT-Kernel Multi-Core Edition