COMPSAC 2106 Plenary Panel
Rebooting Computing:
Future of Architecture and Software

Multicore Software and Architecture

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Performance and Low Power are Key Issues

Power consumption is one of the biggest problems for performance scaling from smartphones to cloud servers and supercomputers ("K" more than 10MW).

\[
\text{Power } \propto \text{ Frequency } \times \text{ Voltage}^2 \\
\text{(Voltage } \propto \text{ Frequency)}
\]

If **Frequency** is reduced to **1/4** (Ex. 4GHz → 1GHz),

**Power** is reduced to **1/64** and

**Performance** falls down to **1/4**.

**<Multicores>**

If **8cores** are integrated on a chip,

**Power** is still **1/8** and

**Performance** becomes **2 times**.
With 128 cores, OSCAR compiler gave us 100 times speedup against 1 core execution and 211 times speedup against 1 core using Sun (Oracle) Studio compiler.
To improve effective performance, cost-performance and software productivity and reduce power.

Multigrain Parallelization
coarse-grain parallelism among loops and subroutines, near fine grain parallelism among statements in addition to loop parallelism.

Data Localization
Automatic data management for distributed shared memory, cache and local memory.

Data Transfer Overlapping
Data transfer overlapping using Data Transfer Controllers (DMAs).

Power Reduction
Reduction of consumed power by compiler control DVFS and Power gating with hardware supports.
Power can be reduced by software control:
MPEG2 Decoding to 1/4 on 8 Core Multicore
by OSCAR Parallelizing Compiler

Without Power Control
(Voltage : 1.4V)

With Power Control
(Frequency,
Resume Standby:
Power shutdown &
Voltage lowering 1.4V-1.0V)

Avg. Power
5.73 [W]

73.5% Power Reduction

Avg. Power
1.52 [W]
Real-time Optical Flow

Power of Multicores with DVFS can be Reduced by Software: Intel Haswell

Intel CPU Core i7 4770K

For HD 720p (1280x720) moving pictures 15fps (Deadline 66.6 [ms/frame])

Power was reduced to 1/4 by compiler on 3 cores

1 core Power (29.3W) was reduced to 1/3 (9.6W) with 3 cores by OSCAR compiler.
Target:

- Solar Powered with compiler power reduction.
- Fully automatic parallelization and vectorization including local memory management and data transfer.
1992 Fujitsu VPP500/NWT: PE Unit