

OSCAR Parallelizing Compiler Cooperative Heterogeneous Multi-core Architecture

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1. Background

Heterogeneous multi-core architectures, which integrates multiple general purpose CPU cores and special purpose accelerator cores on a chip, have become widely spread. However, heterogeneous multi-cores require very difficult coding for load distribution to CPU cores and accelerator cores, synchronizations and data transfer using DMA controllers. To release application programmers from such painful work, powerful parallelizing compiler for heterogeneous multi-core architectures is expected. Furthermore, cooperative work between parallelizing compiler and heterogeneous multi-core architectures is important to fully exploit the potential from these systems. Considering above situations, this poster proposes OSCAR parallelizing compiler cooperative heterogeneous multi-core architecture.

2. The Proposed Architecture

The architecture comprises the following compiler-aware features(Figure.1): (1)Local data memory and distributed shared memory. (2)Advanced DMA controller called DTU (Data Transfer Unit) which enables overlapping task execution and data transfer. (3)Directly connecting an accelerator and a CPU on the same core.

3. Performance Results

For the evaluations, a cycle accurate heterogeneous multi-core architecture simulator is developed. As a CPU, a single issue in-order SPARC V9 pipeline is assumed. Also, as an accelerator, Hitachi FE-GA[1], which is dynamically reconfigurable processor, is assumed.

The performance of the architecture is evaluated using MP3 encoder program and AAC encoder program, which are parallelized by OSCAR compiler[2]. As a result, the proposed architecture gives us 21.4 times speedup with four general purpose PCs and four accelerator PCs for an MP3 audio encoder program versus sequential execution using a single CPU core. Moreover, the architecture gives us 10.0 times speedup when executing an AAC encoder program using the previous architecture.

4. Conclusions

In this poster, We present OSCAR compiler cooperative heterogeneous multi-core architecture. The proposed architecture, which is designed to supports OSCAR compiler, gives us good performance.

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References

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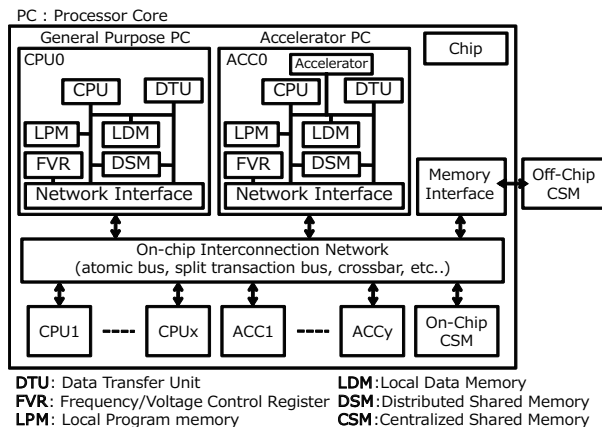


Figure 1. The proposed architecture