Prof. Hironori Kasahara

Head: Department of Computer Science

Director: Advanced Chip Multiprocessor Research Institute

Waseda University

3-4-1 Ohkubo Shinjuku-ku, Tokyo, 169-8555, Japan

E-mail: kasahara@waseda.jp

URL:http://www.kasahara.cs.waseda.ac.jp

Members:

Associate Professor: Dr. Keiji Kimura

Research Associates: Mr. Jun Shirako, Mr. Yasutaka Wada

Ph. D Students: 7, M2: 8, M1: 11, B4: 20 (inc.M0: 14)

Hironori Kasahara

＜Personal History＞

B.S. (1980,Waseda), M.S.(1982,Waseda), Ph.D.(1985,EE, Waseda). Res.Assoc. (1983,Waseda), Special Research Fellow JSPS (1985) ,Visiting Scholar (1985.Univ.California at Berkeley), . Assist. Prof. (1986.Waseda), Assoc. Prof.(1988,Waseda), Visiting Research Scholar(1989-1990. Center for Supercomputing R&D, Univ.of Illinois at Urbana-Champaign), Prof.(1997-,Dept. CS, Waseda). , IFAC World Congress Young Author Prize (1987), IPSJ Sakai Memorial Special Award (1997), STARC Industry-Academia Cooperative Research Award (2004)

＜Activities for Societies＞

IPSJ：Sig. Computer Architecture(Chair), Trans of IPSJ Editorial Board (HG Chair), Journal of IPSJ Editorial Board (HWG Chair), 2001 Journal of IPSJ Special Issue on Parallel Processing(Chair of Editorial Board: Guest Editor, JSPP2000 (Program Chair) etc.

ACM ：International Conference on Supercomputing(ICS)(Program Committee)
Int'l conf. on Supercomputing (PC, esp. '96 ENIAC 50th Anniversary Co-Prog. Chair).

IEEE: Computer Society Japan Chapter Chair, Tokyo Section Board Member, SC07 PC

OTHER: PCs of many conferences on Supercomputing and Parallel Processing.

<Activities for Governments>

METI：IT Policy Proposal Forum(Architecture/HPC WG Chair),
Super Advanced Electronic Basis Technology Investigation Committee

NEDO:Millennium Project IT21 "Advanced Parallelizing Compiler"(Project Leader),
Computer Strategy WG (Chair).Multicore for Realtime Consumer Electronics Project Leader etc.

MEXT:Earth Simulator project evaluation committee,

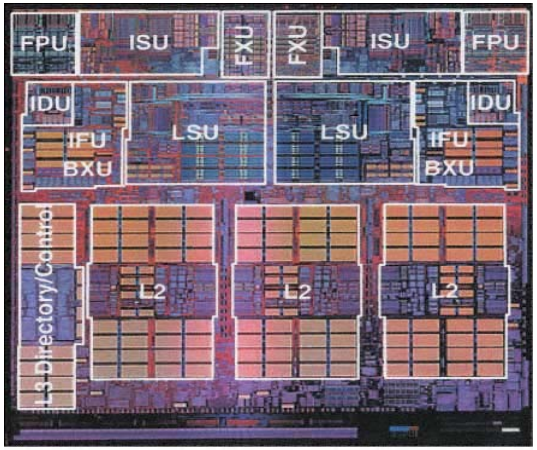
JAERI: Research accomplishment evaluation committee, CCSE 1st class invited researcher.

JST: Scientific Research Fund Sub Committee, COINS Steering Committee ,
Precursory Research for Embryonic Science and Technology (Research Area Adviser)

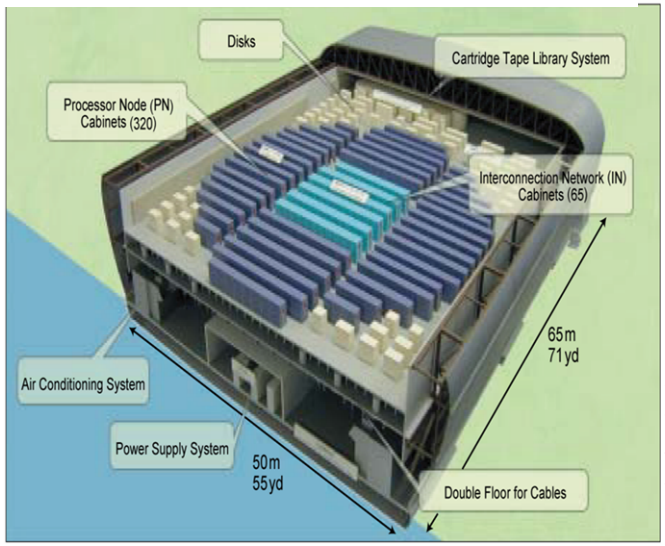
Cabinet Office: CSTP Expert Panel on Basic Policy, Information & Communication Field Promotion Strategy , R&D Infrastructure WG, Software & Security WG

＜Papers＞151 Papers with Review, 20 Papers for Symposium with Review, 105 Technicar Reports, 154 Papers for Annual Convention, 49 Invited Talks, 74 Articles in Newspaper & Web, etc.

Multi-core Everywhere



IBM First Chip Multiprocessor (CMP) Power 4 processor
2 cores on a chip



Earth simulaor：5120 vector processors Multiprocessor Supercomputer

Multi-core from embedded to supercomputers

- **Consumer Electronics (Embedded)**
  - Mobile Phone, Game, Digital TV, Car Navi, DVD, Camera
  - IBM/ Sony/ Toshiba Cell, Fuijtsu FR1000, NEC/ARMMPCore&MP211, Panasonic Uniphier, Renesas SH multi-core(RP1)
- **PCs, Servers**
  - Intel Dual-Core Xeon, Core 2 Duo, Montecito
  - AMD Quad and Dual-Core Opteron
- **WSs, Deskside & Highend Servers**
  - IBM Power4,5,5+, pSeries690(32way), p5 550Q(8 way) , Sun N iagara(SparcT1,T2), SGI ALTIX350,
- **Supercomputers**
  - Earth Simulator:40TFLOPS, 2002, 5120 vector proc.
  - IBM Blue Gene/L: 360TFLOPS, 2005,
    Low power CMP based 128K processor chips

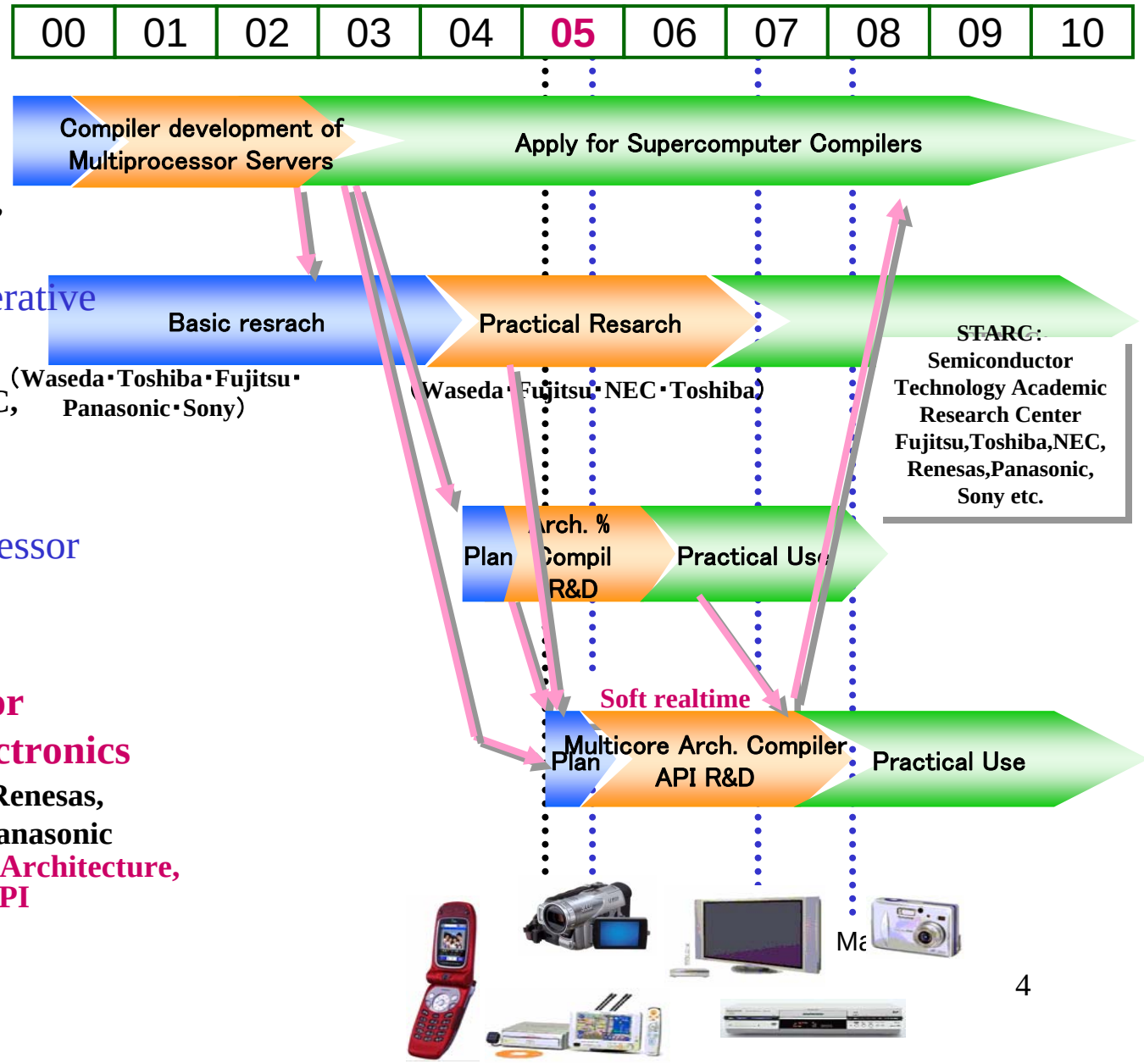
High quality application software, Productivity, Cost performance, Low power consumption are important

Ex, Mobile phones, Games

Compiler cooperated multi-core processors are promising to realize the above futures

Roadmap of compiler cooperative multicore project

- Millennium Project IT21
  NEDO Advanced
  Parallelizing Compiler
  （Waseda Univ. Fujitsu,Hitachi, JIPDEC,AIST）
- STARC Compiler Cooperative
  Chip Multiprocessor
  （ Waseda Univ., Fujitsu, NEC, Toshiba, Panasonic,Sony）
- NEDO
  Heterogeneous Multiprocessor
  （Waseda Univ., Hitachi）
- **NEDO**
  Multicore Technology for
  Realtime Consumer Electronics
  - Waseda Univ., Hitachi, Renesas, Fujitsu, NEC, Toshiba, Panasonic
  - ➢Power Saving Multicore Architecture, Parallelizing Compiler,API



National Project by METI/NEDO

Multi-core for Real-time Consumer Electronics

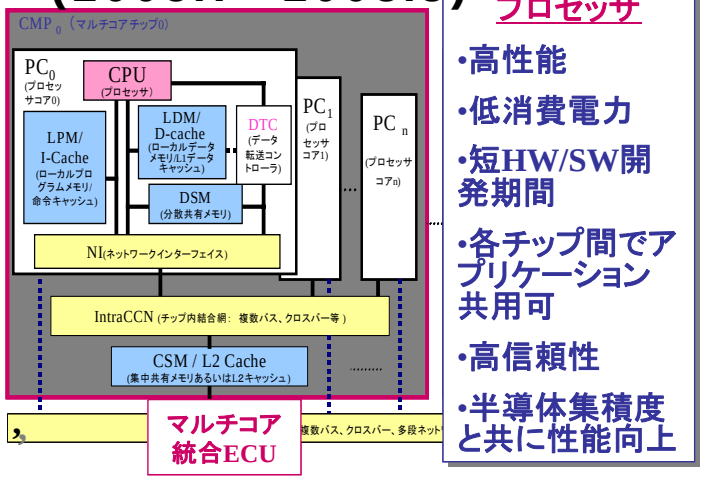
<Goal> R&D of compiler cooperative multi-core processor technology for consumer electronics like Mobile phones, Games, DVD, Digital TV, Car navigation systems.

<Period> From July 2005 to March 2008

<Features>
- Good cost performance
- Short hardware and software development periods
- Low power consumption
- Scalable performance improvement with the advancement of semiconductor
- Use of the same parallelizing compiler for multi-cores from different vendors using newly developed API

API : Application Programming Interface

経済産業省 / NEDOリアルタイム情報家電用マルチコア (2005.7～2008.3) **

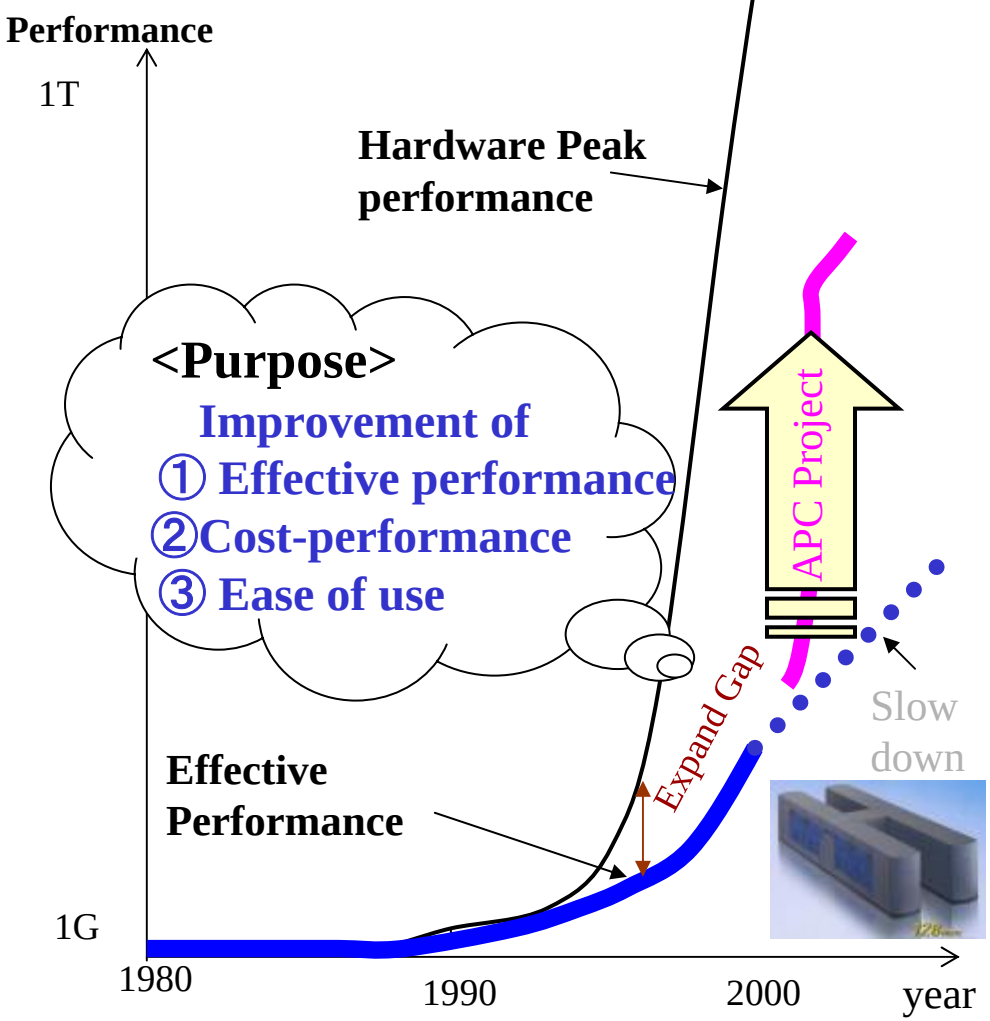


開発マルチコアチップは情報家電へ

**日立,富士通,ルネサス,東芝,松下,NEC

METI/NEDO Advanced Parallelizing Compiler Technology Project

Millenium Project IT21 2000.9.8 –2003.3.31
Waseda Univ., Fujitsu, Hitachi, AIST



Theoretical maximum performance vs. Effective performance of HPC

Background and Problems

①Adoption of parallel processing as a core technology on PC to HPC
② Increase of importance of software on IT
③ Need for improvement of cost-performance and usability

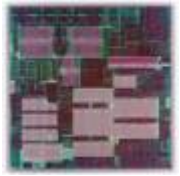
Contents of Research and Development

① R & D of advanced parallelizing compiler
Multigrain, Data localization, Overhead hiding
② R & D of Performance evaluation technology for parallelizing compilers

Goal: Double the effective performance

Ripple Effect

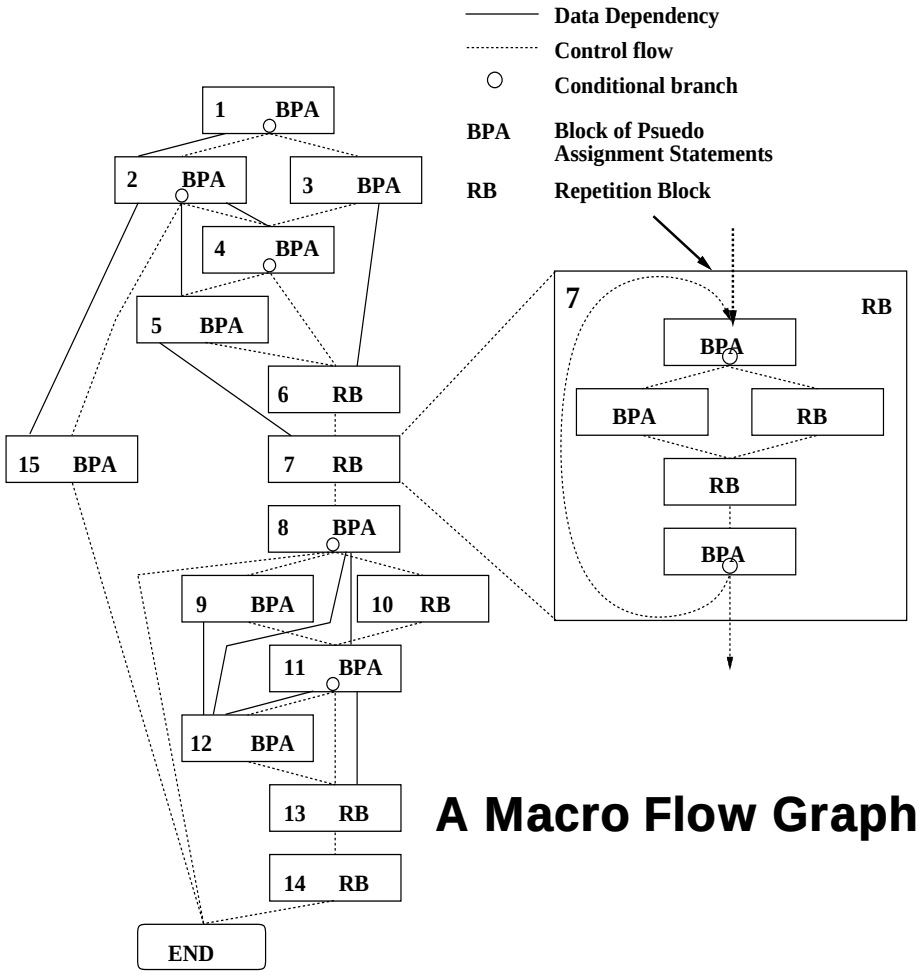
① Development of competitive next generation PC and HPC
② Putting the innovative automatic parallelizing compiler technology to practical use
③ Development and market acquisition of future single-chip multiprocessors
④ Boosting R&D in the following many fields:
IT, Bio-tech., Device, Earth environment, Next-generation VLSI design, Financial engineering, Weather forecast, New clean energy, Space development, Automobile, Electric Commerce, etc



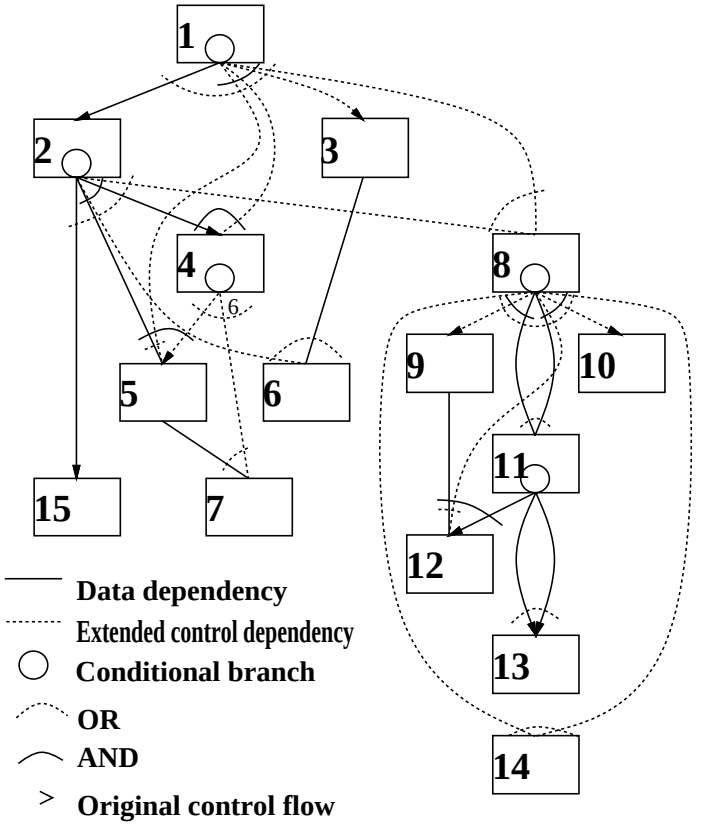
OSCAR Parallelizing Compiler

- **Improve effective performance, cost-performance and productivity and reduce consumed power**
  - **Multigrain Parallelization**
    - **Exploitation of parallelism from the whole program by use of coarse-grain parallelism among loops and subroutines, near fine grain parallelism among statements in addition to loop parallelism**
  - **Data Localization**
    - **Automatic data distribution for distributed shared memory, cache and local memory on multiprocessor systems.**
  - **Data Transfer Overlapping**
    - **Data transfer overhead hiding by overlapping task execution and data transfer using DMA or data pre-fetching**
  - **Power Reduction**
    - **Reduction of consumed power by compiler control of frequency, voltage and power shut down with hardware supports.**

Earliest Executable Condition Analysis for coarse grain tasks (Macro-tasks)



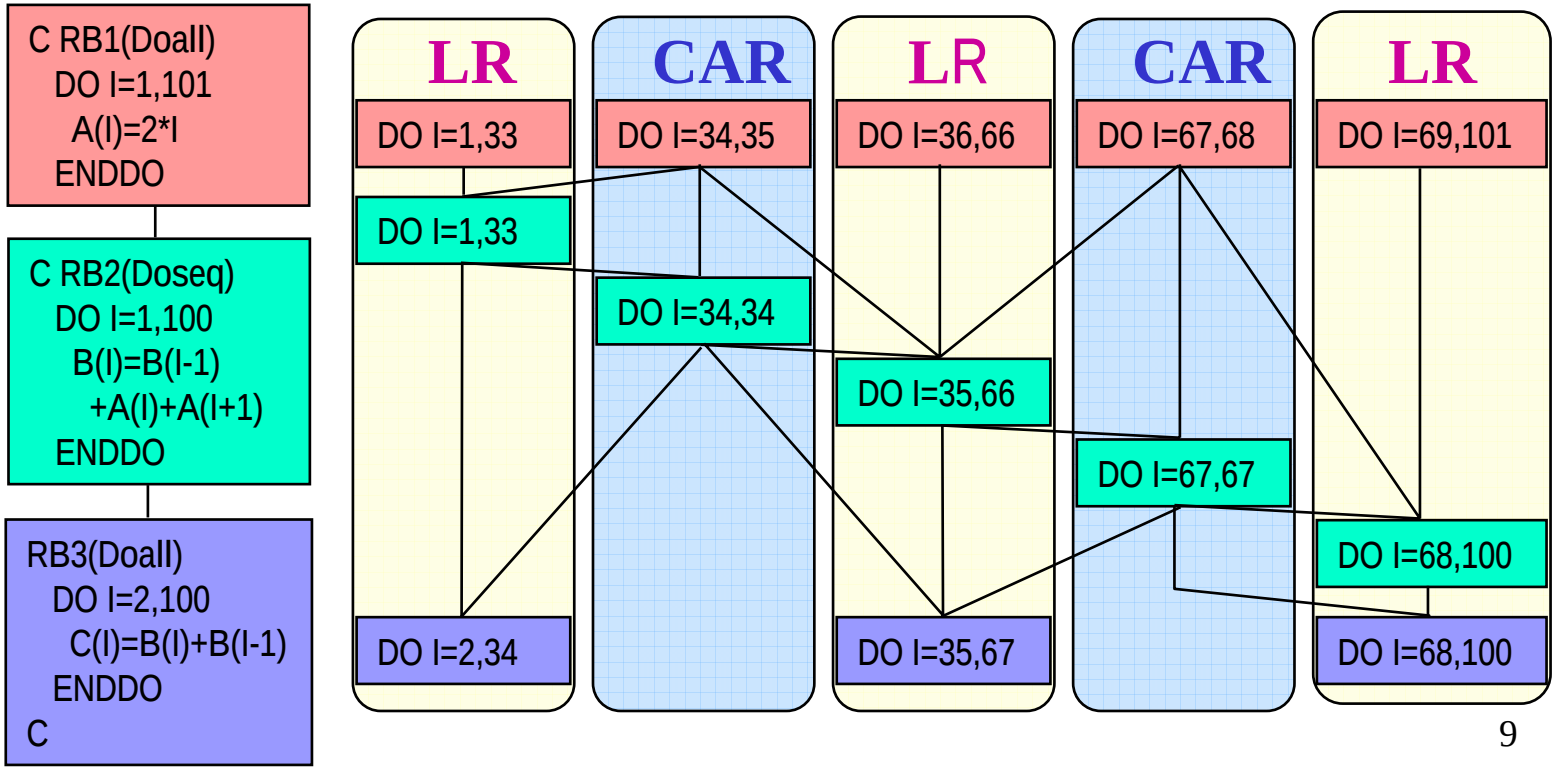
A Macro Flow Graph



A Macro Task Graph

Data-Localization
Loop Aligned Decomposition

- **Decompose multiple loop (Doall and Seq) into CARs and LRs considering inter-loop data dependence.**
  - **Most data in LR can be passed through LM.**
  - **LR: Localizable Region, CAR: Commonly Accessed Region**



APC Compiler Organization

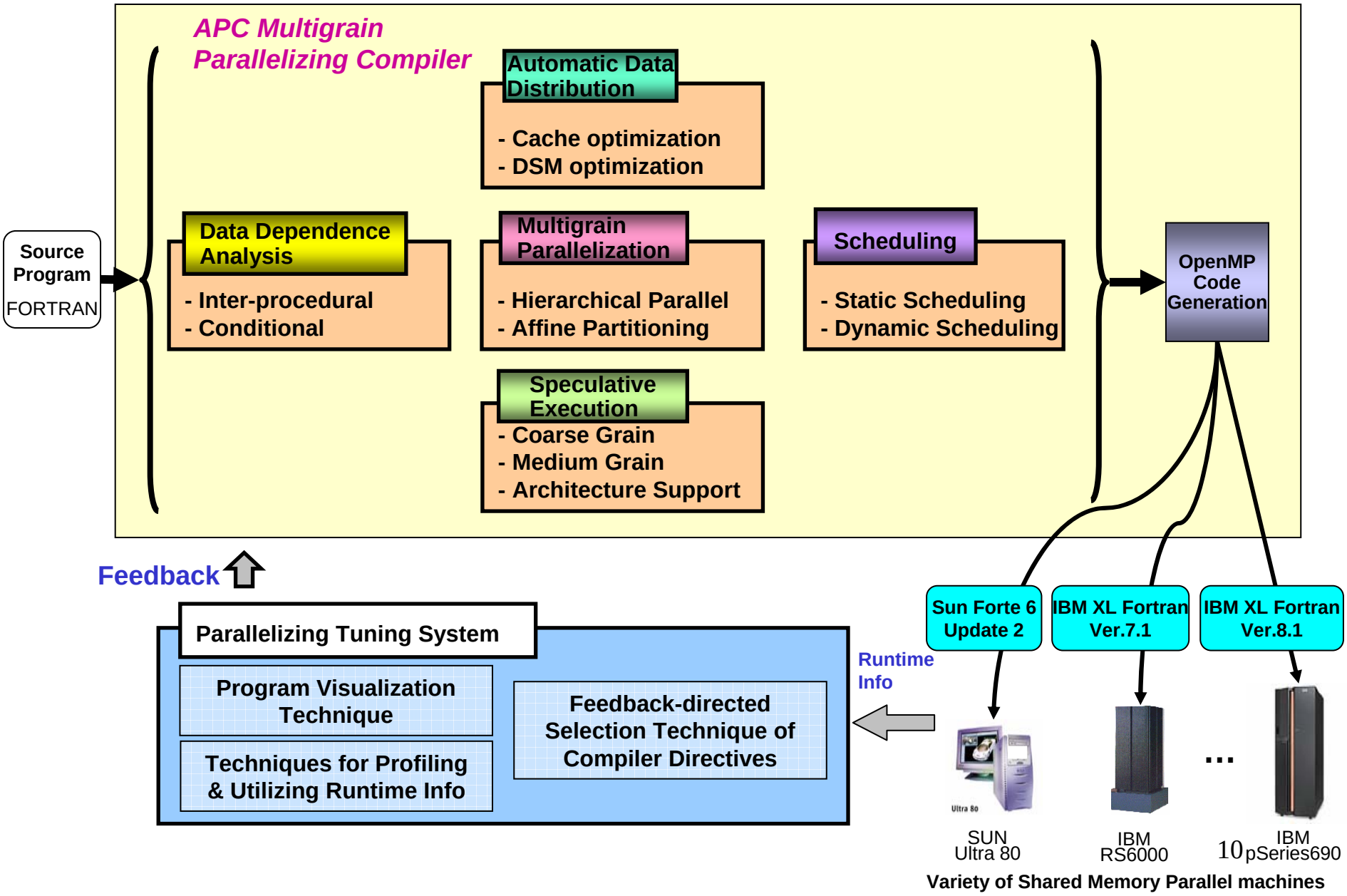
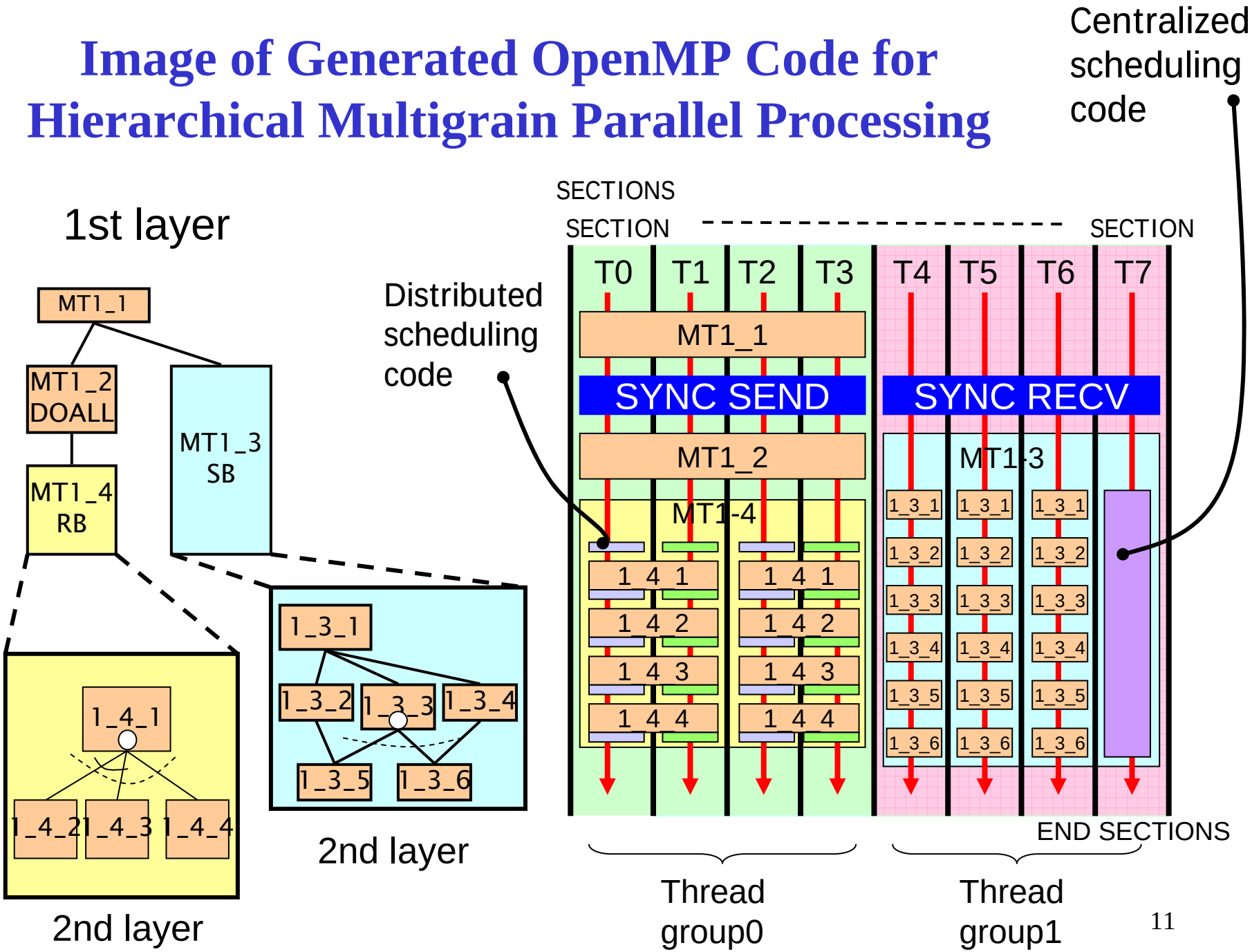
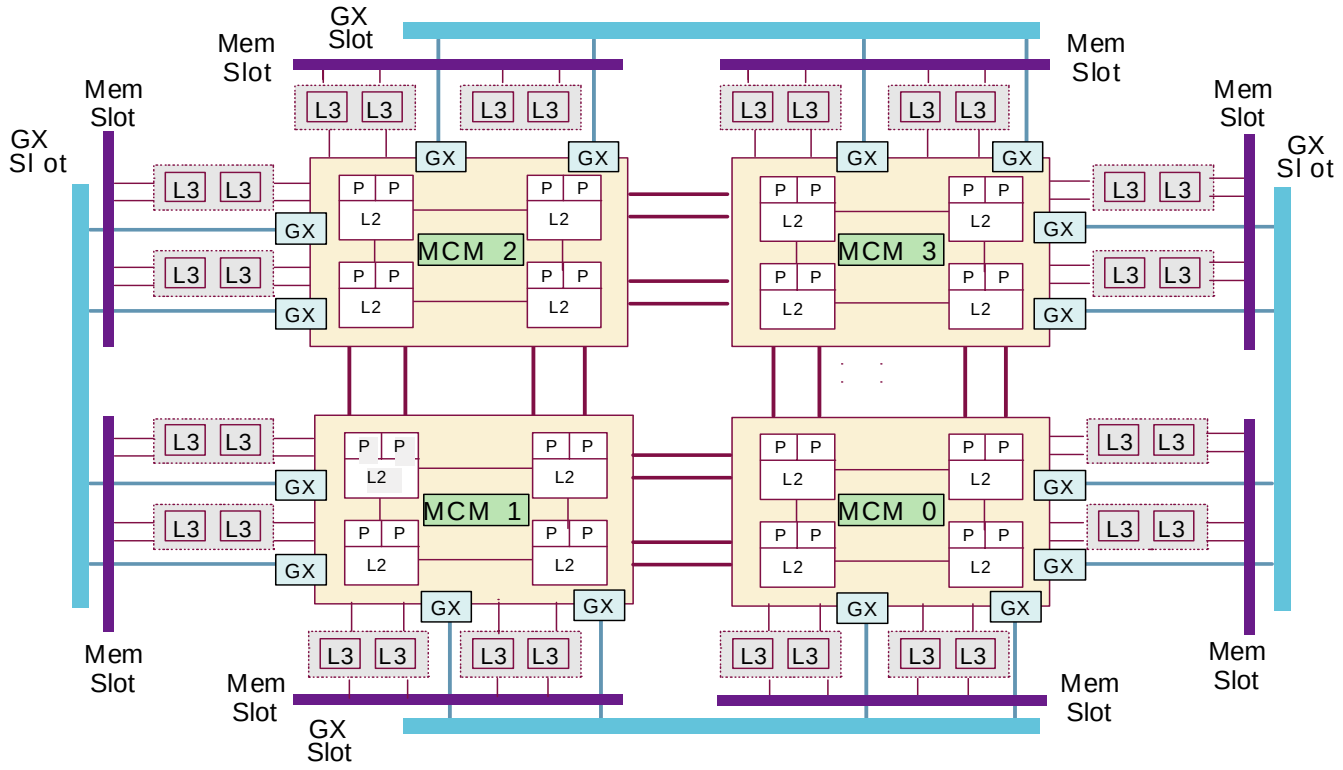


Image of Generated OpenMP Code for Hierarchical Multigrain Parallel Processing



IBM pSeries690 RegattaH

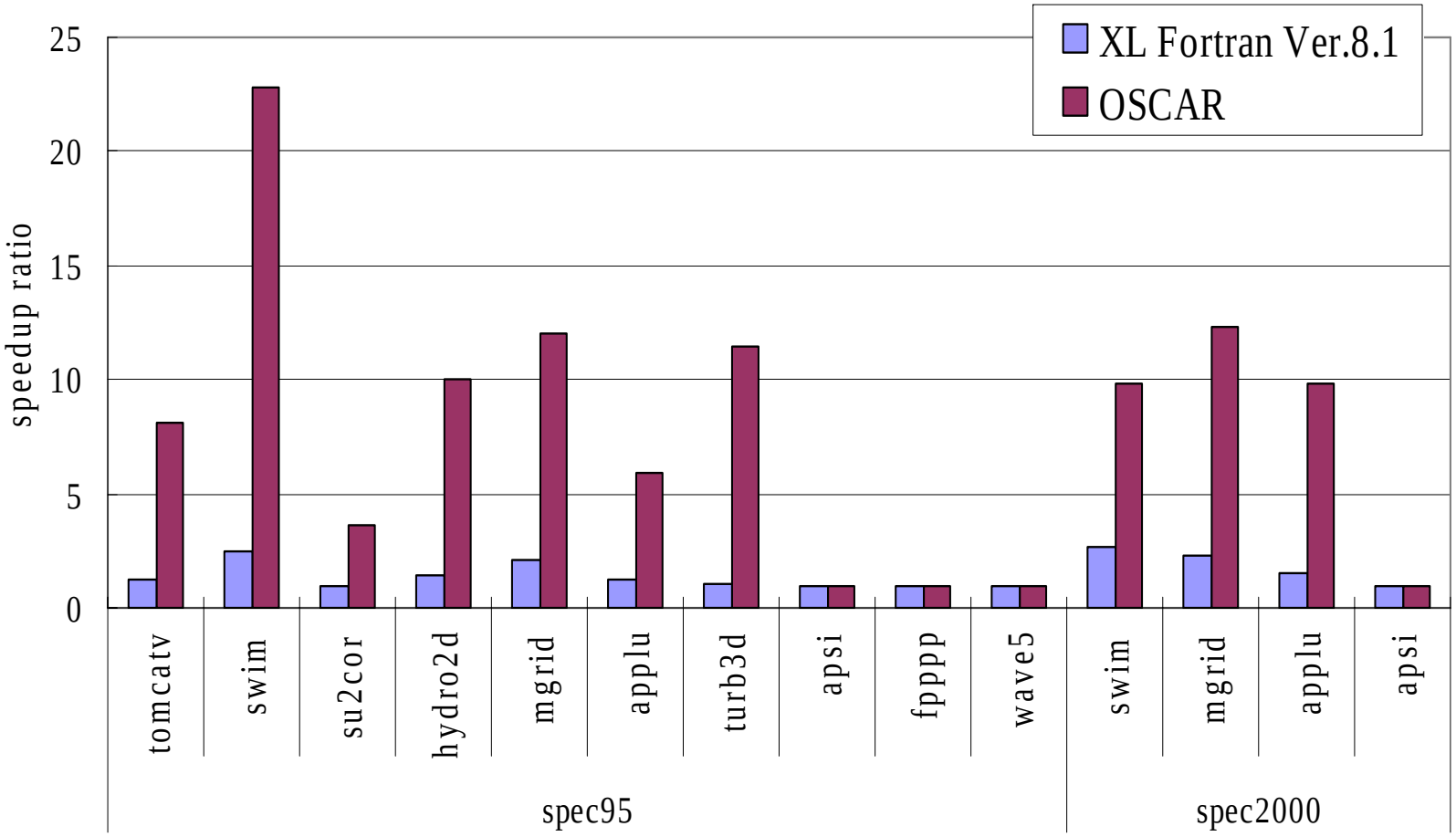
- Up to 16 Power4: 32 way SMP Server
  - L1(D) : 64 KB (32KB/processor, 2 way assoc.), L1(I): 128 KB (64KB/processor, Direct map)
  - L2 : 1.5 MB (shared cache with 2 procs., 4~8 way assoc.)
  - L3 : 32 MB (external, 8 way assoc.) [x 8 = 256 MB]



Four 8-way MCM Features Assembled into a 32-way pSeries 690

http://www-1.ibm.com/servers/eserver/pseries/hardware/whitepapers/p690_config.html

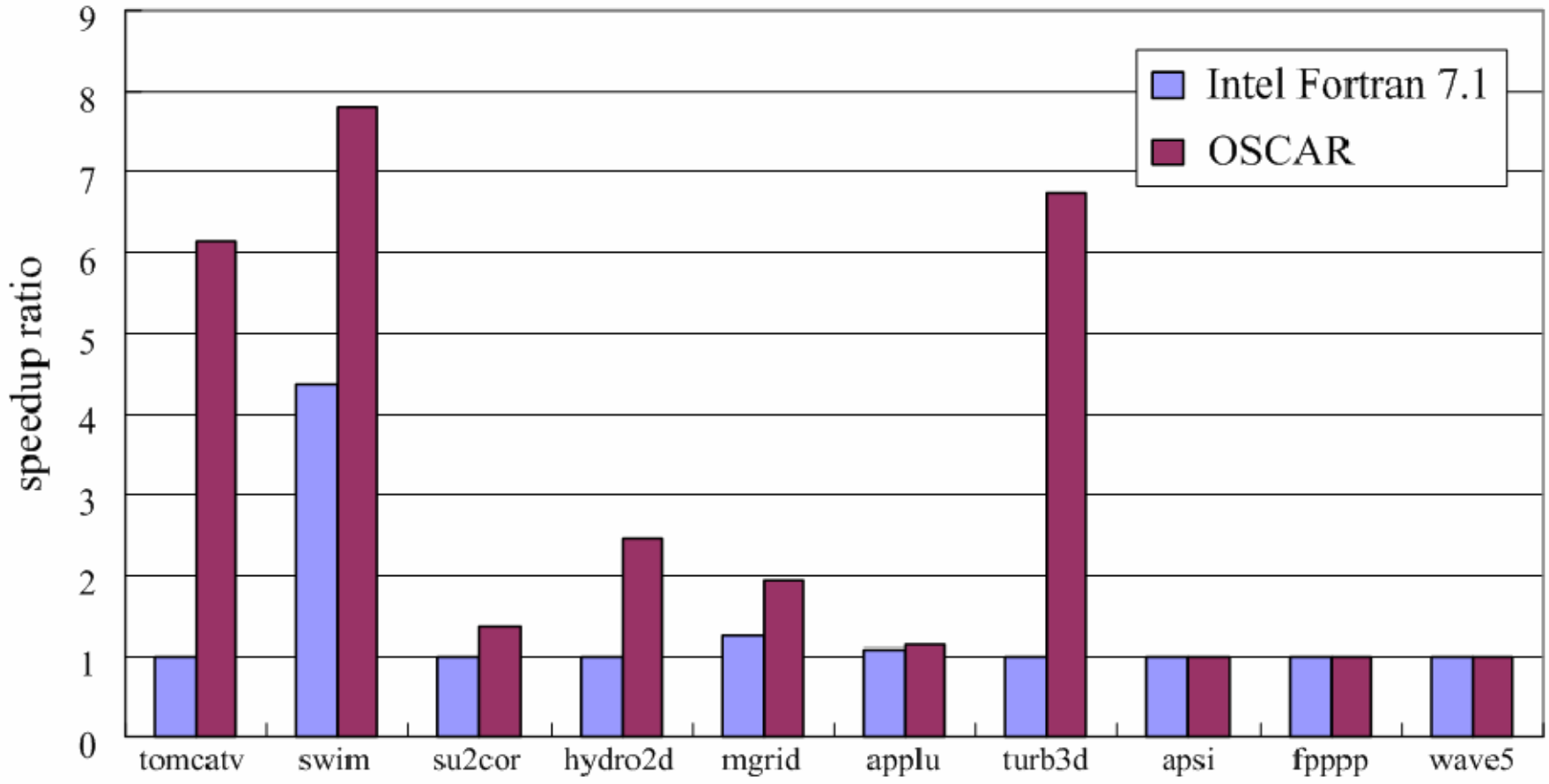
Performance on IBM pSeries690 Power4 24 processors SMP server



- OSCAR compiler gave us 4.82 times speedup against XL Fortran Ver.8.1

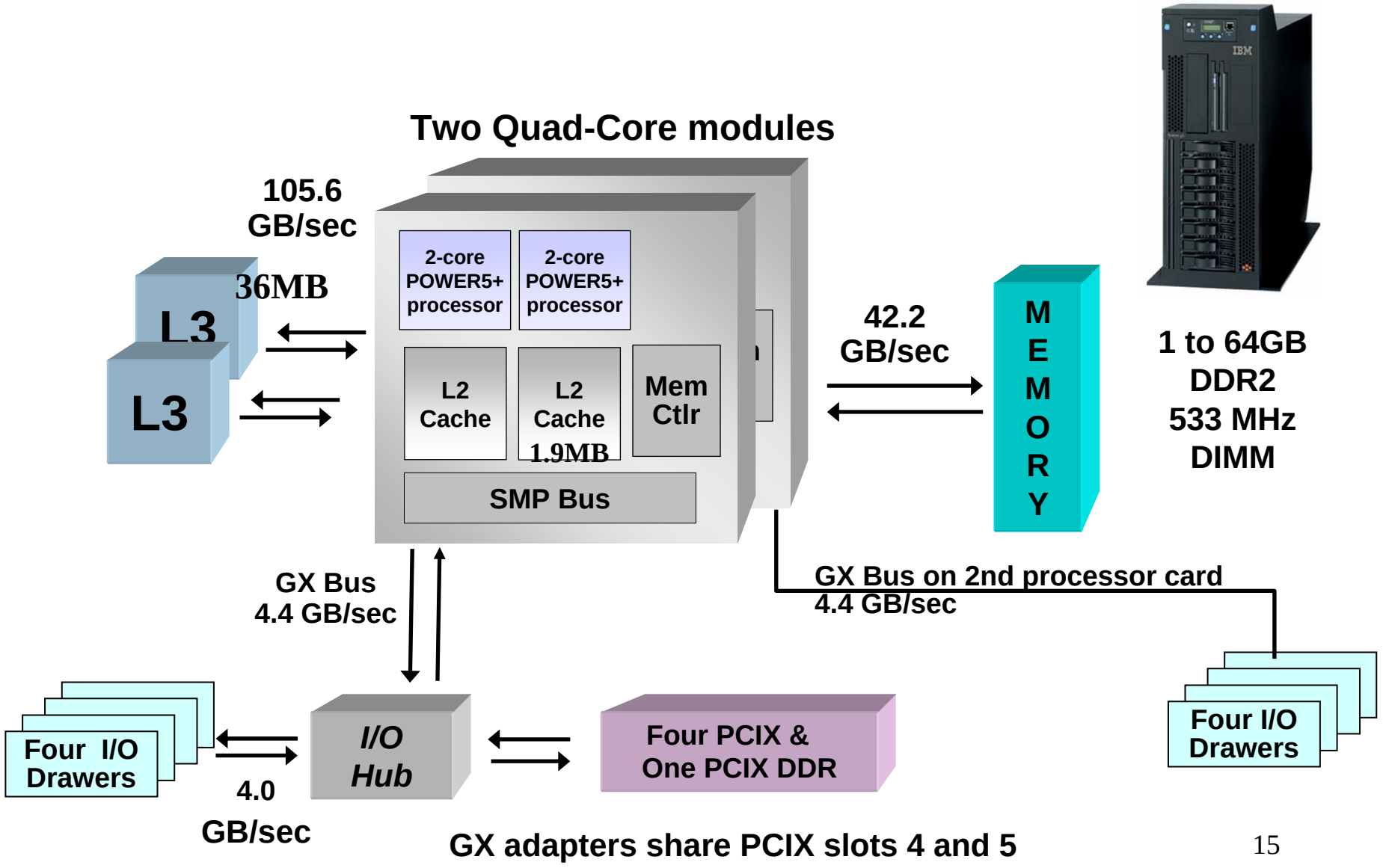
SGI Altix 350

16 Itanium 2 (1.3GHz) SMP server
L1 16KB(4way), L2 256KB(8way), L3 3MB(12way)

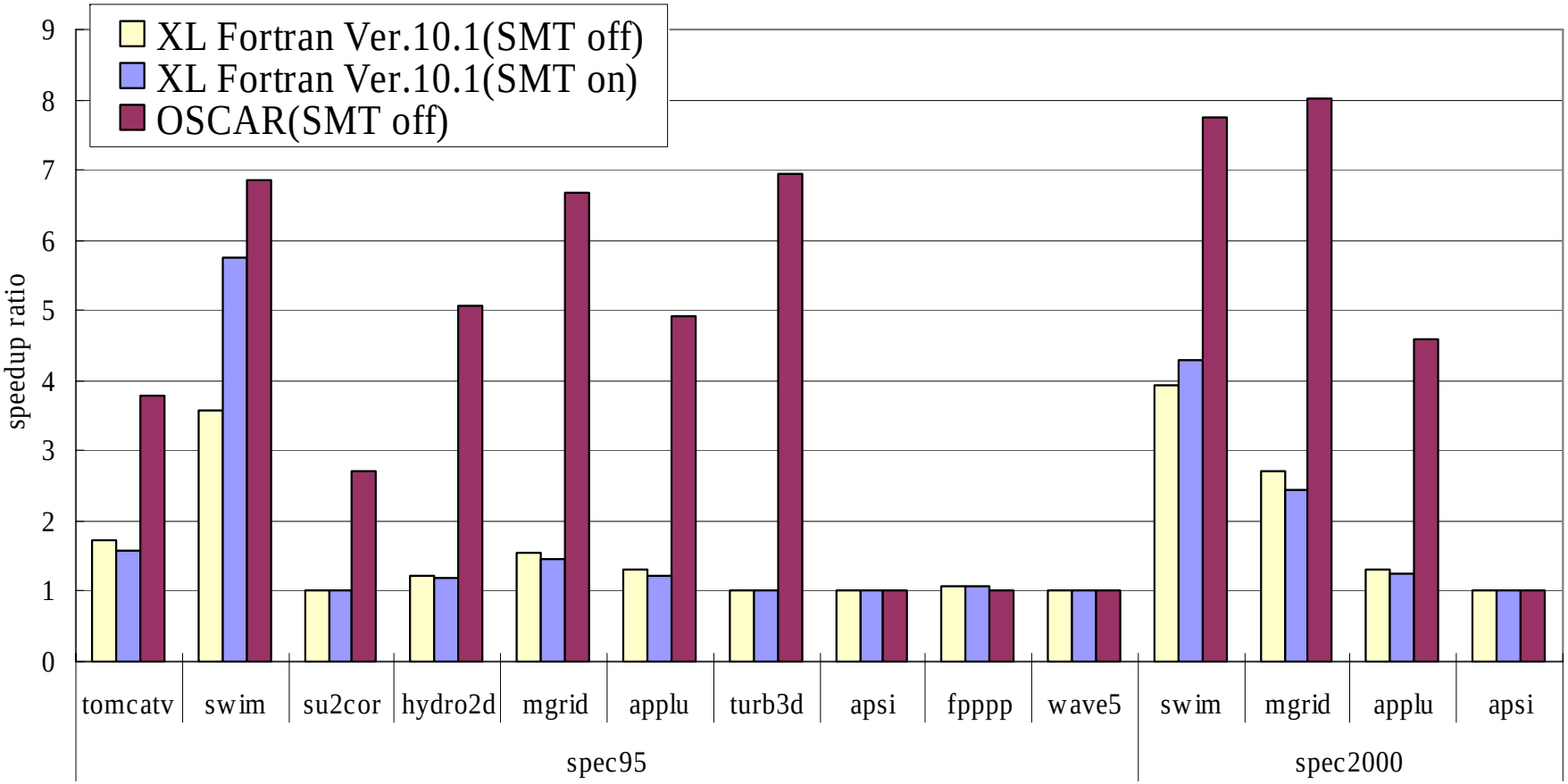


2.4 times speedup against Intel Fortran 7.1 using OpenMP code for IBM p690

IBM p5-550Q server (1.5 or 1.65 GHz)



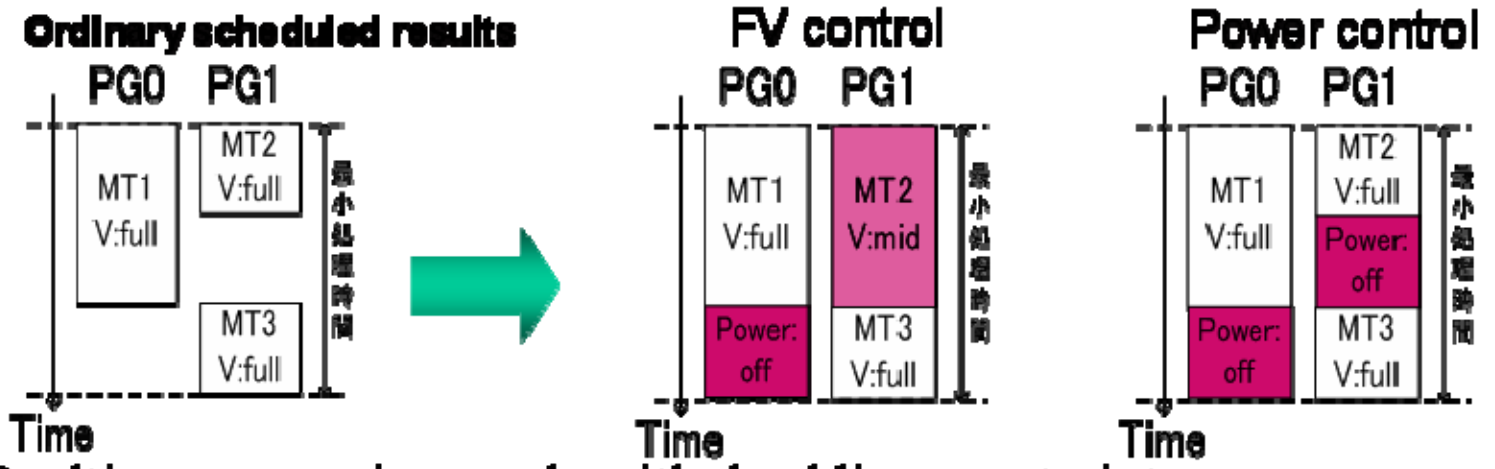
Performance on IBM p5 550 POWER5+ 8 processors SMP server



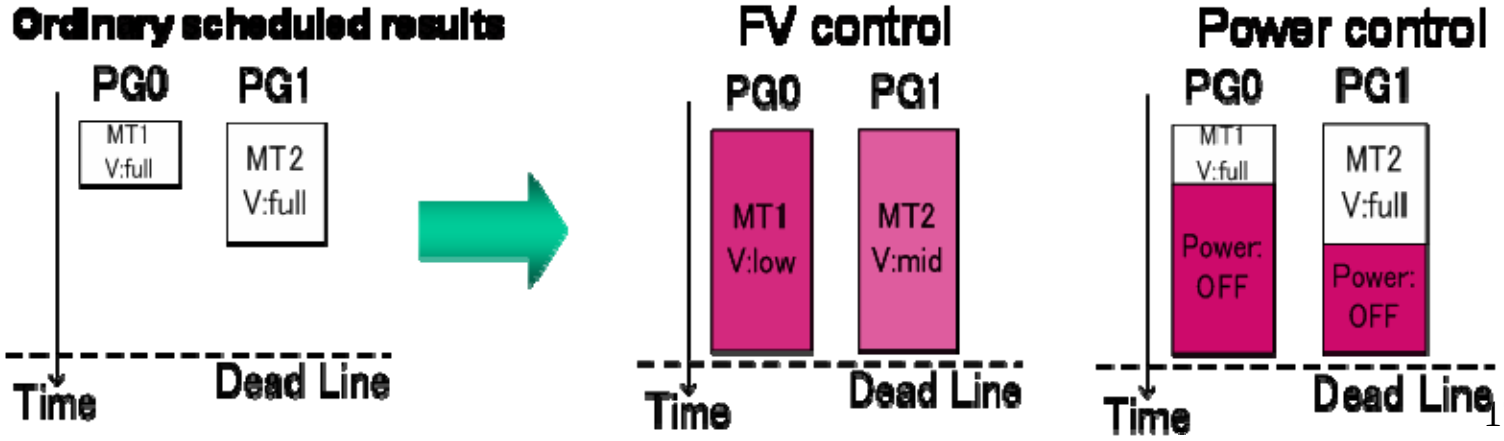
- OSCAR compiler
  - 2.74 times speedup against XL Fortran Ver.10.1 without SMT
  - 2.78 times speedup against XL Fortran Ver.10.1 with SMT

Power Reduction by Power Supply, Clock Frequency and Voltage Control by OSCAR Compiler

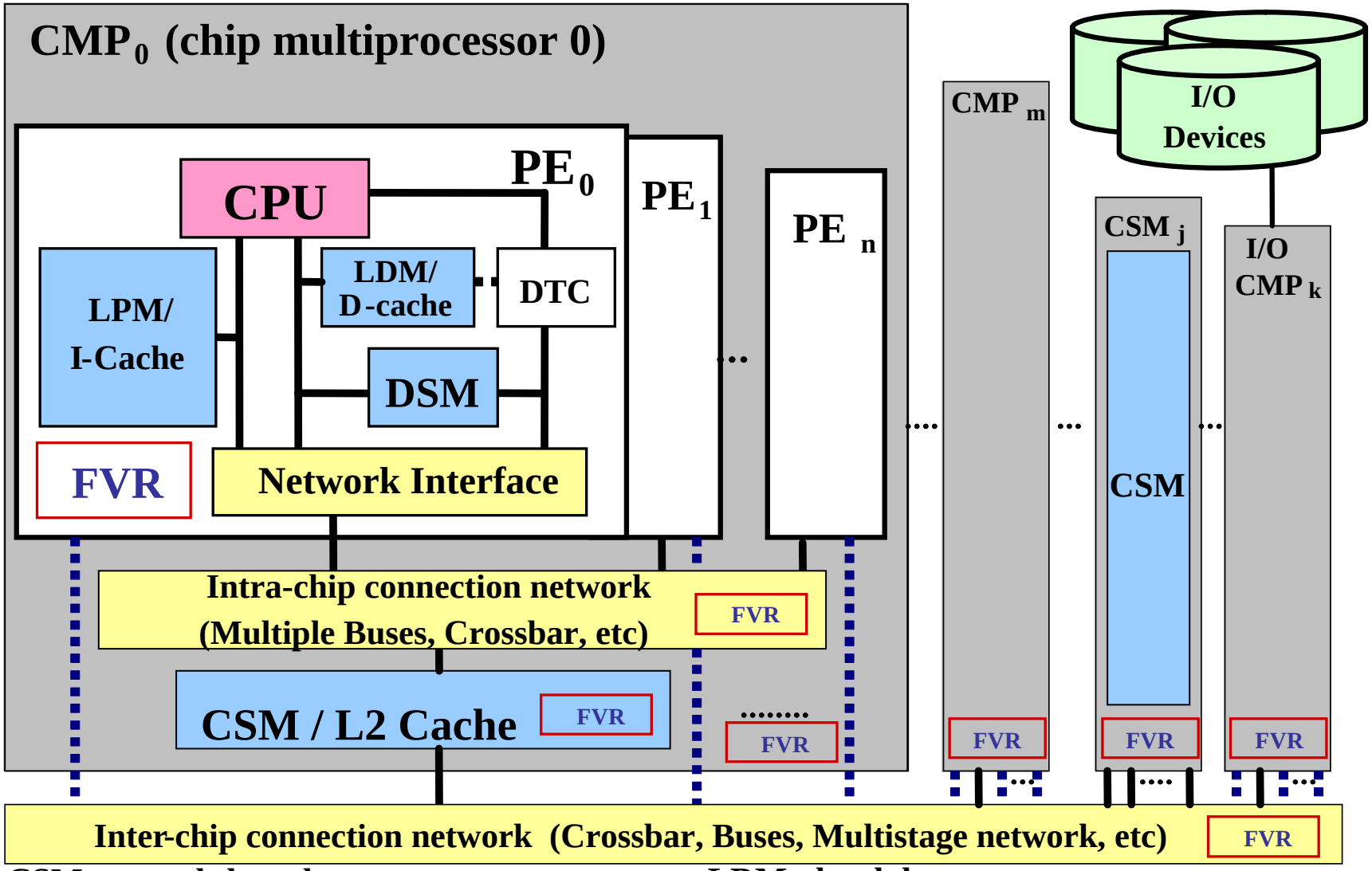
- Shortest execution time mode



- Realtime processing mode with dead line constraints



OSCAR Multi-Core Architecture



CSM: central shared mem.

DSM: distributed shared mem.

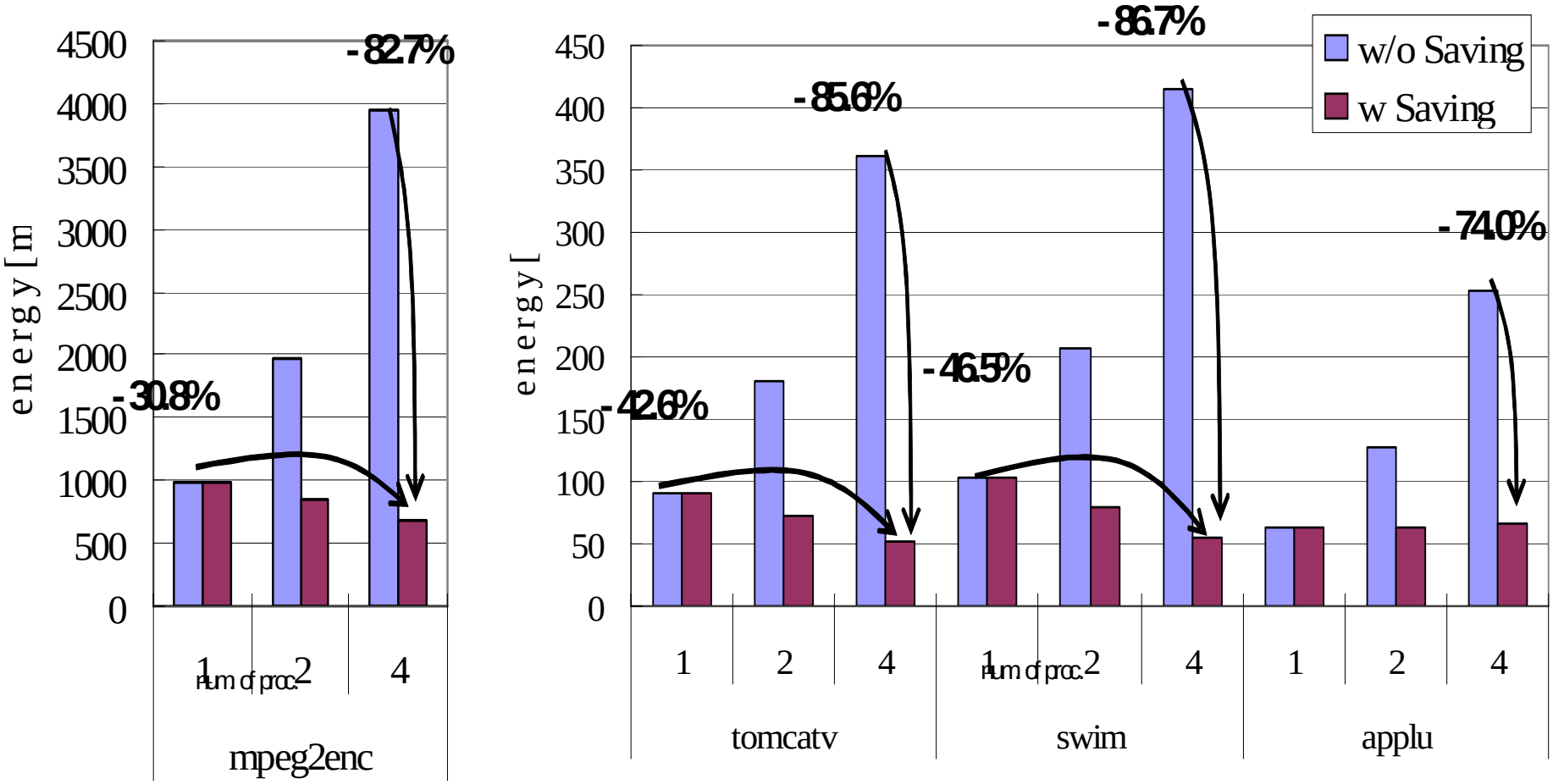
DTC: Data Transfer Controller

LDM : local data mem.

LPM : local program mem.

FVR: frequency / voltage control register

Consumed Energy in Real-time Processing mode



- deadline = sequential execution time

Parallel Processing of VLSI Electronic Circuit Simulation